High-performance Silicon Arrayed-Waveguide Grating (De)multiplexer with 0.4-nm Channel Spacing

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Abstract. A high-performance silicon arrayed-waveguide grating (AWG) with 0.4-nm channel spacing for dense wavelength-division multiplexing (DWDM) systems is designed and realized successfully. The device design involves broadening the arrayed waveguides far beyond the singlemode regime, which minimizes random phase errors and propagation loss without requiring any additional fabrication steps. To further enhance performance, Euler-bends have been incorporated into the arrayed waveguides to reduce the device's physical footprint and suppress the excitation of higher-modes. Additionally, shallowly-etched transition regions are introduced at the junctions between the free-propagation regions and the arrayed waveguides to minimize mode mismatch losses. As an example, a 32×32 AWG (de)multiplexer with a compact size of 900×2200 μm^2 is designed and demonstrated with a narrow channel spacing of 0.4 nm by utilizing 220-nm-thick silicon photonic waveguides. The measured excess loss for the central channel is approximately 0.65 dB, the channel non-uniformity is around 2.5 dB, while the adjacent-channel crosstalk of the central output port is −21.4 dB. To the best knowledge, this AWG (de)multiplexer is the best one among silicon-based implementations currently available, offering both dense channel spacing and a large number of channels.

Keywords: arrayed-waveguide grating, dense wavelength-division multiplexing, silicon.

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1 Introduction

The integration of optoelectronics based on silicon has rapidly gained traction in recent years due to its unique benefits such as compatibility with Complementary Metal-Oxide-Semiconductor (CMOS) technology and the ability to achieve extremely high levels of integration[1, 2]. As a result, it has garnered widespread interest globally and led to the development of a variety of incredibly ultra-compact silicon photonic devices[3]. One particular type of device that stands out as being highly promising and widely applicable is arrayed-waveguide gratings (AWGs)[4]. Despite the ease with which ultra-small AWGs can be created using singlemode silicon photonic waveguides, which boast exceptionally high refractive index differences and diminutive cross-sectional dimensions, these AWG devices often suffer from substantial random phase errors, leading to severe channel crosstalk and elevated excess losses. Over the last two decades, researchers have made considerable strides in developing miniaturized yet high-performance AWG devices[5-11], but

achieving DWDM-grade AWGs (with channel spacings of less than or equal to 1.6 nm) remains a daunting challenge, hindering their widespread adoption. In our prior work, we demonstrated a 16×16 AWG with channel spacing of 1.6 nm by employing a groundbreaking design strategy that involved uniformly broadening the arrayed waveguides far beyond the singlemode condition[12]. Thanks to this innovative approach, the crosstalk of the central channel was significantly reduced to as low as −31.7 dB (a notable improvement of approximately 10 dB over earlier results). Significantly, this inventive technique did not necessitate any specialized processing steps, relying instead on straightforward single-etching methods that did not significantly contribute to excess loss or increased footprint sizes, underscoring its exceptional practical value and real-world applicability.

While significant progress has been made in realizing AWGs for DWDM applications, there remains a pressing need to push the boundaries of these technologies even further by developing devices capable of supporting channel spacings as narrow as 0.8 nm, or even 0.4 nm. This presents a formidable technical challenge, as the inter-channel crosstalk tends to skyrocket under such conditions. For instance, an AWG router with a channel spacing of just 0.2 nm was demonstrated in [13][13], but suffered from unacceptably high inter-channel crosstalk of approximately −4 dB. In 2013, S. Pathak et al. employed this strategy by expanding the straight sections of their arrayed waveguides to 800 nm while maintaining the bent sections in a singlemode configuration to avoid higher-mode excitation and associated crosstalk issues[10]. This technique has proven effective in enabling the realization of AWGs with relatively good performance characteristics. For example, the 0.8-nm-channel-spacing AWG device produced through advanced fabrication techniques[10] exhibits an inter-channel crosstalk of around −17 dB. Regarding the excess loss in this specific type of AWG design, it was estimated to be approximately 2.5 dB. This level of attenuation was

achieved through the introduction of shallowly etched transition regions between the free propagation regions (FPRs) and the arrayed waveguides. By implementing these features, it became possible to effectively minimize mode-mismatch losses while preserving the overall functionality and performance of the AWG architecture. However, there have been no reports to date of high-performance silicon-based AWG (de)multiplexers capable of operating with channel spacing as narrow as 0.4 nm, highlighting the ongoing challenges faced in this area of research.

In this paper, we present a compact silicon AWG incorporating Euler-bend-assisted arrayed waveguides, with both straight- and bent-sections expanded to a width of up to 2 μm. Previous research has established that adopting broader photonic waveguides can significantly reduce random phase errors in optical interference systems, including Mach-Zehnder Interferometers (MZIs)[14] and AWGs[12]. In addition, we have incorporated Euler bends with a gradient curvature design to minimize higher-order mode excitation and ensure low-loss monomode transmission for the fundamental modes. By leveraging these principles, we expect to dramatically decrease random phase errors stemming from fabrication imperfections, thereby reducing channel crosstalk, and improving fabrication tolerances. Furthermore, we have introduced shallowly-etched transition regions (SETRs) to connect the arrayed waveguides to the FPRs, allowing us to keep mode-mismatch losses to a minimum. We demonstrate the effectiveness of this design approach through the realization of a 32×32 silicon AWG with a narrow channel spacing of 0.4-nm and a free spectral range (FSR) of 14.6 nm. The measured excess loss for the center channel is found to be 0.65 dB (from input port #17), with channel uniformity across all 32 output channels averaging around 2.5 dB. Importantly, inter-channel crosstalk for the central channel is as low as −21.4 dB (from input port #17). To the best knowledge, we believe that this AWG (de)multiplexer represents

one of the most successful implementations in terms of performance among comparable silicon-based AWG devices.

2 Principle and design

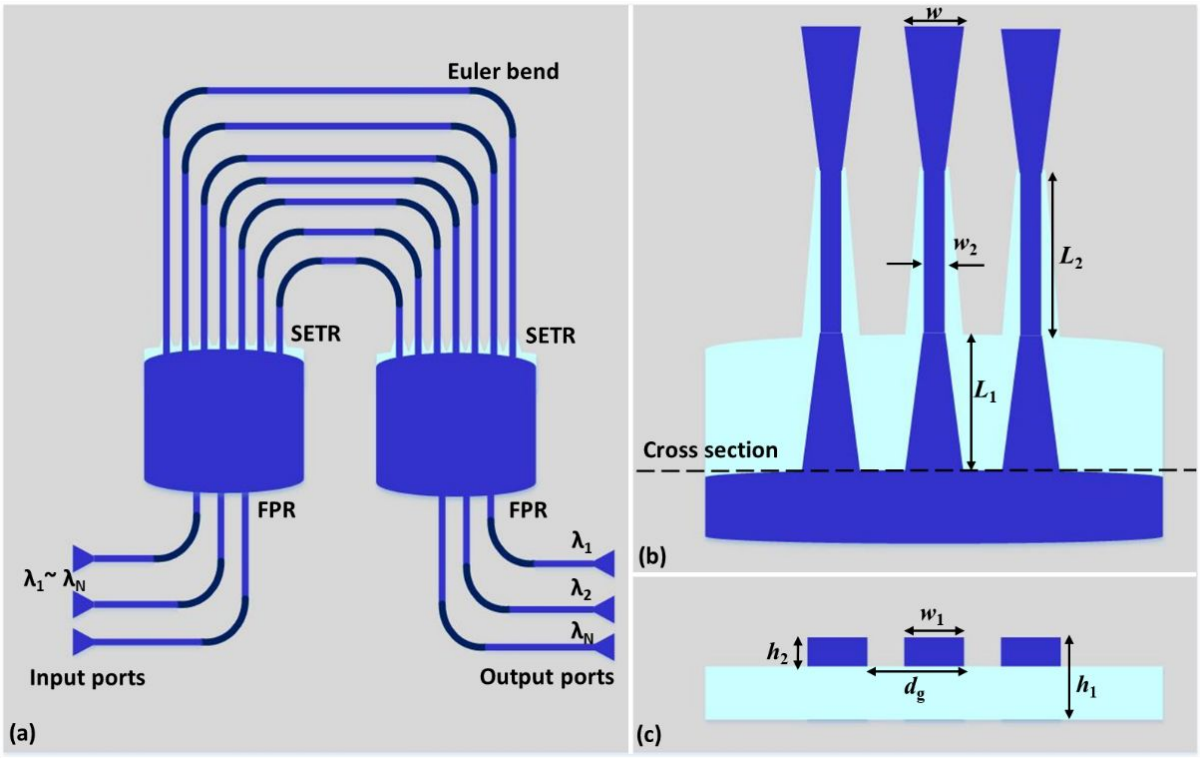

Fig. 1 Schematic configuration of the proposed silicon AWG (a), the partial magnification of the SETR (b), and the cross section (c).

Figure 1 provides a schematic configuration of the proposed silicon AWG, which includes input/output waveguides, two FPRs, two SETRs and broadened arrayed waveguides with Euler bends. The device is optimized for a narrow channel spacing of 0.4 nm and supports up to 32 channels, consistent with the requirements for DWDM systems. **Note that the present AWG is designed for TE polarization regarding that silicon photonic waveguides are usually strongly polarization-dependent due to the ultra-high birefringence. Nevertheless, introducing**

broadened arrayed waveguides is also effective for developing AWGs desired to work with TM polarization. Table 1 gives the key parameters of the present AWG design, including the central wavelength λ_0 = 1550 nm, the interference order m = 80, the length difference ΔL = 43.84 μm, the FPR length L_{FPR} = 200 μm, the pitch d_g = 1.6 μm and the separation d_o = 1.84 μm. With these parameters, the FSR of the AWG device is estimated to be approximately 14.6 nm, covering the full range of 32 channels as intended. In this implementation, the arrayed waveguides are intentionally broadened to 2 μm to minimize random phase errors caused by manufacturing imperfections, thus improving the performance with low crosstalk, and enhancing the fabrication tolerances. **Compared with the traditional AWG whose arrayed waveguides are designed by following the singlemode condition, this present innovative design can significantly reduce the cumulative random phase error of the arrayed waveguides by as high as 100 times[12].** Additionally, Euler-bend-assisted arrayed waveguides are employed to mitigate higher-order mode excitation and promote low-loss transmission of the fundamental mode. For this purpose, we employ a gradient curvature design, with maximum and minimum radii set to 2000 μm and 20 μm, respectively, resulting in an effective radius of 37.1 μm. **In the wavelength range of 1500-1600 nm, the additional loss of the TE_0 mode is <0.01 dB, and the inter-mode crosstalk is <−27.1 dB[12]. In contrast, for ordinary arc-bends with the same radius, serious multi-mode interference appears, greatly increasing the transmission loss and the inter-mode crosstalk.** To minimize mode-mismatch losses, SETRs are strategically positioned to bridge the gap between the FPRs and the arrayed waveguides. These components play a crucial role in ensuring efficient coupling of light from the FPR to the fundamental mode in the arrayed waveguides. Further details on the design of the SETRs are given in the subsequent section.

Table 1 Parameters of the designed AWG device.

Parameters	N	$\Delta\lambda_{ch}$ (nm)	λ_0 (nm)	m	L_{FPR} (μm)	d_g (μm)	d_o (μm)	ΔL (μm)	FSR (nm)
Value	32	0.4	1550	80	200	1.6	1.84	43.84	14.6

Figure 1(b)-(c) zoom in on the structure and layout of the SETR, which comprises two distinct segments: a shallowly-etched region and a transition zone connecting this area to a deeply-etched region. Within the shallowly-etched region, we utilize varying widths along the ridge waveguide, controlled by parameters h_1 (set at 220 nm) and h_2 (set at 70 nm) defined by the manufacturing process. To minimize higher-order mode generation during the transition from the FPR to the arrayed waveguides, careful consideration must be given to selecting optimal values for w_1, L_1 and L_2 in the first part of the SETR and the adiabatic taper connecting them. During this transitional stage, the width decreases gradually to match the width (w_2 = 0.45 μm) specified for arrayed waveguides, filtering out remaining higher-order modes. By carefully designing these geometric aspects of the transition zone, we can facilitate smooth transfer of energy into the dominant mode of the arrayed waveguide and prevent unwanted modes from entering the system, contributing to enhanced signal quality and reduced crosstalk within the AWG architecture.

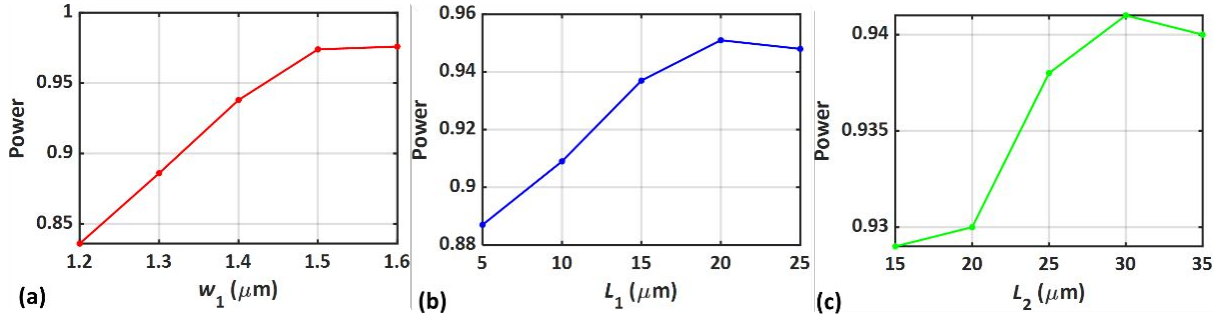

Fig. 2 Calculated the ratio of the TE_0 mode power when choosing different waveguide widths w_1 (a), different taper lengths L_1 (b) and different taper lengths L_2 (c).

Figure 2(a) provides a simulation analysis for the dependence of the ratio of the TE_0 mode coupled power at the FPR-to-SETR interface on the width w_1, which is the initial width of the shallowly-etched portion of the transition region. Here the central wavelength is 1.55 μm. The simulations results show that the ratio of the TE_0 mode coupled power increases proportionally with the width w_1. Regarding that the minimal gap between adjacent arrayed waveguides should be more than of 200 nm (according to the fabrication requirements), we choose w_1 = 1.4 μm to achieve high coupling efficiency. Figures 2(b)-(c) demonstrate how the taper lengths L_1 and L_2 affects the coupling efficiency, revealing that the combination with L_1 = 20 μm and L_2 = 30 μm yields satisfactory performance and ensures compactness without energy leakage between neighboring waveguides.

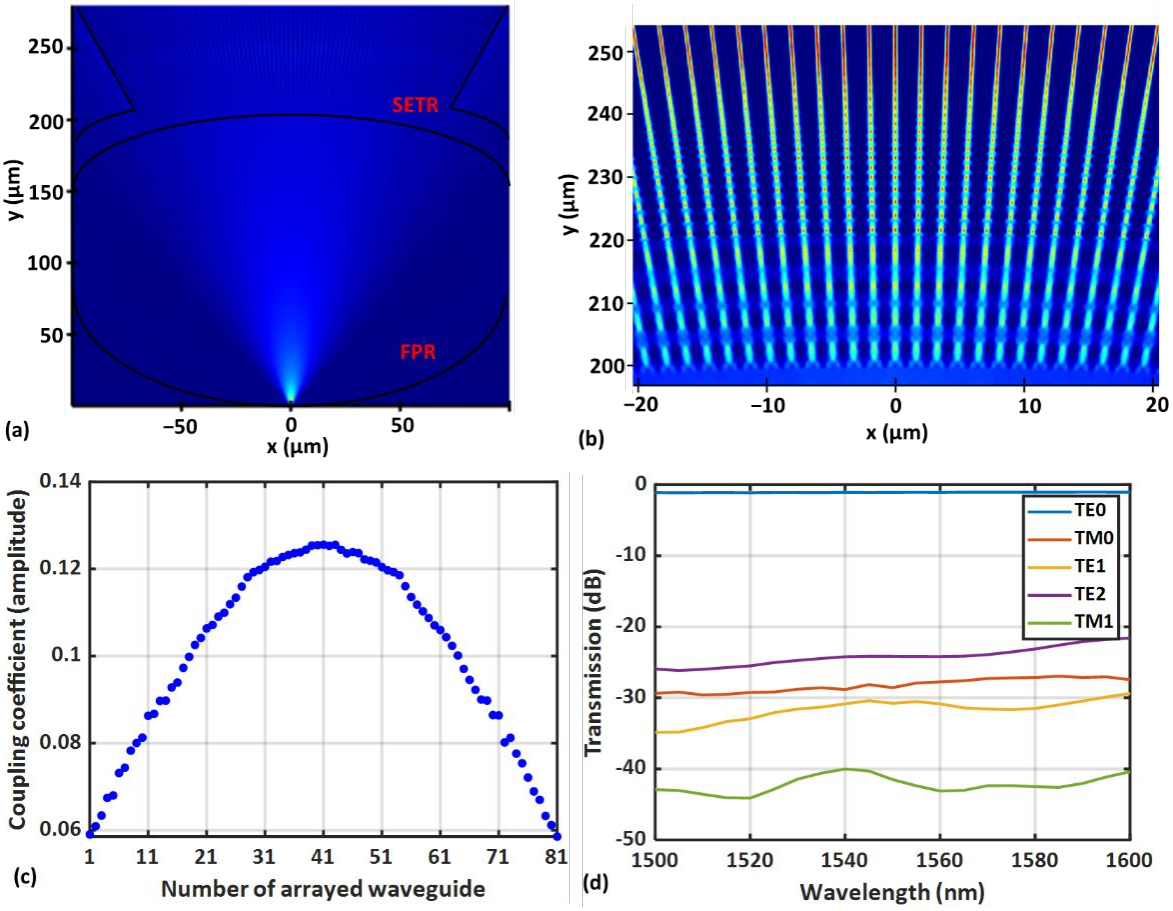

Fig. 3 (a) Stimulated optical field distribution of the FPR and the SETR; (b) Stimulated optical field distribution of the SETR (part); (c) The coupling coefficient: the amplitude distribution; (d) Excess loss and crosstalk of the first FPR and the SETR when light is launched from the center input port.

Figure 3(a) demonstrates the simulated light propagation throughout the FPR and the SETR portions of the designed AWG, while Fig. 3(b) shows the more details about the part of the arrayed waveguides. It can be seen that the light propagation experiences low scattering and negligible excitation of higher-order modes. As a result, the designed SETR region works very well as expected. Figure 3(c) provides the calculated coupling power ratios for all the individual arrayed waveguides, showing a Gaussian profile as predicted theoretically. The total power carried by all the arrayed waveguides suggests that the excess loss from the SETR-FPR connection is ~0.5 dB. Furthermore, Figure 3(d) reveals the power ratios of all the guided modes (TE_0, TM_0, TE_1, TE_2, and TM_1), which shows that high-order modes are suppressed very well with a high extinction ratio of >25 dB in the operating band of 1.5-1.6 μm. Overall, these simulation results confirm the viability of the proposed design and further efforts may be necessary to improve the performance if needed.

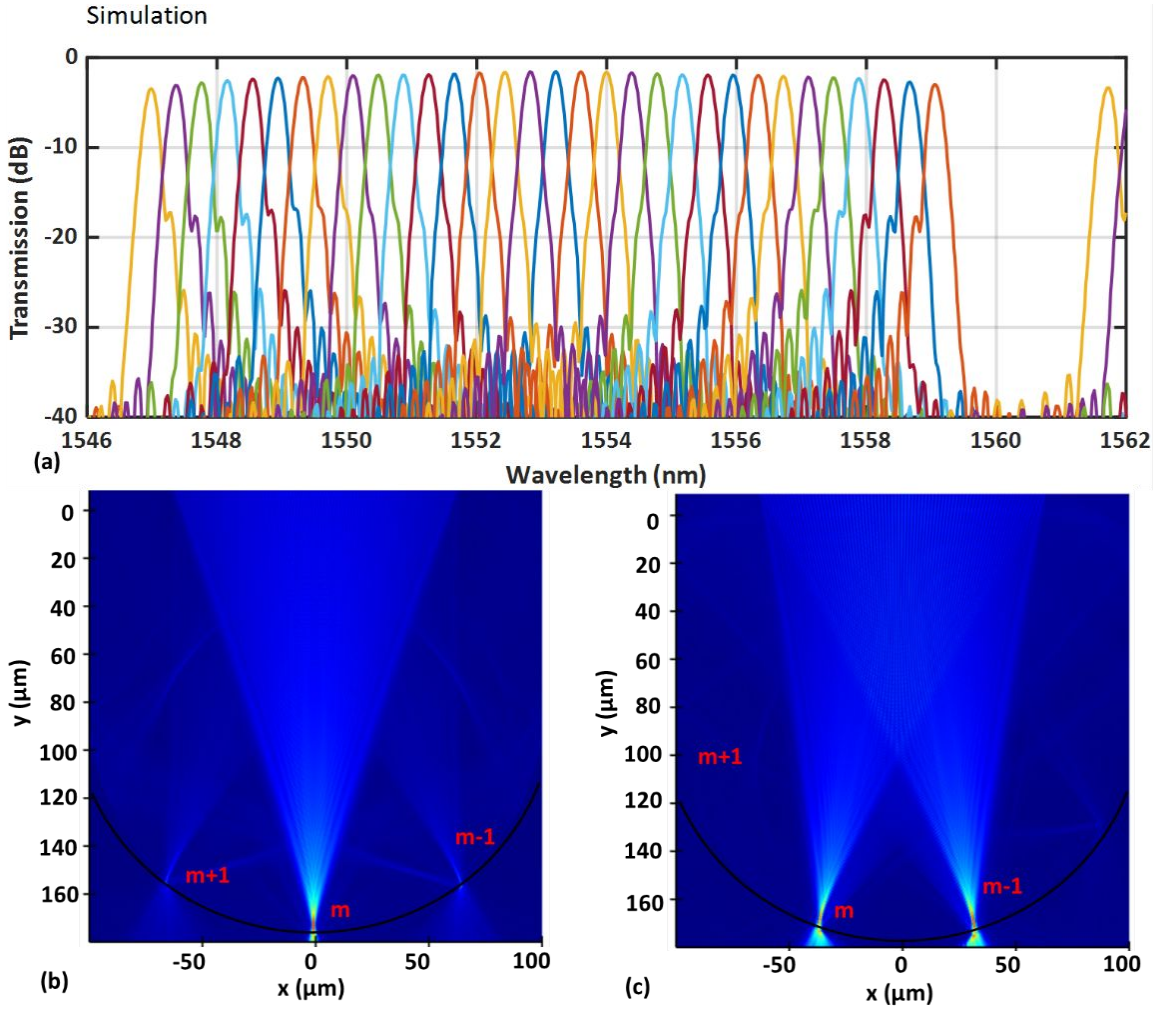

Fig. 4 (a) Stimulated spectral responses of all 32 channels of the designed AWG; Stimulated light propagation in the second FPR for the center channel (b) and the edge channel (c).

Figure 4(a) presents the numerically simulated spectral responses of the 32 channels in the designed AWG. It can be seen that the central channel exhibits a low excess loss of 0.69 dB and the channel non-uniformity is approximately 2.5 dB. The FSR is about 14.6 nm, which closely matches the theoretical predictions. The crosstalks between the adjacent and non-adjacent channels are less than −25 dB and −30 dB for the central channels, respectively. In contrast, the adjacent-channel crosstalk becomes ~ −20 dB for the edge channels. Figure 4(b) and 4(c) show the light propagation in the FPR when the central channel with the wavelength of 1.552 μm and the edge

channel with the wavelength of 1.560 μm is considered. One can see the focusing spots corresponding to the interference orders of $m-1$, m, and $m+1$, respectively. Particularly, for the edge channel shown in Fig. 4(c), the power is distributed at the orders of $m-1$ and m, which is the reason why the edge channel has a relatively high excess loss.

3 Fabrication and characterization

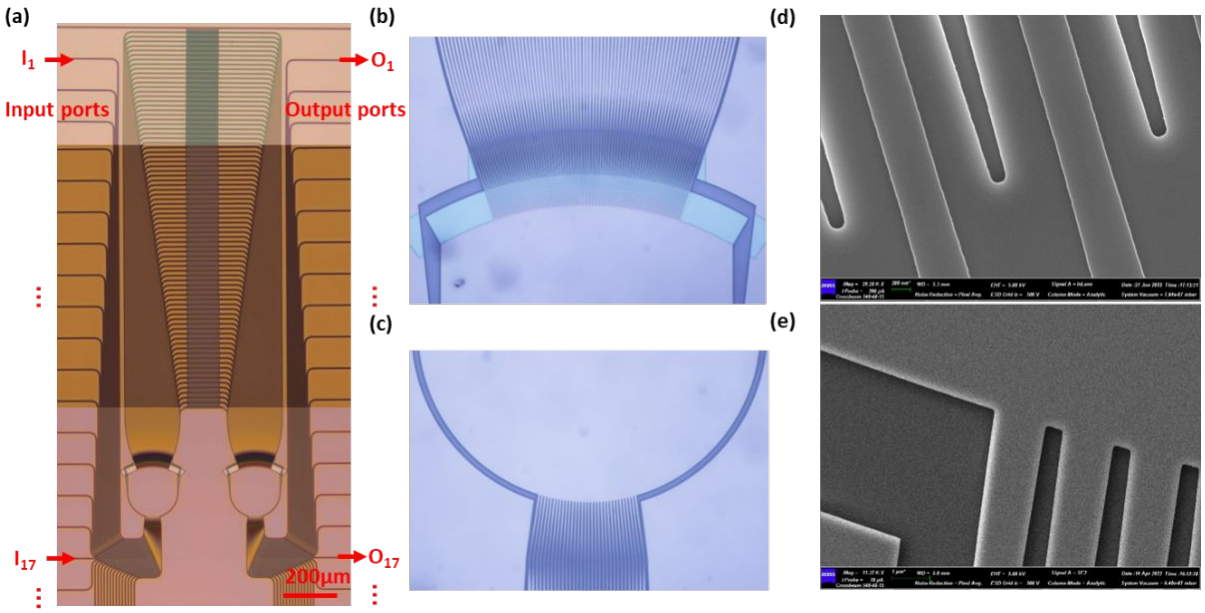

Fig. 5 (a) Microscope image of the fabricated 32×32 AWG; (b) Microscope image of the fabricated SETR; (c) Microscope image of the fabricated input/output tapers; (d) The scanning electron microscope image of the SETR; (e) The scanning electron microscope image of the input/output tapers.

The AWG was fabricated with an Electron Beam Lithography (EBL) process and inductively coupled plasma (ICP) dry-etching techniques on a silicon-on-insulator (SOI) wafer featuring a top-silicon layer thickness of 220 nm and a 2-μm thick buried oxide layer. A 1.5-μm thick SiO_2 layer was then added as an upper-cladding layer. Figures 5(a)-(c) show the microscopy images of the fabricated 32×32 AWG, highlighting the connection points between the FPR and the arrayed waveguides as well as input/outputs. Additional scanning electron microscopy (SEM) images

provides close-up views of the SETR area and the tapers, as shown in Figure 5(d)-5(e). For the characterization of the fabricated device, the ASE light was coupled into the input ports via TE grating couplers, and the transmitted light was then analyzed using an optical spectrum analyzer (OSA) after being collected by the singlemode fibers attached to the output ports. Figure 5(a) also shows the fabricated AWG chip with 32 input ports (i.e., I_1-I_{32}) and 32 output ports (i.e., O_1-O_{32}).

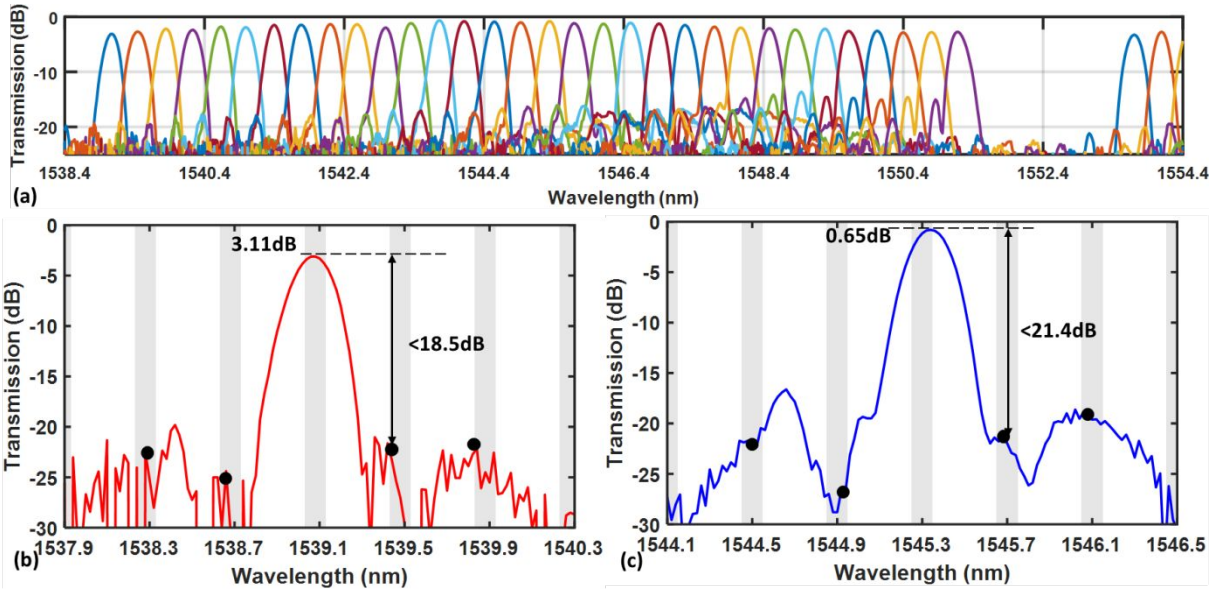

Fig. 6 Measured spectral responses of all output ports (a), the edge output port (#1) (b), and the central output port (#1) (c). Here, light was lunched from the central input port (#17).

Figure 6(a) displays the measurement data obtained when the ASE light were injected into the central input port #17 of the fabricated 32×32 AWG, showing a uniform channel spacing of 0.4 nm and an FSR of 14.7 nm, which is consistent with the design expectation. **Here it was normalized with respect to the transmission of a 2-μm-wide straight waveguide with the same TE grating couplers on the same chip. All input (or output) grating couplers are located in the same column to ensure high uniformity for the fabrication and the fiber coupling.** As shown in Figure 6(b)-(c), the measured excess loss can be as low as ~0.65 dB, the non-uniformity is 2.5 dB, reflecting the challenges posed by non-uniform far-field intensity patterns in the FPR of

an AWG[15]. The potential solution is using long FPRs or manipulating the far field distribution carefully. The measured adjacent-channel crosstalk is −21.4 dB for the central output port (#17), while the measured adjacent channel crosstalk for the edge output port (#1) is −18.5 dB. The measured 1-dB and 3-dB bandwidths are approximately 0.13 nm and 0.21 nm, which also agree well with the simulation prediction. It can be seen that the fabricated AWG works very well, indicating that the present AWG design is excellent.

We have also measured transmissions form all the 32 output ports when light was launched from any one of the input ports (#1~#32). It confirms the consistency with the predicted channel spacing of $\Delta\lambda_{ch}$ = 0.4 nm (corresponding to Δf_{ch} = 50 GHz at 1550 nm). The transmission from the central input port (#17) yields excellent performances with low excess loss of only 0.65 dB, owing to the benefits of introducing broadened arrayed waveguides as well as SETRs. Due to the minor sidelobe, performance degradation is observed when light is lunched from the edge input ports (e.g., #32). The minor sidelobes can be removed by improving the fabrication as well as correcting the aberration of the Rowland circle design[16]. Switching between different inputs highlights the characteristics of wavelength-shifting, as expected for AWGs, and uniform channel spacing persists across the operational bandwidth regardless of input selection, providing the potential realization of cyclic AWG for different scenarios.

Table 2 Comparison of reported SOI AWGs.

Ref.	Channel spacing (nm)	Channel number	FSR (nm)	Excess loss (dB)	Crosstalk (dB)	Footprint (μm²)
17	3.2	16	51.2	3	−19	475×330
18	3.2	16	54	1.5	−26	530×435
10	3.2	12	69.8	0.5	−21.3	380×330
19	2.0	4	8	3.5	−12	425×125
10	2.0	8	24.8	1.3	−19.7	540×320
20	1.6	16	25.3	2.2	−20	500×200
18	1.6	16	29	2	−22.5	920×446
21	1.6	16	24.5	3.5	−16	1200×1000
8	1.6	16	25.8	3	−16	-
22	1.6	16	25.6	2.2	−8	580×170
23	1.6	16	25.6	1.45	−15.4	670×370
12	1.6	16	28.9	2.2	-31.7	600×800
10	0.8	4	6.9	2.5	−17.1	1180×285
24	0.7	64	45	5	−10	2300×2000
13	0.2	512	-	45	−4	16000×11000
This	0.4	32	14.7	0.65	−21.4	900×2200

As a summary, Table 2 shows the summary of the reported silicon AWGs with different channel spacings varying from 3.2 nm to 0.2 nm. Here we show the measured results for the excess loss and the crosstalk of only the central input port for simplicity. Among them, our previous AWG with a channel spacing of 1.6 nm[12] has shown the lowest crosstalk. When the channel spacing is reduced further, the AWG size increases greatly and it becomes even more challenging to achieve high performances because the phase errors increase notably. For example, when the channel spacing is reduced to 0.8 nm, the crosstalk of is as high as −17 dB and the excess loss is about 2.5 dB for the AWG demonstrated in [10]. Currently, few results have been reported for AWGs with a 0.4-nm channel spacing, which is considered in this paper. From Table 2, it can be seen that the present AWG exhibits a low crosstalk of −21.4 dB and very low excess losses of ~0.65 dB for the central channel even with a narrow channel spacing of 0.4 nm, thanks to the design of Euler-bend-assisted broadened arrayed waveguides and the introduction of SETRs. It is possible to further enhance the device

performance by improving the fabrication processes and introducing high-quality silicon-on-insulator wafers with extremely thickness uniformity.

4 Conclusion

In summary, we have reported the design and demonstration of a high-performance 32×32 silicon AWG with a very narrow channel spacing of 0.4 nm, which is suitable for DWDM systems. Especially, the use of Euler-bend-assisted broadened arrayed waveguides minimizes the phase errors and the power attenuation and it also improves the manufacturing simplicity. We have introduced the design of SETRs to mitigate the excess loss related to the mode mismatch between the FPR and the arrayed waveguides. For the fabricated AWG with a footprint of 900×2200 μm^2, the FSR is about 14.7 nm, covering the 32 channels with a spacing of 0.4 nm. For the central channel, the measured excess loss is as low as 0.65 dB and the channel non-uniformity is about 2.5 dB, while the inter-channel crosstalk is about −21.4 dB, which is impressive for the case with a channel spacing as narrow as 0.4 nm. The performance of the present AWG can be improved in potential by **improving the fabrication processes and introducing high-quality silicon-on-insulator wafers with extremely thickness uniformity**. The present high-performing AWGs with dense channel spacing will be useful in various optical systems of e.g., next-generation communication.

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