Effect of annealing temperature on interfacial and electrical performance of Au–Pt–Ti/HfAlO/InAlAs metal–oxide–semiconductor capacitor

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HfAlO/InAlAs metal–oxide–semiconductor capacitor (MOS capacitor) is considered as the most popular candidate of the isolated gate of InAs/AlSb high electron mobility transistor (HEMT). In order to improve the performance of the HfAlO/InAlAs MOS-capacitor, samples are annealed at different temperatures for investigating the HfAlO/InAlAs interfacial characyeristics and the device's electrical characteristics. We find that as annealing temperature increases from 280 °C to 480 °C, the surface roughness on the oxide layer is improved. A maximum equivalent dielectric constant of 8.47, a minimum equivalent oxide thickness of 5.53 nm, and a small threshold voltage of −1.05 V are detected when being annealed at 380 °C; furthermore, a low interfacial state density is yielded at 380 °C, and this can effectively reduce the device leakage current density to a significantly low value of 1×10^{-7} A/cm^2 at 3-V bias voltage. Therefore, we hold that 380 °C is the best compromised annealing temperature to ensure that the device performance is improved effectively. This study provides a reliable conceptual basis for preparing and applying HfAlO/InAlAs MOS-capacitor as the isolated gate on InAs/AlSb HEMT devices.

Keywords: HfAlO/InAlAs MOS-capacitor, annealing temperature, interface, leakage current

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1. Introduction

Compared with traditional high electron mobility transistor (HEMT) based on GaAs, InAs/AlSb HEMT has a high electron mobility and electron saturation drift speed in channel, which has a good application prospect in high speed, low power, and low noise circuits.[1–4] However, due to the type-II alignment energy band structure of InAs/AlSb heterojunction, and the lack of effective electron barrier layer from the InAs channel layer to the gate, electron transporting channels are generated, making the channel electrons easy to leak to the gate and form gate electron leakage current (Schottky leakage current), which is an intrinsic issue affecting the performance of InAs/AlSb HEMTs.[3,5] Especially, when the gate length decreases to a size of 0.18 μm or less, the present Schottky gate structure commonly used in InAs/AlSb HEMTs is much less effective in suppressing gate leakage current.[6,7] As reported, a high-*k* dielectric oxide layer deposited between the InAlAs protective layer and the gate metal can form a metal/high-*k*/InAlAs MOS-capacitor (metal–oxide–semiconductor capacitor), which can be used as an insulating gate structure to effectively suppress gate leakage.[7–9] Currently, Al_2O_3 and HfO_2 are the most commonly used high-*k* materials that are deposited on InAlAs.[10–12] In contrast, HfAlO presents a higher dielectric constant than Al_2O_3, which helps to form higher effective oxide thickness (EOT) under the same physical oxide thickness. Besides, compared with HfO_2, HfAlO has the low frequency dispersion and high thermal stability.[9,13,14] Therefore, HfAlO is considered as a candidate that can improve high-*k* dielectric on InAlAs for MOS capacitor isolated gate application.[15] In the preparation of HfAlO/InAlAs MOS-capacitor samples, annealing temperature markedly affects the oxide–semiconductor interface quality and the device performance.[16–19] Since the low crystallization temperature of InAlAs material is about 400 °C, the annealing temperature scheme of high-*k*/InAlAs process would be very different from other high-*k*/III–V processes, such as high-*k* on GaN, GaAs, and InAs.[20,21] In order to investigate the effects of annealing temperature on the interfacial and electrical characteristics of high-*k*/InAlAs/metal MOS-capacitor device for a better device performance, we prepare Au–Pt–Ti/HfAlO/InAlAs MOS-capacitor samples that are annealed at different temperatures of 280, 330, 380, 430, and 480 °C. The surface roughness of oxide layer is tested by atomic force microscope (AFM) and the chemical composition of the HfAlO/InAlAs interface is tested by x-ray photoelectron spectroscopy (XPS). Parameters such as EOT, the equivalent dielectric constants of the oxide layer (ε_{ox}), the values of threshold voltage (V_{th}), and the values of interfacial state density (D_{it}) of samples annealed at different temperatures are extracted and analyzed through capacitance–voltage (C–V) testing, and the leakage current of the samples are detected and compared. A better understanding of the interfacial characteristics and electrical properties of HfAlO/InAlAs MOS-capacitors at diverse annealing temperatures will help

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to determine the best annealing temperature in order to further improve the performance of the device.

2. Experiment and method

The structure diagram of the Au-Pt-Ti/HfAlO/InAlAs MOS capacitor is shown in Fig. 1(a). A 500-nm $In_{0.5}Al_{0.5}As$ layer was grown on a semi-isolated InP substrate by molecular beam epitaxy. The InAlAs surface was immersed in the 36%–38%-HCl solution for 1 min and 7%-$(NH_4)S$ solution for 15 min to remove native oxides and As–O compounds in sequence, then the films were dried in N_2 atmosphere. The InAlAs surface was characterized by atomic force microscopy (AFM) in the contact mode. Then we used the atomic layer deposition (ALD) process to deposit a 12-nm HfAlO layer on InAlAs as the oxide layer. The HfAlO deposition was realized by alternately growing HfO_2 and Al_2O_3 with ratio of 1 : 2, and the details of ALD process have been reported in our previous paper (see Ref. [9]) as shown below. For each cycle of HfO_2 deposition, we passed the precursor of Hf element as TEMAH for 1 s, then passed N_2 for 2 s in order to drive off the Hf-based residues, and passed the precursor of O element as H_2O for 1 s, finally passed N_2 for 2 s in order to deliver out total residues. For each cycle of Al_2O_3 deposition, we passed the precursor of Al element as TEM for 0.5 s, then passed N_2 for 2 s in order to transfer the Al-base residue out, then passed the precursor of O element as H_2O for 0.5 s, finally passed N_2 for 2 s in order to deliver out total residues. The oxide layers were then annealed in N_2 at temperatures of 280, 330, 380, 430, and 480 °C, respectively. The annealing process was that temperature rised from room temperature to the annealing temperature within 5 s, and then reached the preset annealing temperature in 60 s, with the temperature fluctuating in a range of ±2 °C; finally, the sample naturally cooled to room temperature from the annealing temperature within 300 s. After the oxide layer was annealed, a Ti/Pt/Au metal stack electrode was grown on the surface of the oxide layer. The area of the smallest electrode was 150 μm × 150 μm, and the area of the largest electrode was 100 times that of the smallest electrode. The equivalent circuit of this MOS structure is shown in Fig. 1(b).

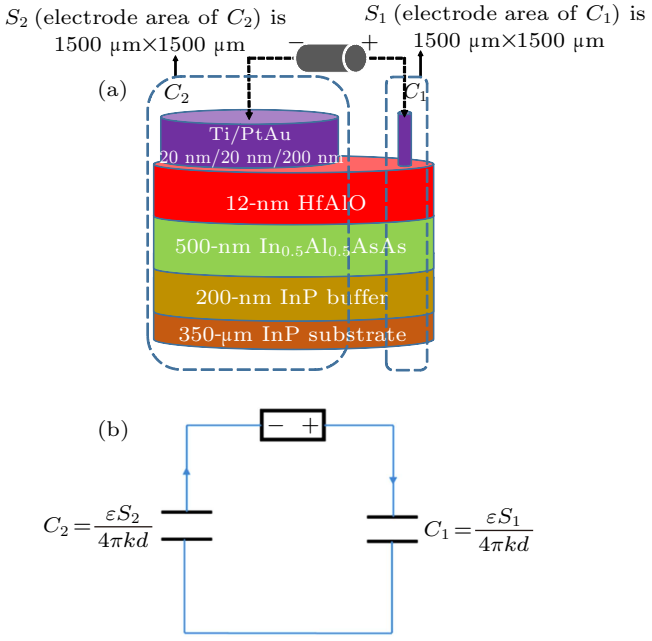

Fig. 1. (a) Structure diagram of MOS capacitor, and (b) equivalent circuit of the MOS capacitor.

The measured capacitance is approximately considered as the capacitor with small electrode (C_1) according to the following equation:

$$C = \frac{1}{1/C_3 + 1/C_2} = \frac{1}{4\pi kd/\varepsilon S_1 + 4\pi kd/\varepsilon S_2} \approx C_1, \quad (1)$$

where d is the thickness of layer, k is Boltzmann constant, and ε is the oxide dielectric constant. This layout is advantageous for applying a high gate voltage to the small electrode for high precision C–V measurements.[9,22] The photograph of electrode is shown in Fig. 2.

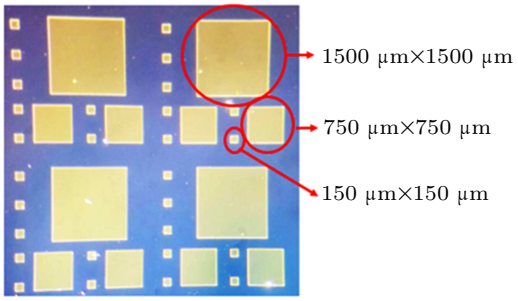

Fig. 2. Photograph of Ti/Pt/Au metal electrode.

3. Results and discussion

In order to analyze the effects of annealing temperature on the HfAlO/InAlAs interfacial and the device's electrical characteristics of the Au–Pt–Ti/HfAlO/InAlAs MOS capacitor, the detailed discussion is carried out based on the AFM, x-ray photoelectron spectroscopy (XPS), capacitance (C)–voltage (V) test, and leakage current results.

3.1. AFM

The AFM (equipment information: Bruker, Dimension Icon) test is applied to oxide surface with an area of 5 μm×5 μm. The AFM images of the samples are shown in Fig. 3, and the root-mean-square (RMS) values of the surface roughness of the samples are illustrated in Fig. 4. It is find that the RMS roughness decreases as annealing temperature increases. This indicates that the higher annealing temperature is crucial to the improvement of the compactness and homogeneity of oxide–semiconductor interface and oxide layer, leading the oxide surface to lower roughness. The oxide layer with less surface roughness can better combine with the metal to reduce the leakage channel in the metal, thus effectively restraining the leakage current.

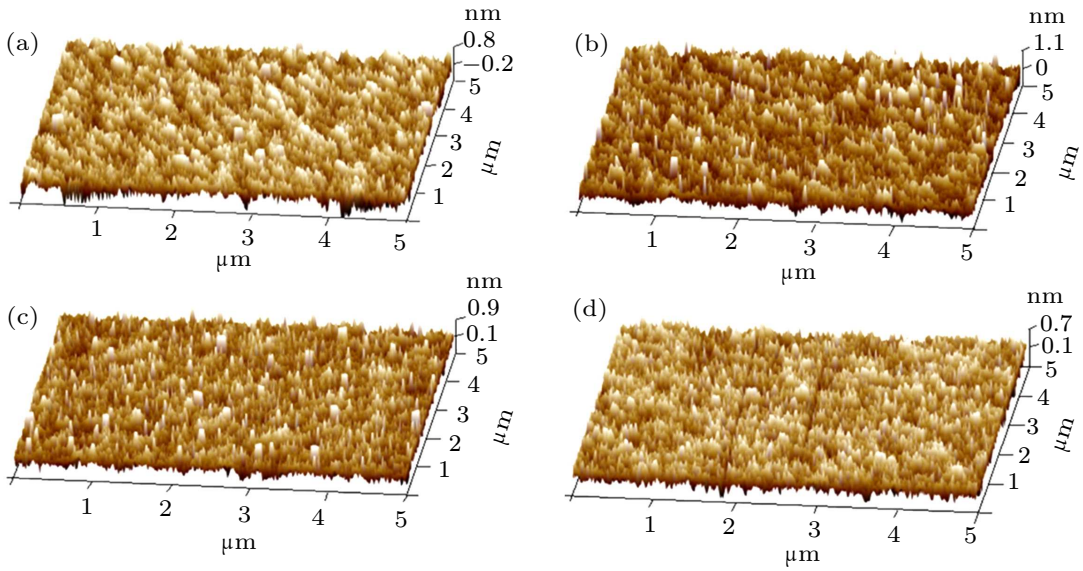

Fig. 3. AFM line scan of HfAlO/InAlAs surfaces of samples annealed at (a) 330 °C, (b) 380 °C, (c) 430 °C, and (d) 480 °C.

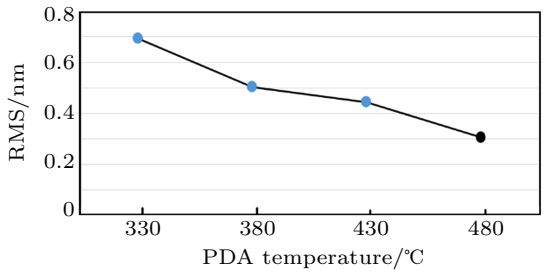

Fig. 4. RMS roughness value *versus* PDA temperature of the samples.

3.2. XPS

An Ar ion beam sputter source is used in the XPS system with a beam current density of 1.067×10^{-5} A/cm^2 under 1.2×10^4 V.

Figure 6 shows the XPS results of the samples annealed in different temperatures after 30-s etching (an etching time of 30 s corresponds to a depth of oxide layer of approximately 6 nm). The dry etching with physical spurring method is adopted to avoid any influence on the element composition of the interface under examination. As the annealing temperature increases, the As_{3d} peak moves toward higher binding energy [Fig. 5(a)] since the HfAl–O chemical bond becomes easier to break and then combine with As to form an As–O compound as the annealing temperature rises. As–O compounds degrade the interface quality by increasing the additional interface states. The Hf_{4f} energy spectra at different annealing temperatures are shown in Fig. 5(b). The Hf_{4f} peaks of the samples move toward low binding energy with annealing temperature rising. This indicates that the HfO_2 content increases and HfAlO content decreases as the annealing temperature goes up. (The Hf binding energy of HfO2 is assigned as a value of 17.2 eV lower than that of HfAlO (18.4 eV[23])). This can be explained by that Hf–Al–O bond is stable at low annealing temperatures; however, as the annealing temperature increases, the Hf–Al–O bond absorbs enough energy to break, and the atomic thermal motion in the oxide layer becomes more intense, thus, the probability of oxygen atoms combining with the Hf atom to form HfO_2 increases and the HfO_2 content augments. The HfO_2 is less dense than HfAlO, resulting in elements easily entering from the semiconductor layer into the oxide layer, at the sacrifice of the overall quality of the oxide layer. The Al_{2p} energy spectra are shown in Fig. 5(c). The Al_{2p} energy spectrum also exhibits the same trend as the Hf_{4f} energy spectrum. As the annealing temperature increases, the Al_{2p} peak shifts toward low binding energy, owing to bonding with oxygen atoms by Al atoms in the oxide layer to form Al–O compounds. As shown in Fig. 5(d), the In_{3d} concentrations of the sample at different annealing temperatures are very small which can be neglected. It indicates that In element has a weak diffusivity in the HfAlO, and the annealing temperature has little effect on it. The interface between the oxide and semiconductor layer is exposed when the oxide layer was etched for 60 s by the spurring method. We fit the peaks of the O_{1s} spectrum to analyze the interfacial characteristics of HfAlO/InAlAs. To highlight the differences between samples at different annealing temperatures, we only consider the samples annealed, respectively, at 280, 380, and 480 °C. The content values of different oxides by peak fitting results with Advantage software are shown in Fig. 6. The content of interfacial impurities increases obviously as the annealing temperature reaches 480 °C, while the rise of the interfacial impurity content (*e.g.*, As–O, In–O, and Al–O) is not obvious below 380 °C. By analyzing the XPS results of the five samples, it is found that selecting a lower annealing temperature is preferable for suppressing the impurity content inside the oxide layer and improving the interface quality of HfAlO/InAlAs MOS-capacitors.

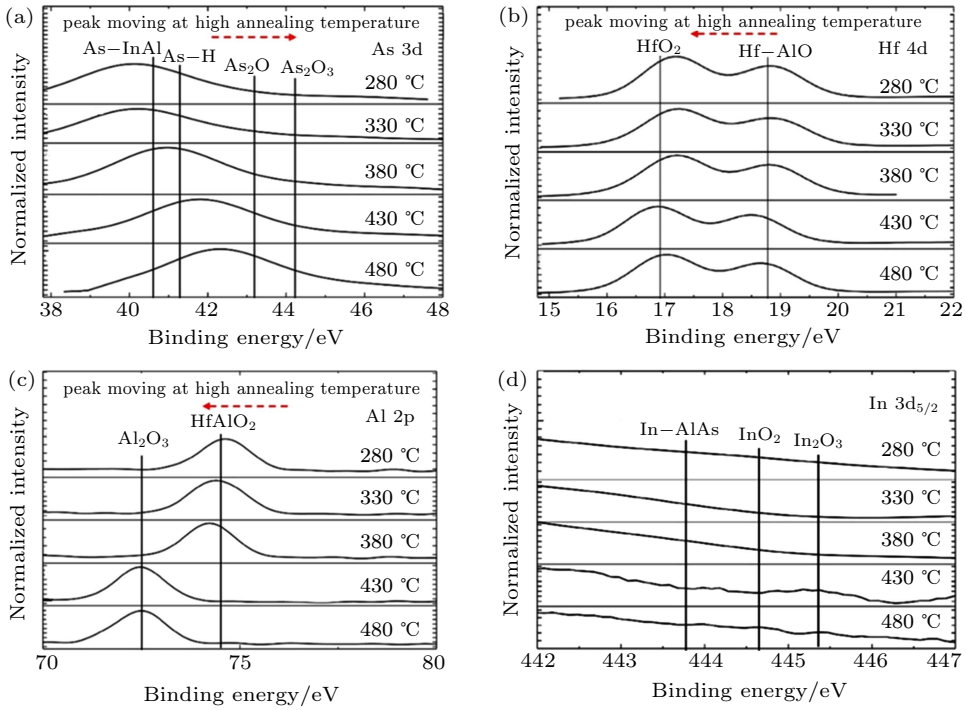

Fig. 5. XPS results after annealing processing of (a) As 3d, (b) Hf 4f, (c) Al 2p, (d) In $3d_{2/5}$.

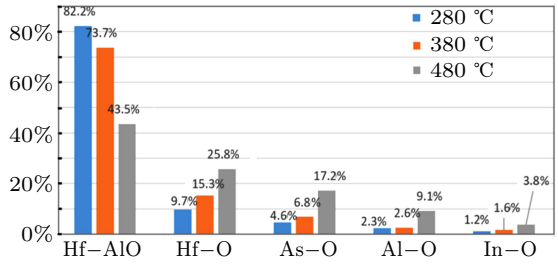

Fig. 6. Interfacial oxide content under annealing temperatures of 280, 380, and 480 °C.

3.3. *C–V* TEST

High-frequency capacitance (*C*)–voltage (*V*) testing of the HfAlO/InAlAs structure is carried out with Agilent B1500 equipment at 1 MHz. As shown in Fig. 7, for the samples annealed at 280, 330, and 380 °C, the accumulation capacitance (C_{ox}) increases as the annealing temperature rises, showing an upward trend due to a higher annealing temperature is helpful in suppressing the formation of traps in oxide layer. However, an obvious accumulation zone cannot be observed in the *C–V* curves as the annealing temperature gradually increases to 430 °C and 480 °C, which is due to the fact that some oxide impurities (*e.g.*, As–O, In–O, and Al–O) are formed in the oxide layer when the annealing temperature exceeds 380 °C, and it seriously degrades the interface quality and leads to a large leakage current. The leakage makes the charges under the oxide layer constantly change, resulting in a change of capacitance value. Thus, an accumulation region cannot form. This result indicates that a certain increase of annealing temperature can improve the capacitor performance. However, excessive temperature over 380 °C is not of benefit to the device performance.

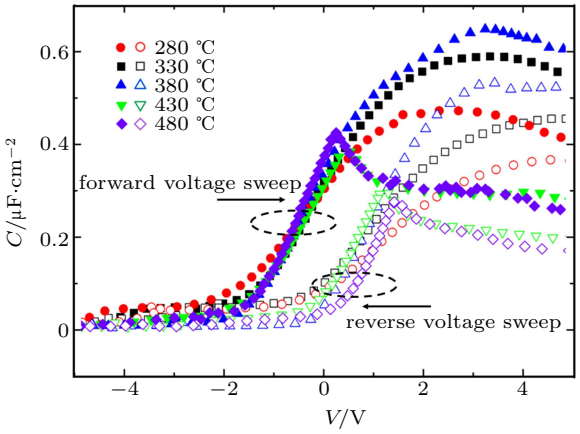

Fig. 7. The *C–V* characteristics of HfAlO/InAlAs MOS-capacitor at different annealing temperatures.

The EOT, ε_{ox}, and V_{th} of the HfAlO/InAlAs MOS-capacitor are extracted[10,24,25] as given in Table 1. The EOT decreases with annealing temperature going up from 280 °C to 380 °C, and then increases as the annealing temperature gradually increases from 380 °C to 480 °C. The sample with an annealing temperature of 380 °C has the smallest EOT (5.53 nm) and its ε_{ox} is the largest (8.47). Thus, when the equivalent oxide layer thickness is uniform, the sample with 380 °C annealing process allows a larger physical thickness of the oxide layer, which can better suppress the gate leakage current. The flat band capacitance (C_{FB}) shows the same trend as the ε_{ox}, and its maximum value is achieved when annealing temperature is 380 °C. The V_{th} is extracted by the method given in

Ref. [20]. It is found that the sample under annealing temperature of 380 °C indicates a low V_{th} of −1.05 V. A reduction of V_{th} is of benefit to reducing the power consumption of the device. It is noted that when the annealing temperature is raised to 430 °C, the extraction error of V_{th} is large due to the deterioration of the *C*–*V* curve. By analyzing the parameters of EOT, V_{th} and other parameters, selecting the 380-°C annealing process can be helpful in reducing the leakage current and the device power consumption.

The electrical parameters extracted from the *C*–*V* measurements for HfAlO/InAlAs MOS-capacitor with different annealing temperatures are shown in Table 1.

Table 1. Electrical parameters extracted from *C*–*V* measurements for HfAlO/InAlAs MOS-capacitor with different annealing temperatures.

Annealing temperature/℃	C_{ox}/(μF/cm^2)	EOT/nm	ε_{ox}	C_{FB}/(μF/cm^2)	V_{FB}/V	V_{th}/V
280	0.34	7.30	6.41	0.31	0.01	1.33
330	0.47	5.85	8.00	0.36	0.23	0.97
380	0.59	5.53	8.47	0.37	0.12	1.05
430	0.63	8.92	5.24	0.27	0.21	1.70
480	0.39	8.11	5.77	0.29	0.34	1.76

We analyze the interfacial trap density (D_{it}) results according to the Terman method from *C*–*V* test result.[26] Here, we use three typical temperatures: 280 °C, 380 °C, and 480 °C to investigate the influence of difference in annealing temperature. The values of D_{it} are obtained as shown in Fig. 8. The D_{it} value is lowest for the sample annealed at 380 °C. This is basically consistent with the XPS results we analyzed above. The sample annealed at 380 °C has fewer oxygen vacancies and other defects on the HfAlO–InAlAs interface. Thus, the sample annealed at 380 °C presents lower interfacial states. While, some elements such as Al and As are easier to combine with vacancy oxygen and other dangling bonds to form interface states for the sample annealed at 480 °C, thus it shows the highest D_{it} value. It is noted that since there is no obvious accumulation region on the *C*–*V* curve of the sample annealing at 480 °C, the D_{it} extraction under this condition is not accurate and is only used as an analysis reference. Especially, the application on high-*k*/InAlAs interface is tricky because of the Fermi level pinning effect caused by the high interfacial state density. The method to suppress the Fermi level pinning effect will be discussed in our next research.

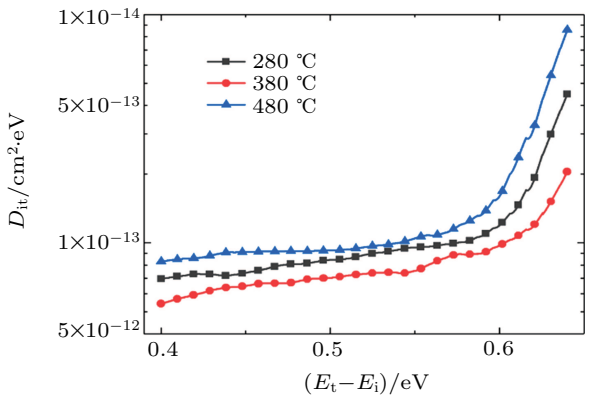

Fig. 8. Interfacial state density (D_{it}) of HfAlO/InAlAs MOS-capacitor with different annealing temperatures. ($E_t - E_i$) indicates the distance from energy level of interface trap state (E_t) to intrinsic Fermi level (E_i).

3.4. Leakage current

Figure 9 shows the leakage current densities of the HfAlO/InAlAs MOS-capacitor at different annealing temperatures. Because the leakage current is mainly contributed from the defects or oxygen vacancies near HfAlO/InAlAs interface, the sample with 380 °C presents the lowest leakage current which is consistent with the above results of D_{it}. Especially, the leakage current density is significantly low, specifically, it is 1×10^{-7} A/cm^2 at 3-V bias voltage under annealing temperature of 380 °C, and it is one order of magnitude lower than under annealing temperatures of 280 °C and 480 °C. Furthermore, it is a very low value of leakage current density and is well compared with the values of the existing reports of high-*k*/InAlAs MOS capacitors in Refs. [9,12,15,22].

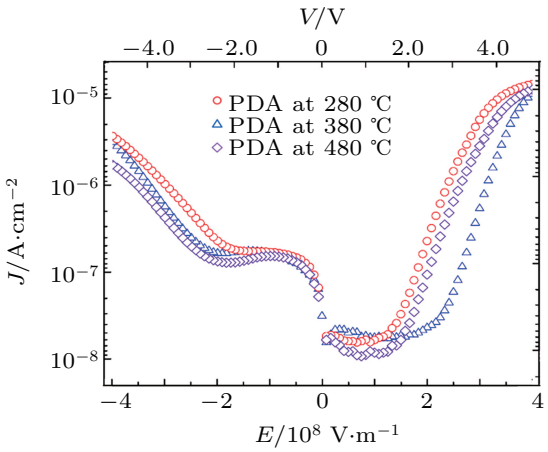

Fig. 9. Leakage current densities of HfAlO/InAlAs MOS-capacitor at different annealing temperatures.

4. Conclusions

In this paper, the effects of postdeposition annealing temperature on the interface and electrical properties of HfAlO/InAlAs MOS-capacitors are investigated in detail. Our experimental results illustrate that as annealing temperature

increases from 280 °C to 480 °C, the oxide layer surface roughness is improved; however, the diffusion of impurity particles inside the oxide layer increases. The HfAlO/InAlAs MOS-capacitor annealed at 380 °C has small values of EOT and V_{th}; furthermore, the device annealed at 380 °C presents a low D_{it} which can drastically reduce the leakage current density down to a significantly value of 1×10^{-7} A/cm^2 at 3-V bias voltage. Therefore, by making a compromise among the oxide surface roughness, the oxide layer, the interface layer quality, and the electrical performances, we adopt 380 °C as the best annealing temperature to make the device performance meet the demands. This study provides a reliable conceptual basis for preparing and applying the InAs/AlSb HEMT devices.

References

[1] Moschetti G, Wadefalk N and Nilsson P A 2011 *Solid State Electron.* **64** 47
[2] Haddadi A, Chevallier R and Dehzangi A 2017 *Appl. Phys. Lett.* **110** 101
[3] Guan H, Lv H L, Guo H and Zhang Y M 2015 *J. Appl. Phys.* **118** 195702
[4] Malmkvist M, Lefebvre E, Borg M, Desplanque L, Wallart X and Dambrine G 2018 *IEEE Trans. Microwave Theory & Tech.* **56** 2685
[5] Guan H and Guo H 2017 *Chin. Phys. B* **26** 058501
[6] Moschetti G, Wadefalk N and Nilsson P A 2012 *IEEE Microwave & Wireless Compon. Lett.* **22** 144
[7] Cui X R and Lv H L 2018 *J. Infrared & Millimeter Waves* **37** 385
[8] Hashizume T, Ootomo S and Inagaki T 2003 *J. Vac. Sci. Technol. B* **21** 1828
[9] Guan H and Lv H L 2018 *Thin Solid Film* **661** 137
[10] Wu L F, Zhang Y M and Lv H L 2015 *Jpn. J. Appl. Phys.* **54** 110303
[11] Liu L N, Choi H W, Xu J P and Tang W M 2007 *IEEE Trans. Electron Dev.* **65** 72
[12] Jin C J, Lv H L, Zhang Y M and Guan H 2016 *Thin Solid Films* **619** 48
[13] Mikhelashvili V, Meyler B and Shneider J 2005 *Microelectron. Reliab.* **45** 933
[14] Gao J, He G and Liu M 2017 *J. Alloys Compd.* **691** 504
[15] Jin C J, Lv H L, Zhang Y M and Guan H 2016 *Solid-State Electron.* **123** 106
[16] Lin Y C, Trinh H D and Chuang T W 2013 *IEEE Electron Dev. Lett.* **34** 1229
[17] Trinh H, Lin Y, Wang H, Chang C, Kakushima K and Iwai H 2012 *Appl. Phys. Express* **5** 1104
[18] Altuntas H, Donmez I, Ozgit-Akgun C and Biyikli N 2014 *J. Vac. Sci. Technol. A* **32** 041504
[19] Liu C, Zhang Y M, Zhang Y M and Lv H L 2014 *J. Appl. Phys.* **116** 142101
[20] Maleev N A, Bobrov M A, Kuzmenkov A G, Vasil'Ev A P and Kulagina M M 2018 *Tech. Phys. Lett.* **44** 862
[21] Asif M, Chen C, Peng D, Xi W and Zhi J 2018 *Solid State Electron.* **142** 36
[22] Guan H and Jing C Y 2018 *Coating* **8** 417
[23] Brennan B, Galatage R V and Thomas K 2013 *J. Appl. Phys.* **114** 317
[24] Inci D, Cagla O and Necmi B 2013 *J. Vac. Sci. Technol. A* **31** 01A110
[25] Guan H, Lv H L, Guo H, Zhang Y M, Zhang Y M and Wu L F 2015 *Chin. Phys. B* **24** 126701
[26] Terman L M 1962 *Solid State Electron.* **5** 285