A high performance fast-Fourier-transform spectrum analyzer for measuring spin noise spectrums*

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A high performance fast-Fourier-transform (FFT) spectrum analyzer, which is developed for measure spin noise spectrums, is presented in this paper. The analyzer is implemented with a field-programmable-gate-arrays (FPGA) chip for data and command management. An analog-to-digital-convertor chip is integrated for analog signal acquisition. In order to meet the various requirements of measuring different types of spin noise spectrums, multiple operating modes are designed and realized using the reprogrammable FPGA logic resources. The FFT function is fully managed by the programmable resource inside the FPGA chip. A 1 GSa/s sampling rate and a 100 percent data coverage ratio with non-dead-time are obtained. 30534 FFT spectrums can be acquired per second, and the spectrums can be on-board accumulated and averaged. Digital filters, multi-stage reconfigurable data reconstruction modules, and frequency down conversion modules are also implemented in the FPGA to provide flexible real-time data processing capacity, thus the noise floor and signals aliasing can be suppressed effectively. An efficiency comparison between the FPGA-based FFT spectrum analyzer and the software-based FFT is demonstrated, and the high performance FFT spectrum analyzer has a significant advantage in obtaining high resolution spin noise spectrums with enhanced efficiency.

Keywords: fast Fourier transform, spectrum analyzer, field-programmable-gate-arrays (FPGA), spin noise spectrum

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1. Motivation

Measuring the spin noise spectrum plays an important role in studying the valuable information of the systems including spin dynamics and magnetic resonance.[1–4] Random fluctuations of N spins should statistically generate measurable noises of order $\sqrt{N}$ spins, and the spin noise signals can be measured by obtaining the spectrums. The commercial spectrum analyzers can be applied to obtain the spin noise spectrums,[5–9] whereas it requires a long experimental time to achieve a favorable signal-to-noise-ratio (SNR) due to the limited efficiency contributed by the spectrum analyzers. Therefore the implementation of high efficiency spectral analysis equipment will be meaningful to the study of spin noise spectrums.

The recent development of the analog-to-digital-converters (ADC) and digital processing techniques gives a great opportunity to improve the efficiency of spectral estimation.[10,11] The fast-Fourier-transform (FFT) method is recognized as a practical solution to analyzing the signal spectrums,[12–15] with reduced complexity and a shortened processing delay. FFT functions developed with customized software can be used to study the spin noise spectroscopy.[16] The efficiency and the effectiveness of the software-based FFT function are limited by the serial computation mode of the software and by the memory capacity of the computer. In order to obtain an improved experimental efficiency, data-acquisition (DAQ) boards, which utilized field-programmable-gate-arrays (FPGA) chips to realize real-time FFT functions, were applied to measure the spin noise spectrums.[17,18] Due to the principle of the FFT method, there is a tradeoff between bandwidth and frequency resolution when implementing real-time FFT modules. Down-sampling is helpful to improve the spectrum frequency resolution whereas the bandwidth is decreased accordingly. The mixture signals will become indistinguishable due to the signal aliasing effect caused by the insufficient bandwidth in spectrum measurement. Thus, there are technical difficulties to study the spin noise spectroscopy with high frequency resolution. Even though there exist various types of FPGA-based spectrum analyzers,[19–21] all of them suffer from such limitations.

In this paper, we report the implementation and the char-

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acterization of a high performance FFT spectrum analyzer. The spectrum analyzer has a 1 GSa/s data acquisition sampling rate and a 12-bit amplitude resolution. A Xilinx Virtex-7 FPGA is used to manage data flow and to perform the FFT operation. Customized operating modes are designed to achieve a full-featured measurement for the spin noise spectrums. The spin noise spectrums with various frequency components can be measured precisely using the FFT spectrum analyzer. Reconfigurable digital filters and frequency down converters are implemented in the FPGA, thus the signal aliasing and noise floor can be suppressed and the SNR can be improved. The spectrum analyzer provides a considerable capacity and flexibility in measuring different types of spin noise spectrums.

2. Architecture and principle

2.1. Hardware architecture

The architecture of the high performance FFT spectrum analyzer is shown in Fig. 1. The board is implemented using a Xilinx Virtex-7 FPGA, which manages the data flow and the digital data processing functions. An ADC chip ADC12D1000, which has a 1 GSa/s sampling rate and a 12-bit amplitude resolution, is integrated to record the input spin noise signals from the experimental platform. In order to realize a 100 percent real-time data utilization ratio for the 1 GSa/s data flow, four parallel digital FFT modules which operate with a 250 MHz clock are implemented inside the FPGA. The external Double-DataRate-III (DDR3) memory is used to provide sufficient on-board data storage capacity. The accumulation module, which is used to calculate the average values of the frequency spectrum output from the FFT modules, is also realized in the FPGA. The FFT modules have a processing ability of 32768 input samples for a single operation. The capacity of the input samples for a single FFT operation is limited by the maximum number of the digital-signal-processors (DSP) and the block random-access-memory (BRAM) resources inside the FPGA chip. The output data from the FFT spectrum analyzer are transmitted to the host computer through a highspeed universal serial bus (USB) port.

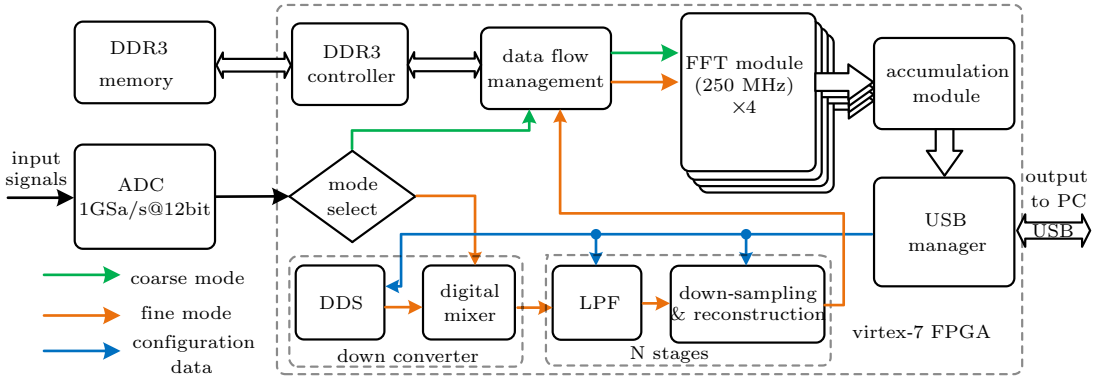

Fig. 1. The architecture of the high performance FFT spectrum analyzer. Two optional operating modes are designed using the reconfigurable FPGA resources.

The FFT DAQ board has two different operating modes, which are named "coarse mode" and "fine mode". In the coarse mode, the data acquired from the ADC chip are handled directly by the FFT module to achieve a coarse scanning, and an $F/32768$ frequency resolution with a DC-$F/2$ bandwidth can be obtained, where F is the sampling rate of the input data. In the fine mode, the input signals are filtered and reconstructed to achieve an enhanced frequency resolution and an improved SNR. The signals are firstly managed by the direct-digital-synthesizer (DDS) and the digital mixer to realize a frequency down conversion. The output frequency of the DDS module is reconfigurable, and it can be determined by the target frequency obtained according to the test results measured using the coarse mode. Thus the target frequency components with arbitrary frequencies can be studied in a low frequency region. The output digital signals from the mixer are processed by the low-pass-filter (LPF) to suppress the noise and the aliasing, and a multi-stage data reconstruction module is used to re-organize the data flow. N ($N = 1,2,3,4,\ldots,8$) stages of LPF and data reconstruction modules are implemented. The N^{th} stage LPF has a passband of DC-$500/2^N$ MHz, and each reconstruction module divides the sampling rate in half. Therefore the bandwidth of the FFT spectrum is reduced to $500/2^N$ MHz, and 2^N arrays of $10^9/2^N$ Sa/s sampling points can be regenerated after the N-stage data reconstruction. The signal aliasing and the noise floor superposition contributed by down sampling can be suppressed by the multi-stage LPFs. The parameters of the LPF and the number of the reconstruction stages N are reconfigurable, and both of them can be reloaded via the universal-serial-bus (USB) port. The re-constructed data are processed by the FFT modules, and the frequency resolution is $10^9/(2^N \times 32768)$ Hz whereas the bandwidth is $500/2^N$ MHz, and the operating efficiency can be improved by 2^N times comparing to the general

FFT DAQ techniques which have a sampling rate of $10^9/2^N$ Sa/s. The output frequency of the DDS module, the number of the LPFs and down-sampling stages are configurable, thus the spin noise spectrums with a bandwidth of DC-500 MHz can be measured with adjustable frequency resolution.

2.2. Down-sampling and data reconstruction

The customized multi-stage reconstruction module is integrated inside the FPGA to achieve a high frequency resolution FFT operation with a retained high efficiency. The principle of realizing hardware acceleration is shown in Fig. 2. The raw input data can be considered as a one-dimension matrix, which has a length of $M \times 2^N$ ($M = 32768$). Each reconstruction stage operates with a decimation factor of 2, and the length of each data array is reduced by half whereas the number of the matrix columns is doubled. After N times of down-sampling and reconstruction, the input data is transformed into an $M \times 2^N$ matrix. The data stored in each column of the matrix are managed in sequence by the FFT module, and the output frequency resolution equals $10^9/(2^N \times 32768)$ Hz. Even though the data sampling rate is reduced to $10^9/2^N$, a 100 percent data utilization rate for the 1 GSa/s input data can be retained, thus the operating efficiency can be enhanced by 2^N times comparing to a general FFT spectrum analyzer. After a 2^N times averaging, the SNR of the FFT spectrums can be improved by $\sqrt{2^N}$ theoretically.

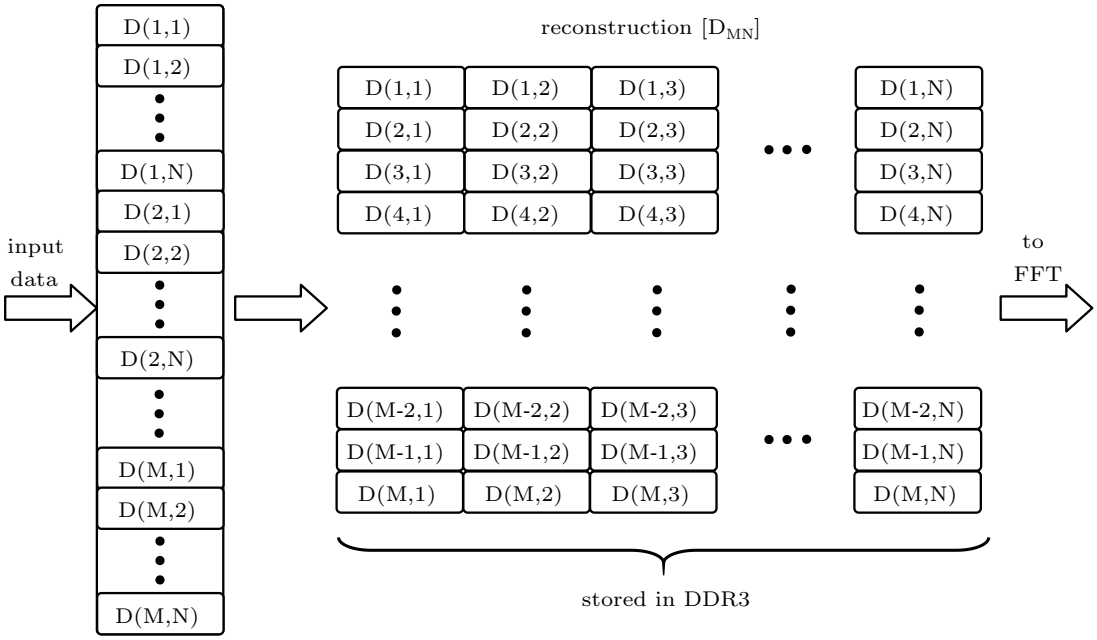

Fig. 2. The block diagram of the down-sampling and reconstruction module. The input data are reconstructed by using N stages of data down-sampling and reconstruction, and the digital data after reconstruction are processed by the FFT module.

2.3. Aliasing suppression

As mentioned above, the signal aliasing in the FFT spectrum can be suppressed when performing spin noise measurement using the FFT spectrum analyzer, and the principle of aliasing suppression is shown in Fig. 3. The spectrograms in Figs. 3(a)–3(c) demonstrate that down-sampling without filters produces signal aliasing. Reducing the sampling rate by half contributes to the decrement of the bandwidth, and the frequency components of the out-of-band signals shift to the 1st Nyquist zone following the Nyquist sampling theorem.[22,23] After the 1/2 and the 1/4 down-sampling, the frequency components f_2 and f_3 shift and exist nearby the principal component f_1, and the aliasing makes it difficult to distinguish the target component f_1. Figures 3(d)–3(f) show that an LPF is implemented before each stage of down-sampling, and the passband of the filter equals half of the current bandwidth. The out-of-band signals can be eliminated before down-sampling thus the signals aliasing can be suppressed.

2.4. Software

Customized software has been developed to handle the FFT spectrum analyzer. The software is written using python and its block diagram is presented in Fig. 4. The design of the configuration parameters for the spectrum analyzer, data processing, bus management, as well as the graphics functions are fully managed by the software. The user-defined operations can be performed through the user interface. The configurable LPF parameters, the output frequency of the DDS module, the number of LPF, and down-sampling stages can be defined according to users' requirements. The graphical tools can be used to plot the curves of the FFT spectrums and the frequency response characteristics. The math tools are designed to provide an off-line arithmetical operation that can be defined by users. The configuration data encoding and the data flow analysis are managed by the application layer. The physical layer connects the spectrum analyzer and the host computer via a USB bus.

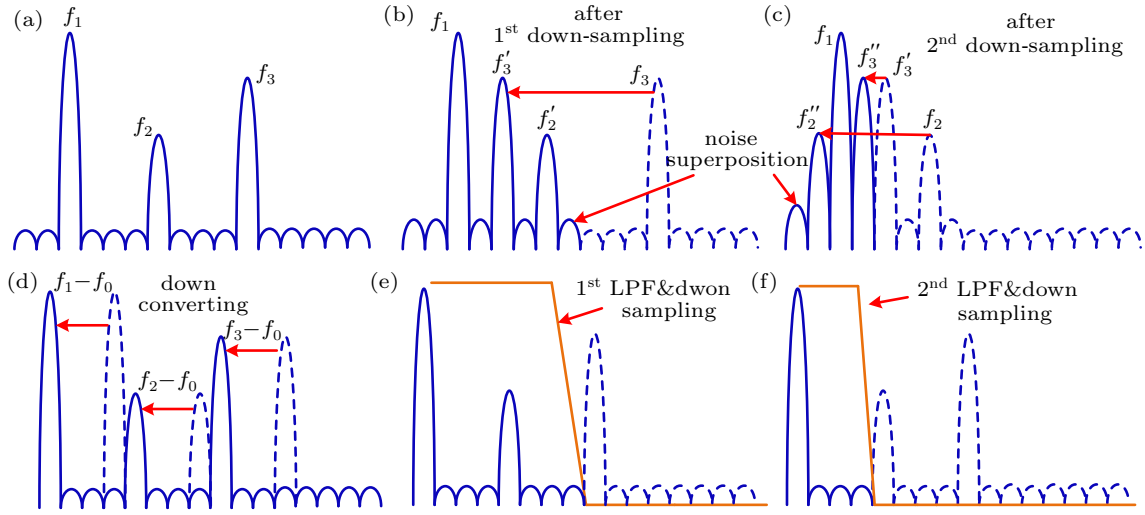

Fig. 3. The frequency spectrums before and after down-sampling and filtering. (a)–(c) The produced signal aliasing when performing down-sampling. (d)–(f) The signal aliasing suppressed effectively by the implementation of the multi-stage filters.

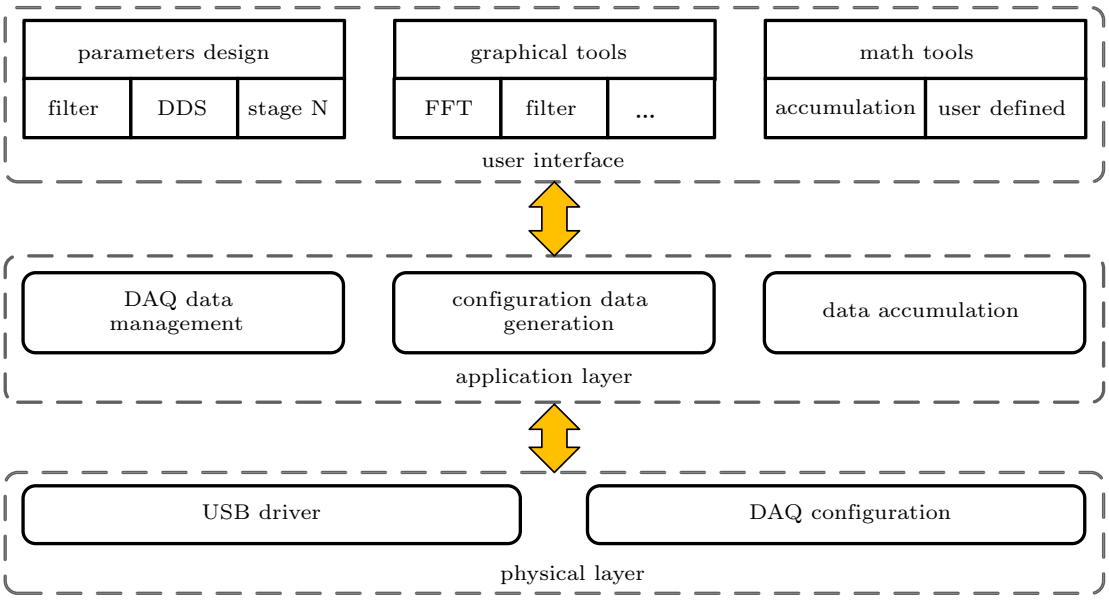

Fig. 4. Block diagram of customized software for the FFT spectrum analyzer.

3. Performance characterization

3.1. Broadband measurements for spin noise spectrums

The FFT spectrum analyzer is applied to measure the spin noise signals from alkali metal Rb,[24,25] and the test results are shown in Fig. 5. The spin noise spectrums are measured within a time span of 64 seconds. The test results obtained using the coarse mode are shown in Fig. 5(a). Decreasing the sampling rate of the input data can increase the frequency resolution of the spectrums, whereas the noise floor is raised due to the superposition of the frequency components. The spin noise signals from Rb are submersed in the noise background when the sampling rate is lower than $10^9/32$ Sa/s. Data reconstruction can be applied to achieve a 100 percent data utilization rate, and the 64×12 Gigabits input data can be fully processed after applying the multi-stage data reconstruction module, thus the SNR of the spectrums can be improved accordingly. As shown in Fig. 5(b), an improved SNR is obtained using the multi-stage data reconstruction module, and the submersed signals measured with the $10^9/32$ Sa/s sampling rate can be located. Figure 5(c) shows that the SNR can be further improved after applying the fine mode. In the fine mode, the input data are firstly managed by the down converting module, and a 5.8 MHz frequency shift is performed to move the frequency component to low frequency region. The output data from the down converting module are processed successively by the multi-stage digital filters, the multi-stage data reconstruction module, and the FFT module to obtain a low noise frequency spectrum. All the digital processing operation are real-time performed within 64 seconds.

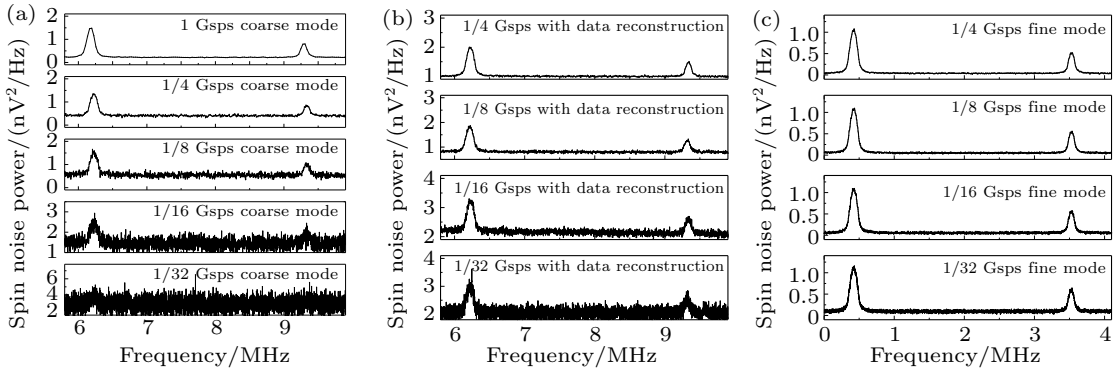

Fig. 5. Spin noise measurements for alkali metal Rb. (a)–(c) FFT spectrums measured with coarse mode, data reconstruction, and fine mode, respectively. In the fine mode, the input data are processed successively by the down converting module, the multi-stage digital filters, the multi-stage data reconstruction module, and the FFT module.

3.2. Signal-to-noise-ratio

Figure 6 demonstrates the relationship between the SNR and the measurement time span of the spin noise spectrums, and the test results for the isotopes ^{85}Rb and ^{87}Rb are plotted respectively. Figures 6(a) and 6(b) show the plots for the SNR obtained with a 1/4 GSa/s sampling rate, and the value of SNR rises when the accumulation time increases. The signal SNR from ^{85}Rb is superior to that from ^{87}Rb due to the difference in signal intensity. The SNR plots obtained with a 1/16 GSa/s sampling rate are shown in Figs. 6(c) and 6(d), and the value of the SNR decreases due to noise superposition. Figures 6(e) and 6(f) show the SNR measured when the sampling rate equals 1/256 GSa/s, and the spin noise spectrums can only be acquired when the fine mode is applied. The test results prove the advantage of the FFT spectrum analyzer in measuring high frequency resolution spin noise spectrums.

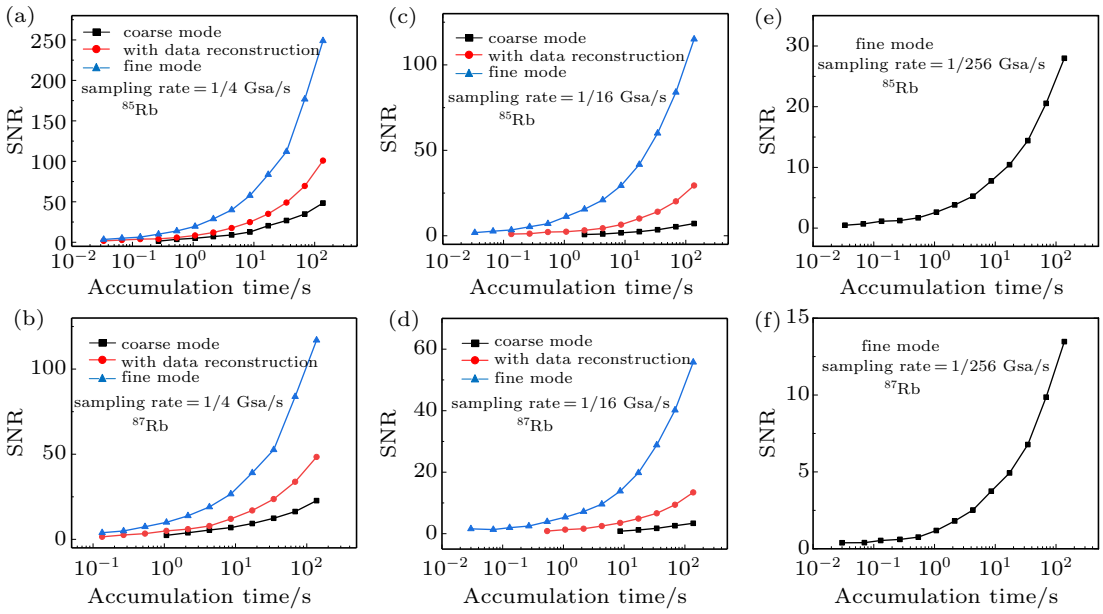

Fig. 6. The plots of the signal-to-noise-ratio versus the time span of spin noise measurements: (a) and (b) with a 1/4 GSa/s sampling rate, (c) and (d) with a 1/16 GSa/s sampling rate, (e) and (f) with a 1/256 GSa/s sampling rate.

3.3. Measuring mixed signals with different frequencies

In order to demonstrate the performance in distinguishing signals with adjacent frequencies, an arbitrary waveform generator[26] (AWG) which has a 1 GSa/s sampling rate and a 16-bit amplitude resolution is applied to generate mixed signals with adjacent frequencies, and the signals are measured by the FFT spectrum analyzer. The output signals from the AWG consist of six frequency components: 8.747 MHz, 8.748 MHz, 8.749 MHz, 39.999 MHz, 40 MHz, and 40.001 MHz. The test results for measuring mixed signals are shown in Fig. 7. As mentioned above, 32768 sampling points are processed within a single FFT operation, thus the frequency resolution equals 30.5 kHz when the sampling rate is 1 GSa/s. Figure 7(a) shows that the adjacent frequency components cannot be distinguished with the 1 GSa/s coarse mode. The FFT spectrum has two peaks at around 8.7 MHz and 40 MHz. Figure 7(b) shows decreasing the sampling rate can improve the frequency resolution, whereas the spectrum is aliasing when the sampling rate is 1/32 GSa/s and 1/256 GSa/s with the coarse mode. The frequency components in the mixed signals can be distinguished effectively by using the fine mode.

As shown in Fig. 7(c), the input signals are processed by the frequency down converter to achieve a frequency shift of 8.25 MHz and 39.5 MHz separately, and the digital filter is used to suppress the signal aliasing. The six frequency components are finally distinguished with a 1/256 GSa/s sampling rate, which contributes to a 119 Hz frequency resolution.

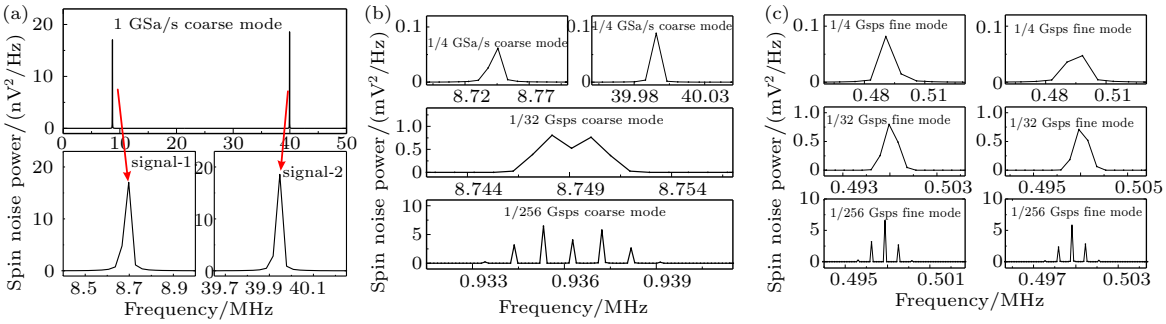

Fig. 7. The test results of measuring mixed signals with different frequency components. Utilizing the high performance FFT spectrum analyzer to obtain the FFT spectrums, the mixed signals can be measured with a high frequency resolution, and the signals aliasing can be suppressed.

4. Discussion

4.1. Digital filters

The multi-stage digital low-pass filters implemented with the FPGA logic resources are used to suppress the signal aliasing and the noise floor. Utilizing a single high-order low-pass filter located before the down sampling module can also suppress the non-target signals and the noise, whereas such a solution will occupy a large amount of FPGA logic resources. Figure 8 shows a comparison of response characteristics between a 30-order filter at the sampling rate of 1/256 GSa/s and a 240-order filter at 1 GSa/s high sampling rate. Both of the two filters have a cut-off frequency of 2 MHz and a transition band from 1.2 MHz to 2 MHz. A single 30-order filter occupies 60 digital signal processor (DSP) units inside the FPGA. Therefore 480 DSP units are required to realize the design, which has an eight-stage 30-order filter. The implementation of the 240-order filter at 1 GSa/s also occupies 480 DSP units. The 30-order filter at the low sampling rate can provide a 60 dB out-of-band rejection ratio, whereas the out-of-band rejection ratio is lower than 20 dB for the 240-order filter which operates at the high sampling rate. In order to achieve a 60 dB out-of-band rejection ratio with an LPF operating at 1 GSa/s, 15360 DSP units are required, whereas only 2800 DSP units are integrated into a single Virtex-7 FPGA chip. Hence, implementing multistage filters is a more effective solution to suppress the noise floor and the signal aliasing in the spin noise spectrums.

4.2. Down conversion

The frequency down converter is utilized to shift the frequency component of the target signals to low frequency region, and the signals can be further managed by the LPFs to suppress the non-target signals and noise. The output digital signal frequency from the DDS module can be reconfigured according to the frequency of the target signal when measuring signals with different frequencies. The band-pass-filters (BPF) can also be used to filter the non-target signals, whereas the parameters of the BPFs should be re-designed and re-loaded when the frequency of the input signal varies. The high performance FFT spectrum analyzer provides a signal processing capacity of measuring signals with various frequencies without redesigning the filters, thus considerable flexibility can be obtained.

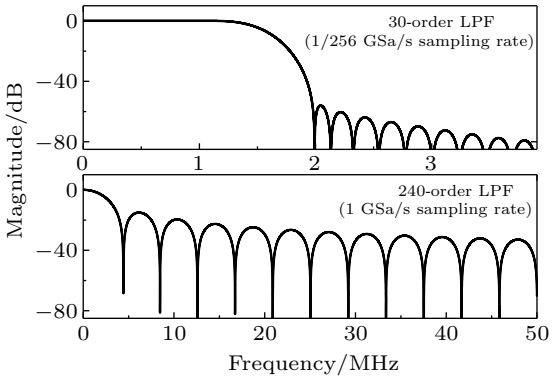

Fig. 8. The plots of frequency response characteristics of the filter. (a), (b) The filters operating at a 1/256 GSa/s and a 1 GSa/s sampling rates, respectively.

4.3. Operating efficiency

In order to demonstrate the operating efficiency of the high performance FFT spectrum analyzer, the occupied operating time for obtaining a single FFT spectrum (32768 samples) and processing 1 Giga samples is measured. We have also developed customized software (Python and C++) based FFT programs which have the same function as the hardware reported in this paper, and an efficiency comparison between the FFT spectrum analyzer and the software-based FFT is shown in Table 1. As the modules in the FPGA-based FFT spectrum analyzer operate in parallel, each module requires 32.75 μs in a single FFT operation, and the total operating time is also 32.75 μs. Thus 30534 FFT spectrums can be obtained within one second using the FFT spectrum analyzer. The software programs occupy more time to perform the same

function. On the other hand, the software operates in serial, therefore the total processing time is much longer than the operating time of a single module. The python based software requires 6898.8 seconds to process 1 Giga samples, and the C++ based software needs to occupy 2298.1 seconds to finish the operation. On the other hand, the FFT spectrum analyzer requires 1 second to process 1 Giga samples. Hence, the reported spectrum analyzer provides a real-time data processing capacity with a 100 percent data utilizing rate in measuring spin noise spectrums.

Table 1. Efficiency comparison between this work and the software based FFT.

Module		FFT	Reconstruction	Filter (one stage)	Down converter	Total time
Time occupation (single FFT spectrum)	FFT DAQ (This work)	32.75 μs	32.75 μs	32.75 μs	32.75 μs	32.75 μs
	Software (Python)	1.2 ms	26.8 ms	22.1 ms	5.8 ms	226 ms
	Software (C++)	1.1 ms	4.6 ms	3.97 ms	2.8 ms	75.3 ms
Time occupation (1 Giga samples)	FFT DAQ (This work)	1 s	1 s	1 s	1 s	1 s
	Software (Python)	40.8 s	876.8 s	723.8 s	190.8 s	6898.8 s
	Software (C++)	33.6 s	140.4 s	121.2 s	85.4 s	2298.1 s

5. Resource occupation

The resource occupation of the hardware accelerated FFT spectrum analyzer is shown in Table 2. 6-input look up tables (LUT), flip flops, and slices are the basic user defined FPGA resources. LUT RAMs and BRAMs are internal data storages that are integrated inside the FPGA. The DSP units are the integrated hardware digital signal processing resources inside the FPGA chip. An 8-stage LPF filter occupies 480 DSP units, thus 960 DSP units are required to manage the real part and the imaginary part of the spin noise signals simultaneously. More than 85 percent of the BRAM resources in the Virtex-7 FPGA XC7VX485T-ffg1761 are utilized to realize the FFT spectrum analyzer.

Table 2. Resource occupation of the hardware accelerated FFT DAQ board.

Resource[a]	FFT	Reconstruction	DDR3 controller	DDS	Filter	Data storage	Total occupation	Available
6-input LUT	5182	36637	22324	91	35019	18267	128038	303600
LUT RAM	1257	25	3438	0	15582	9674	31281	130800
Flip-flop	7964	53627	15097	304	61735	23198	175896	67200
Slice	2003	12955	7100	84	14376	4259	44601	75900
DSP	31	4		3	1160	0	1300	2800
BRAM (36 kb)	97	402	0	1	0	46	840	1030

[a]6-input look up tables (LUT), flip flops (FF), slice are the basic resources of the FPGA chip. LUT RAM are the memories generated using FPGA logics.

Table 3. Performance comparison among FFT DAQs.

Analyzer (Ref.)	This work	Iglesias *et al.*[19]	Agilent N9030A[20]	Tektronics RSA5000[21]	Li[27]	Crooker[17]
N[a]	32768	4096	1024	1024–32768	128000	32768
Bandwidth	500 MHz	100 MHz	160 MHz	110 MHz	500 MHz	1 GHz
Resolution	119 Hz–30.5 kHz	48 kHz	383 kHz	20 kHz	7.8 kHz	61 kHz
Spectrums/s	30.5 k	24.4 k	292 k	30.5 k–292 k	N/A	61 k

[a]The number of FFT points to obtain a single FFT spectrum.

6. Conclusion

We report the principle and the implementation of a high performance FFT spectrum analyzer. The spectrum analyzer can be used to obtain high frequency resolution FFT spectrums with enhanced SNR. The frequency resolution and the parameters of the data processing modules are reconfigurable, thus the spectrum analyzer provides favorable flexibility in spin noise spectrum measurements. A 100 percent real-time data utilization rate is obtained, hence the spin noise spectrums can be measured effectively. In future studies, the high performance FFT spectrum analyzer can be applied to study complex spin noise spectrums with multiple frequency signals. A comparison among various FFT spectrum analyzers is listed in Table 3 for a quick reference.

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