Simulation study of high voltage GaN MISFETs with embedded PN junction*

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In this paper, we propose a new enhanced GaN MISFET with embedded pn junction, *i.e.*, EJ-MISFET, to enhance the breakdown voltage. The embedded pn junction is used to improve the simulated device electric field distribution between gate and drain, thus achieving an enhanced breakdown voltage (BV). The proposed simulated device with $L_{GD} = 15$ μm presents an excellent breakdown voltage of 2050 V, which is attributed to the improvement of the device electric field distribution between gate and drain. In addition, the ON-resistance (R_{ON}) of 15.37 Ω·mm and Baliga's figure of merit of 2.734 GW·cm^{-2} are achieved in the optimized EJ-MISFET. Compared with the field plate conventional GaN MISFET (FPC-MISFET) without embedded pn junction structure, the proposed simulated device increases the BV by 32.54% and the Baliga's figure of merit is enhanced by 71.3%.

Keywords: TCAD, Baliga's figure of merit (BFOM), breakdown voltage (BV)

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1. Introduction

Gallium nitride (GaN)-based electronic devices have become one of the most promising candidates for power applications. Owing to the strong polarization charge in the AlGaN/GaN hetero-junction, high-density two-dimensional electron gas (2DEG) is formed at the interface between GaN and AlGaN.[1–5] It has drawn intensive attention for high voltage applications due to its wide band gap. However, it is still a challenge to improve the breakdown voltage.[6] Like the scenario in LDMOS, the peak electric field in GaN MISFET is distributed in the device surface. Chen has made a great contribution to the development of power device, and he proposed a composite buffer layer structure which was called COOLMOS^{TM}.[7] Moreover, theoretical analysis on the structure was reported in detail, and the structure was also called the super junction. The super junction concept was also known as super multi-RESURF.[8] So, the technologies of RESURF were widely applied to power devices. Back electrode has been used to realize RESURF GaN HEMT in Ref. [9]. Field plate is also a common method to improve the electric field distribution.[10] Source field plates, gate field plates, and drain plates were used to improve the electric field distribution between gate and drain.[11–15] Some researchers demonstrated the GaN-based super HFETs based on polarization junction concept and they have great power characteristics.[16] Some researchers proposed a novel enhancement-mode polarization-junction HEMT with vertical conduction channel which has a uniform electric field distribution between source and drain.[17] Some researchers proposed and experimentally demonstrated a high-breakdown-voltage HEMT by implanting fluorine ions in a thick SiN_x passivation layer between the gate and drain. The fluorine ions in the passivation layer can extend the depletion region and improve the average electric field between gate and drain.[18] A large gate metal height was proposed to enhance breakdown voltage in GaN-based HEMTs and the breakdown voltage enhancement resulting from the increase of the gate sidewall capacitance and depletion region extension.[19]

In this paper, we introduce an MISFET with embedded pn junction (EJ-MISFET). The N-type layer and P-type layer form a pn junction which is embedded in the barrier layer and the buffer layer. To ensure the ON-resistance remains stable and consistent, a part of 2DEG is replaced with a highly doped N-type layer. The P-type layer is embedded in the N-type layer. The embedded pn junction improves the device's electric field distribution between the gate and the drain to enhance the breakdown voltage.

Additionally, the substrate of the conventional GaN MISFET (C-MISFET), field plate conventional GaN MISFET (FPC-MISFET) and proposed EJ-MISFET are removed for suppressing the vertical leakage current through substrate.[20] With the same parameter, the authors in Ref. [21] showed the experimental results. In the present paper, we propose a new architecture to improve the breakdown voltage of the simulated device. We simulate the structure by using Sentaurus TCAD tools,[22] verifying that the proposed EJ-MISFET structure provides higher breakdown voltage than the conven-

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tional one with field plates.

2. Proposed structure and principle

Figures 1(a) and 1(b) illustrate the architecture of the FPC-MISFET and the EJ-MISFET, respectively. The parameters of the FPC-MISFET without field plate are the same as those of the GaN-on-Si sample in Ref. [21]. The epitaxial layers each consist of 2.4-μm Al-containing transition layer, 1.6-μm GaN buffer layer, and 21-nm AlGaN barrier layer. The mole fraction of the AlGaN barrier in the FPC-MISFET and that in the EJ-MISFET are both 0.25. The unintentionally doped (UID) GaN buffer layer is doped with 1×10^{15} cm^{-3} N-type concentration.[23] For the two structures the fully recessed gate technique is used, and the Si_3N_4 is chosen as the gate dielectric and passivation layer. The thickness of the gate dielectric and the passivation layer are 17 nm and 100 nm respectively.

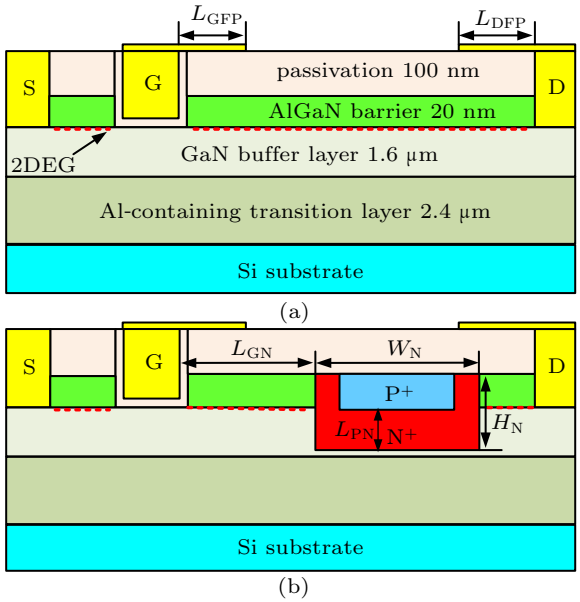

Fig. 1. Schematic diagram of (a) FPC-MISFET and (b) EJ-MISFET.

The details of key structural parameters of FPC-MISFET and proposed EJ-MISFET are summarized in Table 1. Figure 2 shows the brief steps of fabrication processes for the proposed structure, and the step for each graph may be summarized as follows.

(i) Growing transition layer on a silicon (111) substrate, then growing a buffer layer and an AlGaN barrier layer on the transition layer in turn by MOCVD.[21,24]

(ii) Forming SiO_2 as the etching mask by using plasma-enhanced chemical vapor deposition.[25,26]

(iii) Etching AlGaN barrier layer and GaN buffer layer by transformer-coupled-plasma reactive ion etching in a BCl_3/Cl_2 gas mixture.[27]

(iv) Performing a combination of UV-ozone cleaning and HF + HCl wet etch to reduce impurity concentration at the etched surface, and the N-typer layer and P-type layer are regrown by MBE.[28,29]

(v) Depositing a SiO_2 mask on the top of P-type layer by using the plasma-enhanced chemical vapor deposition, forming an N-type layer by using Si ion implantation.[30,31]

(vi) After implantation, removing the SiO_2 mask by using the hydrofluoric acid followed by a postimplantation annealing to activate the implanted Si and removing the surface native oxide on the sample with minimum surface damage by using *in situ* remote plasma pretreatment (RPP) and depositing Si_3N_4 as passivation layer by using plasma-enhanced chemical vapor deposition.[24,32]

(vii) Etching Si_3N_4 by inductively coupled plasma (ICP) and achieving the gate recess by a low-power ICP dry-etch.[24]

(viii) Depositing Si_3N_4 as gate dielectric by using plasma-enhanced chemical vapor deposition.

(ix) Forming gate electrode and forming an ohmic contact source electrode and an ohmic contact drain electrode.

Table 1. Key structural parameters.

Parameters	Unit	Values
Distance from source to gate (L_{SG})	μm	2
Gate length (L_G)	μm	1.5
Gate field plate length (L_{GFP})	μm	3
Drain field plate length (L_{DFP})	μm	0.5
Distance from gate to drain (L_{GD})	μm	15
Thickness of gate dielectric (T_{Gd})	nm	17
Thickness of passivation layer (T_{pass})	nm	100
Thickness of $Al_{0.25}Ga_{0.75}N$ barrier layer (T_{bar})	nm	21
Thickness of GaN buffer layer (T_{buff})	μm	1.6
Thickness of Al-containing transition layer ($T_{transition}$)	μm	2.4
Distance from gate to N-type layer (L_{GN})	μm	13
Distance from N-type layer to P-type layer (L_{PN})	μm	0.01
N-type layer length (W_N)	μm	1.5
Thickness of N-type layer ($H_{N)}$	nm	41
Thickness of P-type layer ($H_{P)}$	nm	31
P-type layer doping concentration (N_{P+})	cm^{-3}	1×10^{17}
N-type layer doping concentration (N_{N+})	cm^{-3}	1×10^{19}
GaN buffer doping concentration (N_{buff})	cm^{-3}	1×10^{15}

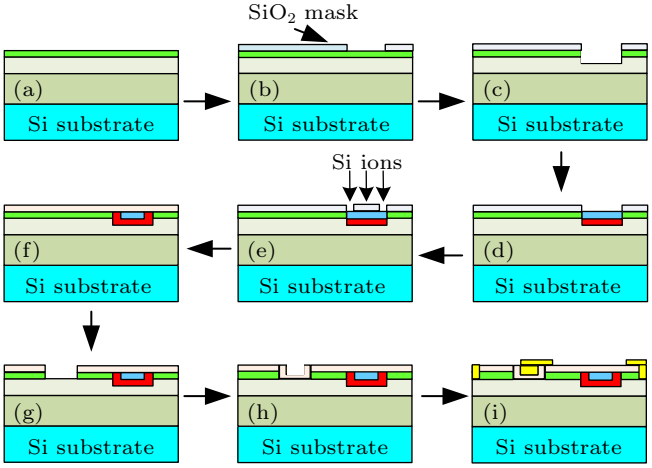

Fig. 2. Schematic diagram of fabrication steps for proposed structure.

To achieve more accurate simulations, we select some suitable physical models which were widely used, such as the Recombination models, *e.g.*, Shockley–Read–Hall (SRH) model and Auger model, and the mobility models, *e.g.*, DopingDep model and high-field-saturation model.[33] Besides, the polarization effects of AlGaN and GaN are calculated by the piezoelectric_polarization (strain) model.[34] The thermionic model is used to account for the self-heating effect on the assumption that the charge carriers are in thermal equilibrium with the lattice. The avalanche model is used to simulate the device breakdown.

Figure 3(a) shows the comparison of I_D–V_{DS} characteristic between the experimental results by Tang *et al.*[21] and simulation results by TCAD, for $V_{DS} = 10$ V and $V_{GS} = 2$ V, 4 V, 6 V, 8 V, and 10 V. From this figure we can see that the I_D–V_{DS} characteristics with different values of V_{GS} fit well with the experimental results[21] and the R_{ON} of 14.98 Ω· mm from TCAD simulation by sentaurus is close to that of 16.1 Ω·mm from experimental results.

Figure 3(b) shows the blocking characteristics between TCAD simulation and experiments. The breakdown voltage of simulated device is close to the experimental result. Because the field plates have a great effect on blocking characteristics, we prefer to select optimized field plates conventional MISFET for comparison.

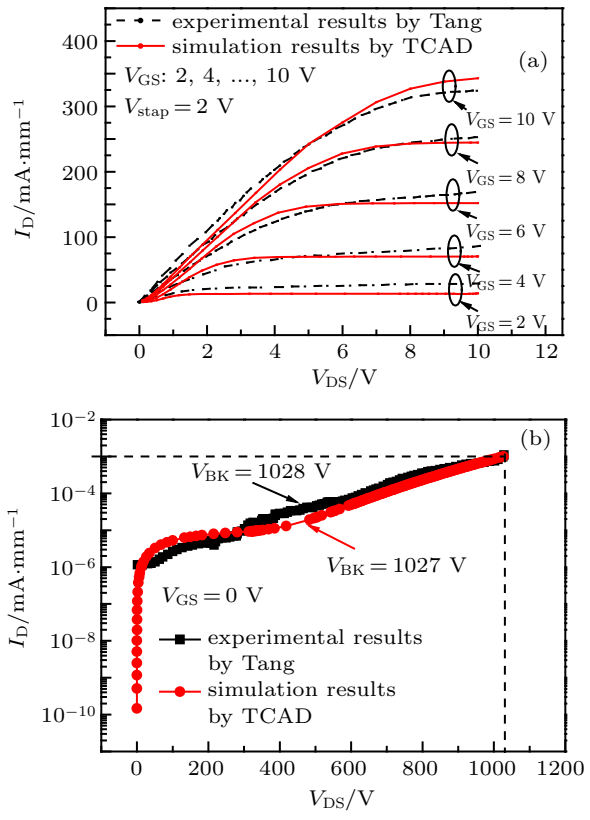

Fig. 3. (a) The I_D–V_{DS} characteristic curves and (b) blocking characteristic cuves from simulation and experiment to validate effectiveness of models used in simulation.

3. Results and discussion

Figure 4 shows the plots of the comparison of the device channel electric field distributions on condition that three types of GaN MISFETs are breakdown. This figure shows a high electric field accumulating on the drain side in the gate electrode corner for the C-MISFET. For the C-MISFET, the peak of the electric field near the gate reaches up to 4×10^6 V/cm which almost arrives at the critical electric field of GaN material.[35] Therefore the device has been breakdown before the 2DEG is depleted completely. For the FPC-MISFET, with the gate filed plate and drain field plate introduced, the electric field near the gate sharply decreases and a peak electric field appears at the position near the gate field plate. Compared with the C-MISFET, the FPC-MISFET can improve the electric field distribution between gate and drain.

For the GaN MISFET, the drain leakage current is mainly composed of substrate-drain leakage current and source–drain leakage current.[36] In Ref. [21], the floating substrate could achieve higher device voltage rating and enable better dynamic R_{ON} for high drain bias switching operation. In the present simulation, substrate is float, thus avoiding substrate-drain leakage current. On the other hand, the source–drain leakage current is mainly caused by the buffer leakage current. When the N-type layer and P-type layer are introduced into the FPC-MISFET, the N-type layer and unintentionally doped GaN buffer layer form an N-/N+ junction which introduces a peak electric field in the GaN buffer layer, thereby improving the device internal electric field distribution. The N-type layer and P-type layer form an N/P junction, thus improving the electric field distribution between gate and N-type layer. Because of the P-type layer under the drain field plate, the peak electric field near the drain field plate decreases sharply.

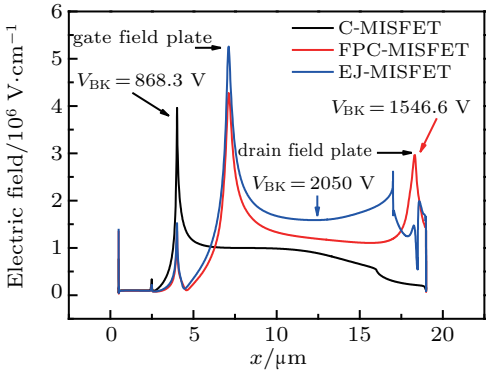

Fig. 4. Channel electric field distribution of C-MISFET (without field plates), FPC-MISFET, and EJ-MISFET.

Figure 5 shows the plots of the off-state characteristic of the C-MISFET, FPC-MISFET, and EJ-MISFET, and also displays the comparison among the simulated off-state characteristic curves at $V_{GS} = 0$ V for the three architectures with

$L_{GD} = 15$ μm. The breakdown voltage is defined as the voltage at a drain current of 10^{-6} A/mm in the off-state. The simulation breakdown voltage of the C-MISFET is 868.3 V, the simulation breakdown voltage of the FPC-MISFET is 1546.6 V and the simulation breakdown voltage of the EJ-MISFET is 2050 V. It may be seen that with the introduction of the field plates, the blocking capability of the C-MSIFET increases to a certain extent. And, the embedded pn junction helps the FPC-MISFET further improve the breakdown characteristic. The simulation breakdown voltage of the FPC-MISFET is increased by 32.54%.

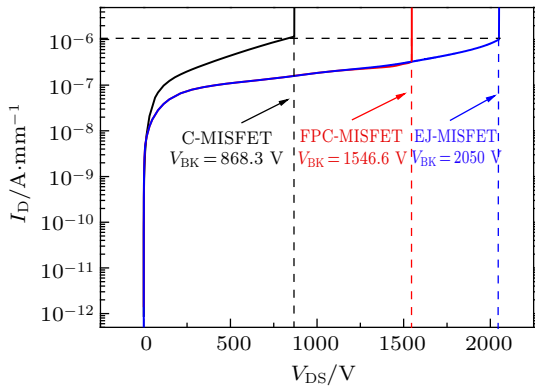

Fig. 5. Off-state breakdown voltage from simulation of C-MISFET (without field plate), FPC-MISFET, and EJ-MISFET.

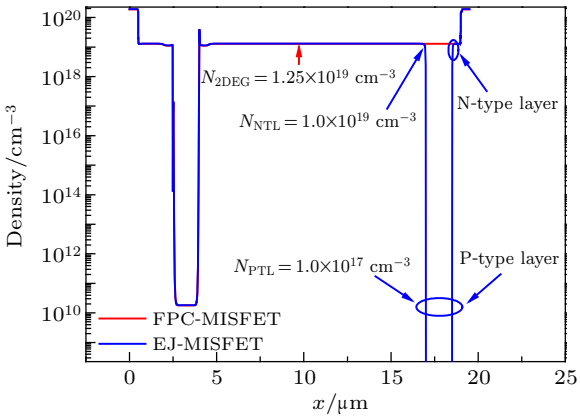

Fig. 6. Lateral electron density distribution in 2DEG for FPC-MISFET and EJ-MISHFET.

The lateral electron density distribution in 2DEG is shown in Fig. 6. To match the experimental results, 4.8×10^{12} cm^{-3} trap is set to be in the face of the AlGaN/GaN hetero-junction, and the 2DEG density N_{2DEG} is assumed to be 1.25×10^{19} cm^{-3}. The density of P-type layer takes a value of 1×10^{17} cm^{-3}, which is enough to deplete the extra charge generated by the N-type layer. The 2DEG in the P-type layer region is replaced by the P-type layer. The P-type layer is embedded in the N-type layer, thus cutting off a part of the 2DEG between gate and drain. The density of N-type layer with a value of 1×10^{19} cm^{-3}, is close to the 2DEG density (N_{2DEG}). The distance from N-type layer to P-type layer (L_{PN}) is 0.01 μm, which is appropriate to realize low channel resistance, although a part of 2DEG is replaced by N-type layer and P-type layer.

Figure 7 shows the comparison of drain current curves between the FPC-MISFET and EJ-MISFET for $V_{DS} = 10$ V and $V_{GS} = 2$ V, 4 V, 6 V, 8 V, and 10 V. We see that the current of EJ-MISFET is almost similar to that of the FPC-MISFET. The GaN based electronic device output characteristic is mainly determined by the density of 2DEG and the channel current density. The FPC-MISFET and EJ-MISFET have similar channel current densities. For the EJ-MISFET, a highly doped N-type layer is used to replace a part of 2DEG region. The concentration of N-type layer is close to the density of 2DEG that leads to a similar on-state current. The R_{ON} of the EJ-MISFET with a value of 15.37 Ω·mm which is slightly higher than that of the FPC-MISFET with a value of 14.98 Ω·mm.

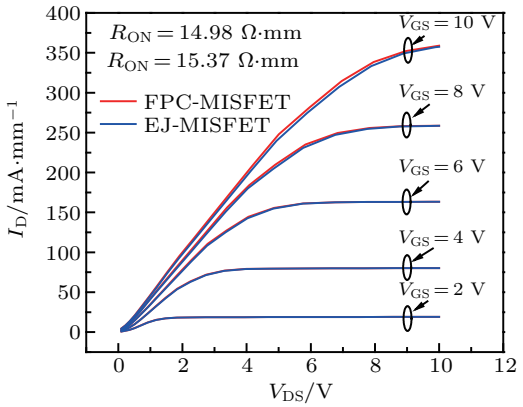

Fig. 7. Output characteristics of FPC-MISFET and EJ-MISFET.

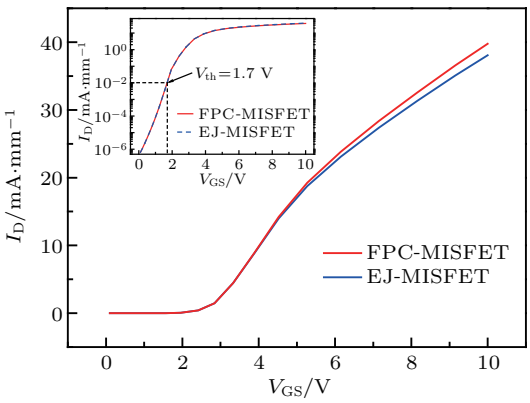

Fig. 8. Transfer characteristics of FPC-MISFET and EJ-MISFET.

Figure 8 shows the comparison of transfer characteristic curve between the FPC-MISFET and the EJ-MISFET at $V_{DS} = 1$ V. The threshold voltages of both structures are both about 1.7 V, and the threshold voltage is determined at $I_{DS} = 0.01$ mA/mm. As is well known, the threshold voltage of the GaN MISFET structure is mainly determined by the thickness of gate dielectric and the space charge under the gate electrode. The proposed EJ-MISFET structure has not any effect on the thickness of gate dielectric nor the space charge under the gate

electrode. Hence, the EJ-MISFET does not change the structure transfer characteristic. The EJ-MISFET structure adopts highly doped N-type layer to replace a part of 2DEG, and the current density between gate and drain decreases slightly.

Figure 9 shows the plot of V_{BK} and R_{ON} *versus* N_{N+} for optimized EJ-MISFET. The R_{ON} reaches a maximum when N_{N+} is 6×10^{18} cm^{-3}. As the doping of N-type layer increases, the R_{ON} value decreases. When the doping of the N-type layer reaches 1×10^{19} cm^{-3}, the simulated device breakdown voltage reaches the maximum value 2050 V and the Baliga's figure of merit (BFOM) tends to maximum and reaches to a value of 2.734 GW·cm^{-2}.

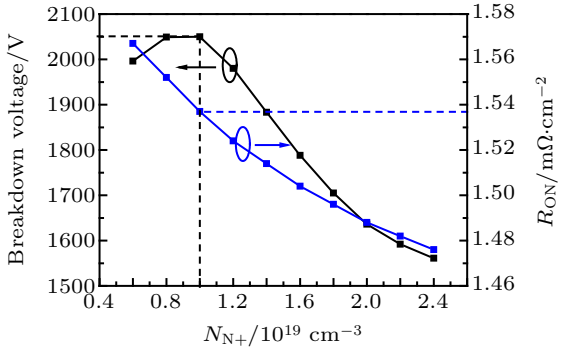

Fig. 9. Plot of optimized V_{BK} and R_{ON} *versus* N_{N+} with N_{N+} ranging from 6×10^{18} cm^{-3} to 2.4×10^{19} cm^{-3} and L_{GN} taking optimized value.

Figure 10 shows the plot of V_{BK} and R_{ON} *versus* L_{GN} for the optimized EJ-MISFET. When the length of L_{GN} is 4 μm, the V_{BK} keeps a minimum 1500 V. With the increase of L_{GN}, the V_{BK} increases almost lineraly. When the length of L_{GN} increases up to 13 μm, the V_{BK} reaches the maximum 2050 V. The trend of the corresponding calculated R_{ON} is maintained within a narrow range, while the trend of the optimized BFOM is consistent with that of optimized V_{BK}. We achieve a maximum BFOM of 2.734 GW·cm^{-2} at $L_{GN}=13$ μm and $N_{N+}=1.0\times10^{19}$ cm^{-3}.

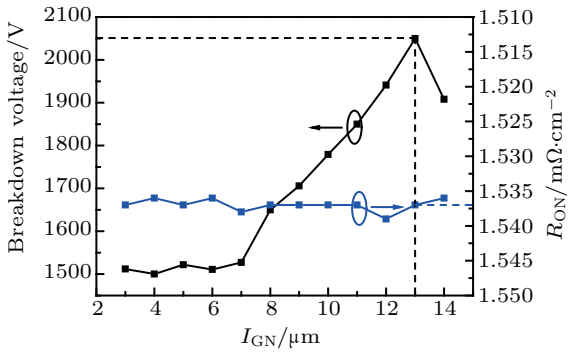

Fig. 10. Plot of optimized V_{BK} and R_{ON} *versus* L_{GN} with L_{GN} ranging from 3 μm to 14 μm and N_{N+} bing 1×10^{19} cm^{-3}.

Figure 11 shows the plot of V_{BK} and R_{ON} *versus* W_N for the optimized EJ-MISFET. As W_N rises, the breakdown voltage goes up. When $W_N=1.5$ μm, the breakdown voltage reaches the saturation value 2050 V. With the increase of W_N, more 2DEGs are produced by N-type layer, the R_{ON} increases gradually. Figure 12 shows the plot of V_{BK} and R_{ON} *versus* H_N for the optimized EJ-MISFET. The V_{BK} and R_{ON} decrease with H_N increasing.

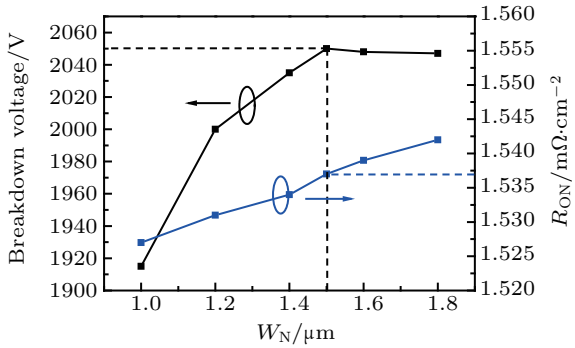

Fig. 11. Plot of V_{BK} and R_{ON} *versus* W_N with W_N ranging from 1 μm to 1.8 μm.

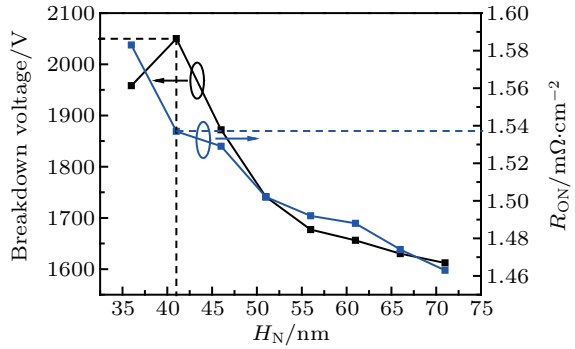

Fig. 12. Plot of V_{BK} and R_{ON} *versus* H_N with H_N ranging from 36 nm to 71 nm and H_P being 31 nm.

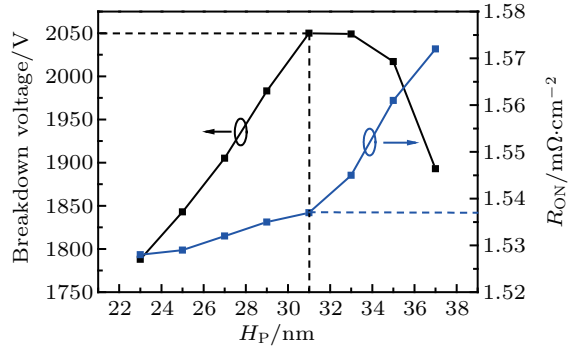

Fig. 13. Plot of V_{BK} and R_{ON} *versus* H_P with H_P ranging from 23 nm to 37 nm and H_N being 41 nm.

Figure 13 show the plot of V_{BK} and R_{ON} *versus* H_P for the optimized EJ-MISFET. With H_P increasing, the breakdown voltage first rises and then falls. Larger H_P means that lower H_N causes R_{ON} to rise with H_P increasing. When $H_P=31$ nm, the breakdown voltage reaches the maximum value 2050 V. Figure 14 shows the plot of V_{BK} and R_{ON} *versus* of the optimized EJ-MISFET. With N_P increasing, the breakdown voltage first rises slightly and then drops down. The R_{ON} keeps rising with N_P increasing. More N-type layers will be depleted and the breakdown voltage fluctuations are maintained in a small range of the voltage margin when increasing doping concentration of P-type layer. Summarized in Table 1 are the performances of the devices in this paper and other reported normally-off GaN devices.

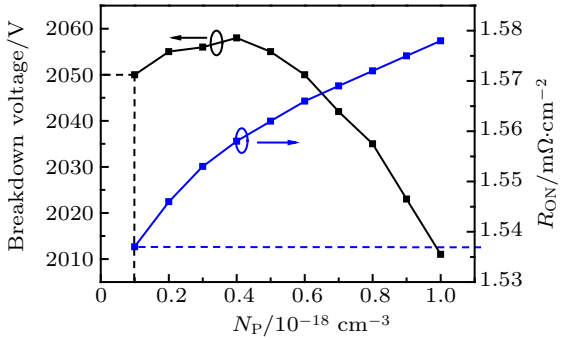

Fig. 14. Plot of V_{BK} and R_{ON} *versus* N_P, N_P ranging from 1×10^{17} cm^{-3} to 1×10^{18} cm^{-3}.

Summarized in Table 2 are the performances of the devices in this paper and other reported normally-off GaN devices. It is obvious that the proposed EJ-MISFET shows the highest V_{BK} in these reported normally-off GaN device results. It indicates the EJ-MISFET structure has excellent potential applications in high power devices.

Table 2..Comparison of device characteristic between device in this paper and other reported GaN devices.

V_{BK}/V@1 μA/mm	R_{ON}/Ω·mm	References
868	14.98	C-MISFET
1546	14.98	FPC-MISFET
2050	15.37	EJ-MISFET
650	13.2	[24]
1290	10.3	[37]
1400	9.2	[38]
1456	10.1	[39]
1528	13.3	[40]

4. Conclusions

We investigated the behavior of the GaN MISFET structure with embedded pn junction which realizes the improvement of the device electric field distribution. It is shown that the breakdown voltage of the proposed EJ-MISFET reaches up to 2050 V. Compared with the FPC-MISFET, the EJ-MISFET provides 32.54% improvement in the breakdown voltage. The R_{ON} of the proposed EJ-MISFET is 15.37 Ω·mm. The transfer characteristic keeps almost the same and the V_{TH} values of two structures are both 1.7 V. The optimized device with $L_{GN} =$ 13 μm exhibits a high power BFOM of 2.734 GW·cm^{-2}, V_{BK} of 2050 V, and an R_{ON} of 15.37 Ω·mm. Compared with that of the FPC-MISFET, the Baliga's figure of merit of the EJ-MISFET is enhanced by 71.3%.

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