Interface and border trapping effects in normally-off Al_2O_3/AlGaN/GaN MOS-HEMTs with different post-etch surface treatments*

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Trapping effect in normally-off Al_2O_3/AlGaN/GaN metal–oxide–semiconductor (MOS) high-electron-mobility transistors (MOS-HEMTs) with post-etch surface treatment was studied in this paper. Diffusion-controlled interface oxidation treatment and wet etch process were adopted to improve the interface quality of MOS-HEMTs. With capacitance–voltage (C–V) measurement, the density of interface and border traps were calculated to be 1.13×10^{12} cm^{-2} and 6.35×10^{12} cm^{-2}, effectively reduced by 27% and 14% compared to controlled devices, respectively. Furthermore, the state density distribution of border traps with large activation energy was analyzed using photo-assisted C–V measurement. It is found that irradiation of monochromatic light results in negative shift of C–V curves, which indicates the electron emission process from border traps. The experimental results reveals that the major border traps have an activation energy about 3.29 eV and the change of post-etch surface treatment process has little effect on this major activation energy.

Keywords: AlGaN/GaN MOS-HEMTs, interface traps, border traps, photo-assisted C–V measurement

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1. Introduction

AlGaN/GaN high-electron-mobility transistors (HEMTs) have demonstrated state-of-the-art performance for high frequency and high-power applications.[1–4] The strong polarization effect in conventional AlGaN/GaN HEMTs results in normally-on devices, while normally-off operation is preferred to in practical circuits in terms of maintaining the system safety, reducing power consumption, and simplifying circuit design.[5,6] Recess-gate metal–oxide–semiconductor HEMTs (MOS-HEMTs) have been widely studied to achieve normally-off GaN-based devices, which have smaller leakage current and larger gate voltage swing compared with Schottky-gate HEMTs.[7,8] However, there exist a large amount of interface charges between gate dielectric and nitride semiconductor, being one of the critical issues that restrict the development of device performance and reliability.[9,10] For recess-gate devices, the plasma etch process of gate trench may cause rough nitride surface, leading to worse interface quality of MOS-HEMTs.[11–13] Therefore, the interface analysis as well as its improvement is of vital importance for GaN-based recess-gate MOS-HEMTs.

Generally, there exist three kinds of oxide-related charges in GaN-based MOS-HEMTs having major influence on device performance and reliability, including interface traps, interface fixed charges, and border traps.[14,15] The previous works about normally-on MOS-HEMTs demonstrated that interface traps caused transient threshold voltage (V_{th}) instability while border traps induced retentive V_{th} shift.[16] The high density of interface fixed charges does not exhibit trapping effect, but it will lead to a negative V_{th} shift, being an obstacle to normally-off operation. Various methods have been developed to solve the interface issue, which can be classified into two types either by effective removing the native oxide layer[17] or by forming a high-quality interfacial layer.[18] In our previous work, we presented diffusion-controlled interface oxidation (DCIO) process,[19,20] which resulted in an increase in the conduction band offset at Al_2O_3/AlGaN interface by over 0.6 eV and a decrease in MOS interface charges by about 4×10^{12} cm^{-2} DCIO is a promising interfacial engineering method for both MOS-HEMTs with and without recess gate. This novel interface oxidation method followed by wet etch was then used for the post-etch surface treatment of normally-off Al_2O_3/AlGaN/GaN MOS-HEMTs, leading to an improvement of channel transport property, on-resistance, and breakdown voltage.

To evaluate the interface treatment method comprehensively, quantitative characterization of interface charges in detail is desirable. The change of interface fixed charges can be easily derived from a voltage shift of transfer sweep or capacitance–voltage (C–V) curves. Many methods have also been reported to map the interface traps in GaN devices,

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such as frequency-dependent *C–V* measurement,[21] conductance method,[22–24] and transient current or capacitance.[25,26] For the border traps, however, it is quite difficult to identify the trap density and its mapping because of the very long time constant during de-trapping process and uncertain trap location away from interface. In this paper, normally-off Al_2O_3/AlGaN/GaN MOS-HEMTs were achieved with fully recessed gate, and then the influence of DCIO treatment and wet etch after recess etch on trapping effect was investigated in detail. Sequential hysteresis *C–V* sweeps with increased gate swing voltage show two types of voltage shift induced by interface trapping and border trapping, respectively, which is similar to the case in normally-on devices. Photo-assisted *C–V* measurement[27,28] was used to identify the activation energy and density distributions of deep-level interface traps and border traps. The major border traps have an activation energy of de-trapping process about 3.29 eV for both two devices with different post-etch surface treatment methods.

2. Device fabrication

The AlGaN/GaN epilayers used in this paper were grown by metal organic chemical vapor deposition on sapphire substrate, consisting of a 180-nm AlN nuclear layer, a 0.8-μm carbon-doped GaN buffer layer, a 1-μm unintentionally doped (UID) GaN channel layer, a 0.6-nm thick AlN interlayer, a 21.6-nm $Al_{0.25}Ga_{0.75}N$ barrier layer, and a 2.9-nm GaN cap layer from bottom to top, as shown in Fig. 1. Hall measurement shows that the carrier density and mobility are 9.78×10^{12} cm^{-2} and 1675 cm^2/V·s, respectively.

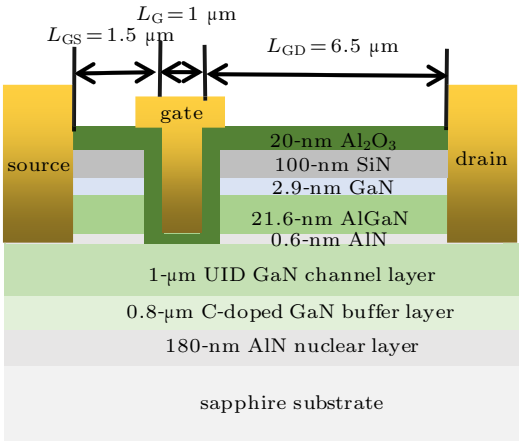

Fig. 1. Schematic cross section of recess-gate Al_2O_3/AlGaN/GaN MOS-HEMTs.

Device fabrication started with Ohmic contacts of Ti/Al/Ni/Au. Ohmic contact resistance of 0.52 Ω·mm was achieved after rapid thermal annealing at 880 °C in N_2 for 50 s. Then mesa isolation was performed by inductively coupled plasma (ICP) etch with a depth of 125 nm, followed by 100-nm SiN passivation layer grown with plasma-enhanced chemical vapor deposition (PECVD). Before gate fabrication process the PECVD-grown SiN layer and $Al_{0.25}Ga_{0.75}N$ barrier layer beneath gate area were completely removed using CF_4 and BCl_3/Cl_2 plasma etch in sequence. After plasma etch, the surface contaminant and residual photoresist were cleaned by organic solutions and $NH_3{\cdot}H_2O$ (1:6) at 55 °C. To improve the post-etch surface morphology, DCIO oxidation treatment[19] and wet etch in 1:5 HCl solution were carried out. Then 20-nm Al_2O_3 gate insulator layer was grown by atomic layer deposition (ALD) at 300 °C, following *in situ* nitridation plasma pre-treatment. The gate electrodes of Ni/Au were evaporated on the Al_2O_3 gate insulator layer. Finally, the device underwent post metallization annealing (PMA) in O_2 at 450 °C for 5 minutes using rapid thermal annealing system.

Two kinds of devices with different post-etch surface treatment processes were studied, the one with the aforementioned process (sample 1#) and the controlled one without DCIO oxidation and wet etch (sample 2#). MOS-HEMTs have T-shaped gate with gate foot length (L_G) of 1 μm, gate cap length of 2.8 μm, and gate width (W_G) of 50 μm. The gate–source (L_{GS}) and gate-drain (L_{GD}) distance are 2.5 μm and 6.5 μm, respectively. Ring diode were also fabricated for *C–V* measurement, with gate diameter of 130 μm and gate-ohmic distance of 25 μm.

3. Results and discussion

The interface quality of recess-gate normally-off MOS-HEMTs was characterized using transmission electron microscope (TEM) as shown in Fig. 2. There exists about 5 nm over etch into the GaN channel layer for the gate trench process. Enlarged views at Al_2O_3/GaN interface show that a rough interface can be observed for the controlled sample, which will cause a high density of interface charges and degrades the channel transport property of recess-gate normally-off MOS-HEMTs. MOS-HEMTs with DCIO oxidation and wet etch post-etch surface treatment show a sharp Al_2O_3/AlGaN interface by effective removal of surface damage and native oxide.

Figure 3(a) shows the transfer characteristics of normally-off MOS-HEMTs with different post-etch surface treatment processes, where the drain voltage (V_D) is 10 V and the gate voltage (V_{GS}) sweeps from 0 V to 15 V. V_{th} is defined as the maximum gate voltage where the drain current is below 10 μA/mm, estimated to be 2.8 V and 3.1 V for samples 1# and 2#, respectively. DCIO treatment and wet etch after recess etch lead to an increase in maximum drain current (I_d) from 174 mA/mm to 294 mA/mm and an increase in peak transconductance (G_m) from 14 mS/mm to 40 mS/mm. In addition, the OFF-state leakage current reaches 1 mA/mm at $V_D = 94$ V for sample 2#, while the breakdown voltage increases up to 260 V for sample 1# with DCIO treatment and wet etch, as shown in Fig. 3(b).

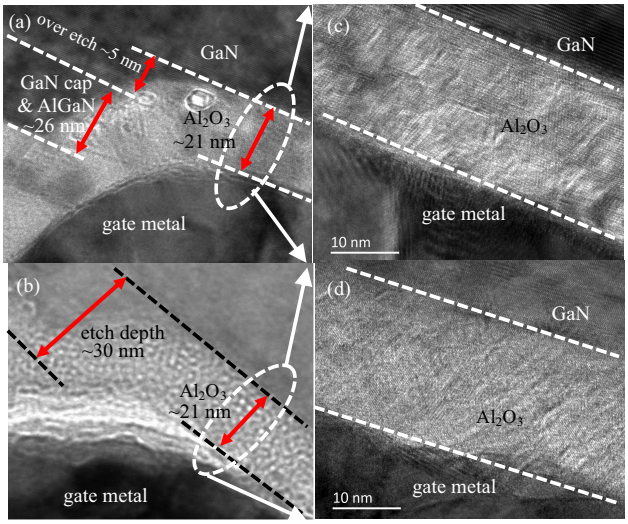

Fig. 2. (a)-(b) Cross-sectional TEM micrographs of recess-gate Al_2O_3/AlGaN/GaN MOSHEMTs and (c)–(d) the enlarged view at Al_2O_3/GaN interface: (a) sample 1# with DCIO and wet etch post-etch surface treatment and (b) the controlled sample 2#.

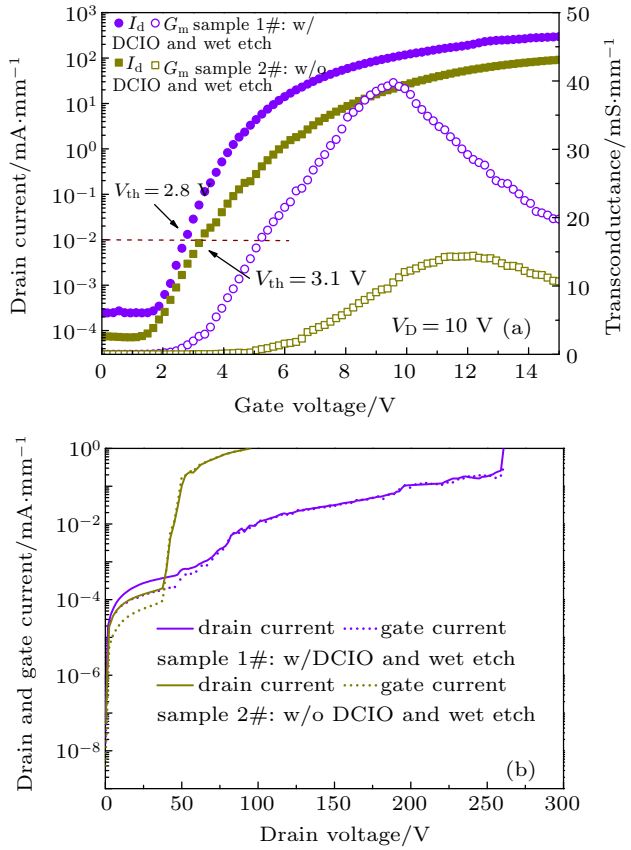

Fig. 3. Influence of post-etch surface treatment on normally-off Al_2O_3/AlGaN/GaN MOS-HEMTs in terms of (a) transfer and transconductance characteristics and (b) breakdown characteristics.

It is obvious that post-etch surface treatment with DCIO treatment and wet etch results in improved device performance. The interface issue of recess-gate Al_2O_3/AlGaN/GaN MOS-HEMTs was studied using *C*–*V* hysteresis measurement as shown in Fig. 4. During each hysteresis sweep, gate voltage is swept from the maximum gate voltage to 0 V and then swept back. The maximum gate voltage during each sweep is defined as program voltage (V_p), which is increased from 6 V to 15 V with step of 1 V. The ascending region in *C*–*V* curve corresponds to the accumulation of electron at Al_2O_3/GaN interface, and capacitance plateau represents the capacitance of Al_2O_3 dielectric ($C_{Al_2O_3}$). Devices with DCIO treatment and wet etch method leads to a higher saturation capacitance and a negative V_{th} shift.[21] The V_{th} shift and *C*–*V* hysteresis caused by defective charges can be distinctly viewed. The voltage hysteresis is defined as ΔV_1 for each sweep, which is caused by the trapping effect of interface traps. ΔV_2 represents the entire positive shift of backward sweep *C*–*V* curves with an increase in V_p compared to the initial V_p of 6 V. This voltage shift induced by border trapping is cumulative because of the very large de-trapping time constant.[16]

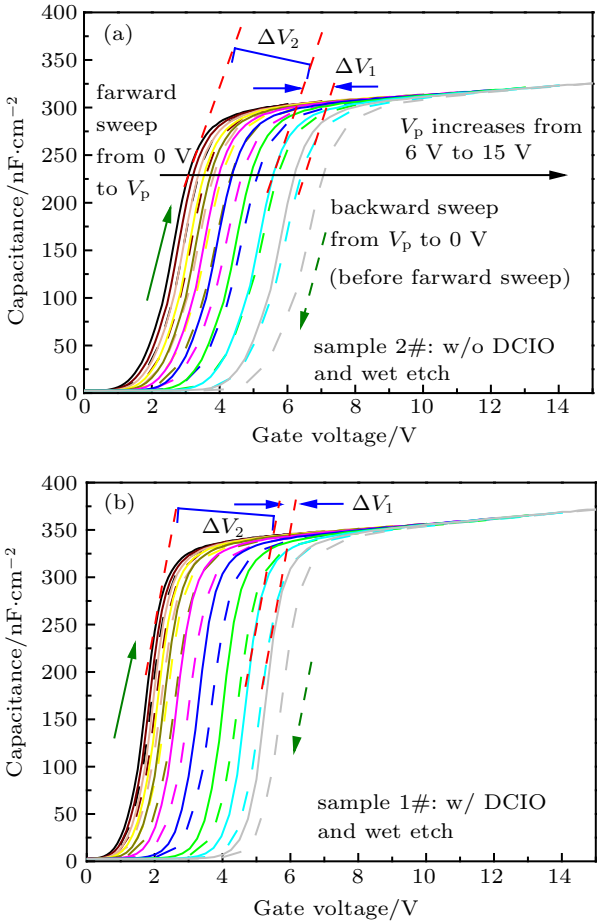

Fig. 4. Sequential *C*–*V* hysteresis curves of Al_2O_3/AlGaN/GaN MOS-HEMTs (a) without and (b) with DCIO treatment and wet etch.

Figure 5 shows the voltage shift extracted for *C*–*V* hysteresis sweeps with program voltage ranging from 6 V to 15 V. The trap density can be calculated by the following equation:

$$N_T = \frac{C_{OX}\Delta V}{q}, \tag{1}$$

where N_T is the density of interface or border traps, ΔV is the voltage shift, and q is the magnitude of electronic charge. The capacitance of Al_2O_3 gate dielectric for samples 2# and 1# are 330 nF/cm^2 and 363 nF/cm^2. With program voltage above

11 V, the density of detected interface traps tends to be saturated. The density of total interface traps for samples 2# and 1# is estimated to be 1.54×10^{12} cm^{-2} and 1.13×10^{12} cm^{-2}, leading to a voltage hysteresis by 0.75 V and 0.5 V, respectively. The decrease in trap density by 27% for devices with DCIO treatment and wet etch makes contribution to the remarkable increase in output current and transconductance. The density of border traps for samples 2# and 1# is estimated to be 7.73×10^{12} cm^{-2} and 6.35×10^{12} cm^{-2} with program voltage of 15 V, resulting in a cumulative voltage shift by 3.75 V and 2.8 V, respectively. The border traps are reduced by 14% with DCIO treatment and wet etch.

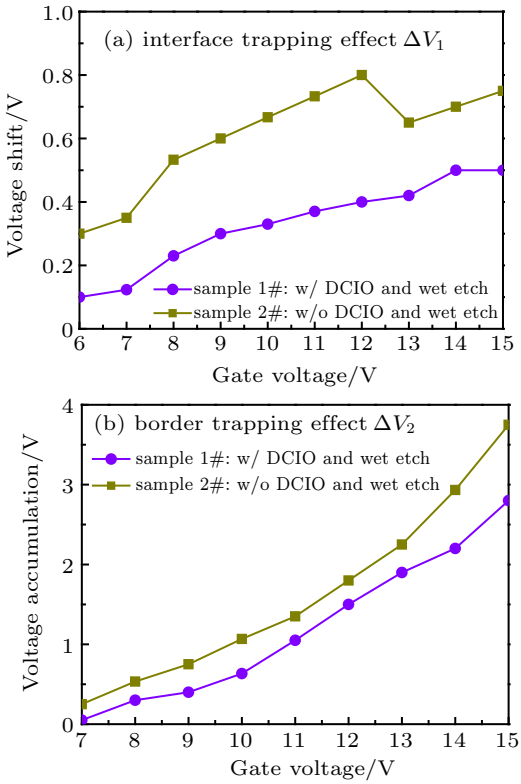

Fig. 5. Voltage shift due to (a) interface traps and (b) border traps as a function of program voltage for normally-off Al_2O_3/AlGaN/GaN MOS-HEMTs.

To activate the de-trapping of border traps with very large time constant, photo-assisted *C*–*V* measurement was carried out. Figure 6 shows the *C*–*V* characteristics of normally-off MOS-HEMTs before and after light illumination. The reference *C*–*V* curve (black curve) is firstly given under dark condition. With gate voltage swept from 0 V to 8 V, the electrons will be captured by border traps. Then the second sweep under dark condition gives *C*–*V* curves (gray curves) after filling of border traps. For photo-assisted *C*–*V* measurement, the devices are illuminated by monochromatic light for 60 s to enhance the electron emission from border traps, following which the *C*–*V* curve is swept from 0 V to 8 V immediately under dark condition. The photo-assisted *C*–*V* sweeps are repeated with wavelength of monochromatic light decreasing from 500 nm to 360 nm.

After light illumination with wavelength shorter than 400 nm, there is a significant negative voltage shift of *C*–*V* curves due to the de-trapping of border traps. With a decrease in wavelength, the higher photon energy causes a larger negative voltage shift. For sample 2# without DCIO treatment and wet etch, the voltage shift caused by photo-assisted de-trapping process increases from 0.06 V to 0.54 V with the wavelength decreases from 500 nm to 375 nm as shown in Fig. 6(a). For sample 1#, the voltage shift shows an increase from 0.05 V to 0.35 V. The photon energy (E), *i.e.*, activation energy of border traps (E_A), can be calculated using $E = h\nu$ where h is the Boltzmann's constant and ν is frequency of photon. With the activation energy ranging from 2.48 eV to 3.29 eV, the density of border traps contributing to voltage shift is 1.11×10^{12} cm^{-2} and 7.94×10^{11} cm^{-2} for samples 2# and 1#, respectively. Then, the *C*–*V* curves are further recorded under the wavelength of incident light varying from 400 nm to 360 nm with a step of 5 nm. As shown in Fig. 6(b), the most remarkable voltage shift appears at 375 nm of light illumination. This indicates that the major border traps have an activation energy about 3.29 eV.

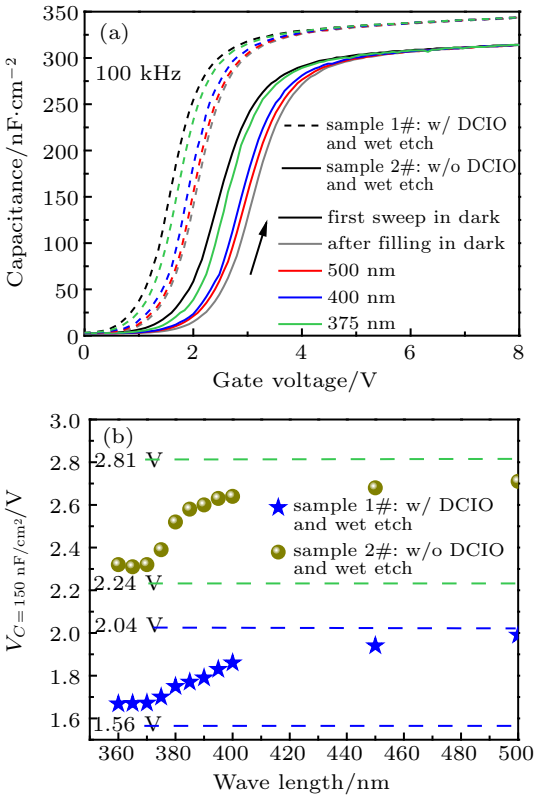

Fig. 6. (a) Typical photo-assisted *C*–*V* characteristics of normally-off MOS-HEMTs before and after light illumination with different wavelength. (b) Gate voltage at $C = 150$ nF/cm^2 as a function of wavelength varying from 500 nm to 360 nm. The lower and upper dashed lines for each device show the reference voltage level under dark before and after trap filling.

To obtain the trap distribution as activation energy, the state density of border traps with activation energy of E_A can be estimated by using the following equation:[29]

$$D_T(E = E_A) = \frac{C \cdot \Delta V}{q \cdot \Delta h\nu}, \tag{2}$$

where $\Delta h\nu$ is the energy difference determined from photon wavelength. Figure 7 shows the distribution of border traps in normally-off MOS-HEMTs. Sample 1# with DCIO and wet etch has a peak trap density $D_{\rm T}$ of 2.60×10^{12} cm^{-2}·eV^{-1} at the activation energy of 3.29 eV, and shows a sharp decrease by over one order of magnitude with larger or smaller activation energy. The improved post-etch surface treatment reduces border trap density by about half with little effect on the activation energy.

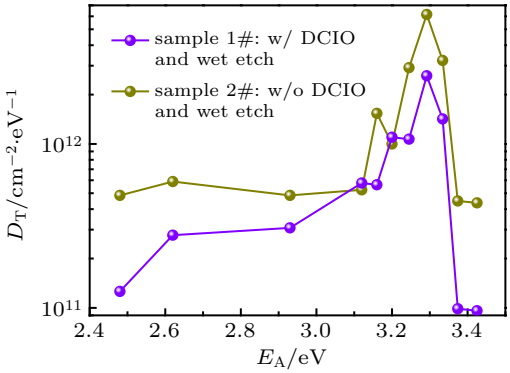

Fig. 7. State density distribution of border traps in normally-off MOS-HEMTs with and without DCIO treatment and wet etch.

4. Conclusions

In conclusion, interface issue of normally-off recess-gate Al_2O_3/AlGaN/GaN MOS-HEMTs with different post-etch surface treatment was investigated using hysteresis *C*–*V* and photo-assisted *C*–*V* method. DCIO and wet etch process results in a decrease in interface and border traps by 27% and 14%, respectively, leading to the improved device performance. Photo-assisted *C*–*V* reveals that both samples with different post-etch surface treatment have the similar distribution of border traps, showing peak state density at activation energy of 3.29 eV. The peak border trap density for sample with DCIO and wet etch is 2.60×10^{12} cm^{-2}·eV^{-1}, reduced by half compared with the controlled sample.

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