OPEN ACCESS
JOURNAL OF ADVANCED DIELECTRICS
Vol. 11, No. 1 (2021) 2150004 (8 pages)
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DOI: 10.1142/S2010135X21500041

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# Ultralow switching voltage and power consumption of $GeS_2$ thin film resistive switching memory

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Received 21 July 2020; Revised 31 December 2020; Accepted 19 January 2021; Published 10 February 2021

The coming Big Data Era requires progress in storage and computing technologies. As an emerging memory technology, Resistive RAM (RRAM) has shown its potential in the next generation high-density storage and neuromorphic computing applications, which extremely demand low switching voltage and power consumption. In this work, a 10 nm-thick amorphous $GeS_2$ thin film was utilized as the functional layer of RRAM in a combination with Ag and Pt electrodes. The structure and memory performance of the $GeS_2$-based RRAM device was characterized — it presents high on/off ratio, fast switching time, ultralow switching voltage (0.15 V) and power consumption (1.0 pJ and 0.56 pJ for PROGRAM and ERASE operations, respectively). We attribute these competitive memory characteristics to Ag doping phenomena and subsequent formation of Ag nano-islands in the functional layer that occurs due to diffusion of Ag from electrode into the $GeS_2$ thin film. These properties enable applications of $GeS_2$ for low energy RRAM device.

*Keywords*: $GeS_2$; conductive bridge memory; thin film; resistive switching memory.

## 1. Introduction

Resistive RAM (RRAM)[1–3] has been known for decades as a potential substitution of traditional memories such as flash memory and Dynamic Random Access Memory (DRAM). Despite the advantages that flash memory and DRAM possess, they have particular limitations. Flash memory is nonvolatile (it stores the data when the power is off), but its operational speed is low. By contrast, DRAM possesses high operational speed, but it loses the data as soon as the power is turned off. Although RRAM possesses high operational speed and nonvolatile property simultaneously, it is preferable to consider it not as the replacement for flash memory and DRAM, but as complementary memory that can fill in the performance gap in between. In particular, RRAM can find its place in embedded memory applications such as wearable electronics and Internet of Things devices where the low switching voltage and power consumption are the most essential requirements.

A RRAM device is a capacitor-like structure that consists of two electrodes and a dielectric layer sandwiched in between. While in flash memory and DRAM 0s and 1s are stored as the electric charge, in RRAM the data is recorded as the resistance of the memory cell. The working principle of a RRAM device is based on formation and rupture of conductive filament (CF) within the dielectric media under voltage applied between the two electrodes.[4] Although the idea of RRAM sounds simple, its wide commercialization cannot occur until some particular challenges are overcome. Many research groups have been working on the improvement of important memory characteristics, such as data retention and endurance, by trying different material combinations. Basically, in terms of the materials used for a device fabrication, there are mainly two types of RRAMs — oxygen vacancy RRAM that is also known as OxRAM[5] and conductive bridge RRAM also known as CBRAM.[6,7] While the structures of OxRAM and CBRAM devices are similar, their working principle is slightly different. In OxRAM, the dielectric media is typically a metal oxide material,[8] and when the voltage is applied to the device, oxygen ions from the oxide layer move towards one of the electrodes that is chosen to have a high oxygen accommodation capability. Thus, in OxRAM a CF is formed with oxygen vacancies, while for CBRAM it is metallic.

Typically, for CBRAM the metal is chosen to be either Cu or Ag and the dielectric media is a material family such as Cu or Ag ion conductors like halides (for example, AgI) or chalcogenides (for example, $As_xS$, $Ag_xS$, $Ge_xSe$, $Cu_xS$, $GeS_x$).[4,6,9,10] Ag and $GeS_2$ were the materials chosen for the first commercially available CBRAM realized in 2012. Since

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that time, a lot of works in practice and theory have been done with this material combination[11–13] as well as with the doped films known as $Ag_xGe_yS_z$ glasses. As it was reported, Ag dissolved in $GeS_2$ solid electrolyte is advantageous for achieving low switching voltage and power consumption.[6] There are many candidate materials for RRAM, among them $GeS_2$ is one of those that have great potential for real application in commercial devices due to its stable performance. In our work, we successfully achieved much lower switching voltage and low power consumption, which are lower than most reported work. Here, we report on our attempts towards further improvement of these essential memory characteristics and discovery of the mechanism behind.

## 2. Experiment

Commercial $Si/SiO_2$ substrates were used for the memory cell fabrication in which Pt layer deposited by e-beam evaporation acts as the bottom electrode with a thin adhesion layer of Ti underneath also deposited by e-beam evaporation. Then a thin functional layer of $GeS_2$ was deposited by pulsed-laser deposition technique at 150 °C substrate temperature for 2 min with $GeS_2$ target. The laser source used in the experiment is COHERENT Excimer laser at the wavelength of 248 nm, while the distance between the substrate and the target is 48 mm and the laser frequency is 1 Hz. The $GeS_2$ layer was deposited across the whole substrate with a small window left covered to ensure access of the probe to the bottom Pt electrode during the electrical characterization. Lastly, Ag top electrodes of a circular shape with the diameters varied from 50 $\mu$m to 500 $\mu$m were deposited by magnetron sputtering through a shadow mask. Unless specified, the size of the electrodes for the measured results is 100 $\mu$m.

Memory characteristic measurements were conducted in a commercial memristor characterization platform ArC ONE, and the switching time measurement was performed in a customized measurement set-up. During the measurements with ArC ONE, when a voltage is applied between the electrodes of the device, the current flowing through the device is measured and the resistance of the device is calculated. The voltage applied to the device in a form of pulses gradually changes from 0 V to $V_{max}$ positive, then from $V_{max}$ positive to $V_{max}$ negative and then from $V_{max}$ negative back to 0 V. $V_{max}$ positive is set to 0.25 V and $V_{max}$ negative is set to 0.75 V. The voltage step is set to 0.01 V, the step width is set to 50 ms and the inter-pulse time is set to 10 ms. No positive and negative current cut-off values are needed to be applied to prevent the device's breakdown since the maximum current that flows through the device is low and there is no dielectric breakdown happened. Memory characteristic measurements provide data showing the value of the memory window, the value of the current that flows through the device and the switching voltage of the device, i.e., resistance–voltage ($R$–$V$) and current–voltage ($I$–$V$) curves.

## 3. Results and Discussion

Scanning electron microscopy (SEM) examination of the top Ag electrodes was conducted to investigate their quality and actual geometry as shown in Fig. 1(a). One can see that the electrode's edge presents time-dependent diffusion

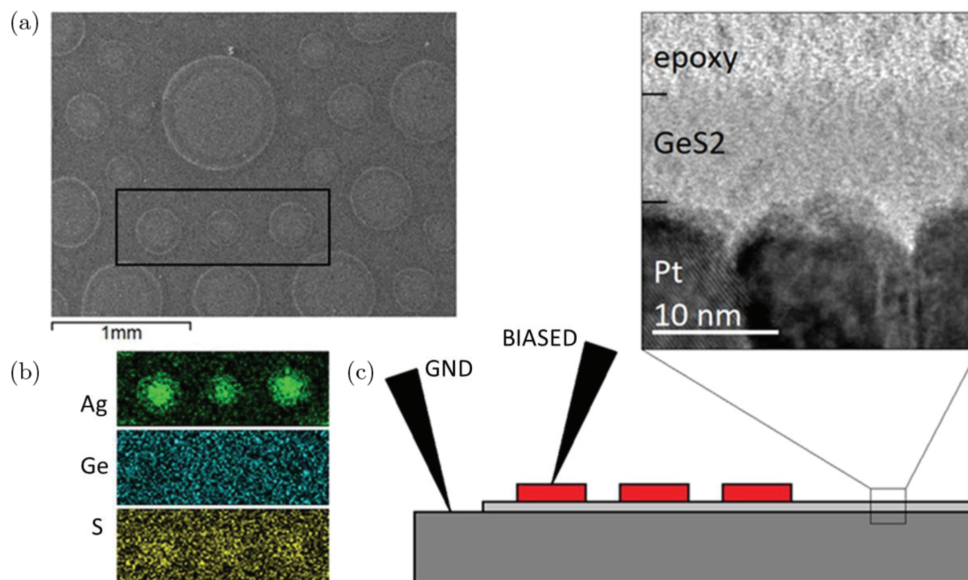
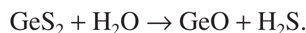



Fig. 1. (a) SEM image of the $GeS_2$ thin film with Ag top electrodes of different diameters. In the black box there are two electrodes of size 100 $\mu$m (left and right) and one electrode of size 70 $\mu$m (in the middle). (b) The EDX mapping represents distribution in the black box of Ag, Ge and S from top to bottom. (c) The diagram of the memory structure and cross-sectional TEM image of the $GeS_2$ thin film on Pt substrate.

pattern which suggests diffusion of Ag from electrode into the functional layer of the device. This was further proved by energy dispersive X-ray (EDX) analysis as shown in Fig. 1(b). A diffusion process of Ag into $GeS_2$ thin film might be attributed to photo-doping phenomena that was reported by Murakami and Wakaki[14] for identical materials combination and by Mitkova and Kozicki for a similar system of Ag/Ge–Se[15] — when the system is illuminated by light with the photon energy near or larger than the energy bandgap of a chalcogenide film, an anomalous diffusion process of Ag into the chalcogenide film can be observed. As it was found, the diffusion process saturates when the doping concentration reaches 24%.

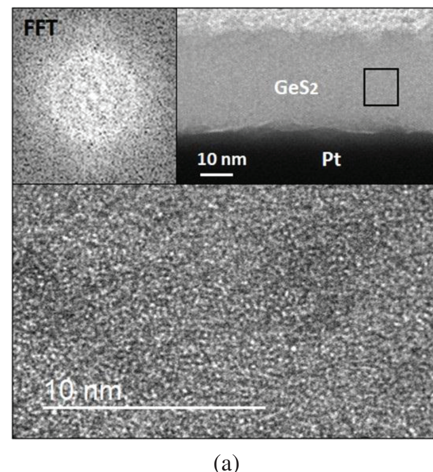
It is also interesting to notice that, while concentration of Ge is uniform, S mapping shows relatively higher concentration of S under Ag electrodes. It might be a sign of S accumulation in Ag-rich region due to Ag and S inter-diffusion. Conversely, as-deposited concentration of S under Ag electrodes might stay unchanged while relatively lower concentration of S that can be observed around Ag electrodes may take place due to hydrolysis reaction reported by Horton *et al.*[16] for $GeS_2$ thin film left in air — unprotected by Ag layer $GeS_2$ thin film turns into GeO while S loss takes place by $H_2S$ desorption, i.e.,



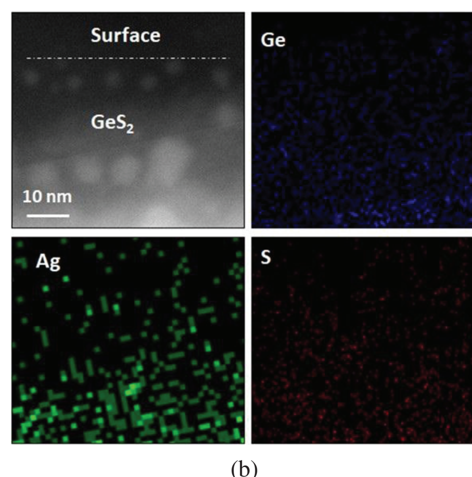
$$GeS_2 + H_2O \rightarrow GeO + H_2S.$$

Transmission electron microscopy (TEM) characterization of the sample was conducted to investigate the functional layer's crystal structure and thickness. The diagram of the memory structure as well as cross-sectional TEM image is shown in Fig. 1(c). As can be seen, the dielectric layer is amorphous in structure and its thickness is found to be around 10 nm. The bottom electrode of the device has a clear columnar structure that was achieved intentionally by adjustment of the deposition parameters. As it is known, the roughness of the electrode's surface leads to decreased switching voltage of the device, and this further leads to decreased power consumption which is essential for low energy applications.

Results of the detailed TEM analysis of a thicker $GeS_2$ thin film with Ag top electrodes are shown in Fig. 2, where one can see that the structure remains amorphous which is confirmed by fast Fourier Transform (FFT) diffraction pattern shown in Fig. 2(a). Figure 2(b) shows the STEM image where the bright nanodots are Ag-rich islands which are confirmed by element mapping of Ag. As reported by Sadovnikov and Gerasimov,[17] $Ag_2S$ may be formed due to the reaction of Ag and S; while for the detailed reaction process and phase formation between Ag electrode and $GeS_2$ film, more detailed study, especially *in situ* TEM characterization with applied electric field, is needed.




(a)




(b)

Fig. 2. (a) $GeS_2$ film showing amorphous structure illustrated by its FFT diffraction pattern. Ag nano-islands can be identified in the $GeS_2$ film. (b) STEM image of the film and elemental mapping of the film showing Ag-rich region.

### 3.1. *Resistive switching characteristics*

Figure 3(a) shows 10 consecutive *R–V* curves of the Ag/$GeS_2$/Pt memory cells. As can be seen, the device presents excellent switching uniformity, in low resistance state (LRS) the device's resistance goes down to around 100 Ω, while in high resistance state (HRS) it goes up to a few kΩ; this ensures the memory's on/off ratio in the range of 50. This is not a big memory window, but reasonable for the investigated thickness of the functional layer of the device equal to 10 nm. One can also find that the SET and RESET voltage values are both below 0.15 V which is a very low voltage for resistive switching to take place. Here, SET voltage is the voltage when the resistance of the device starts changing from HRS to LRS and RESET voltage is the voltage when the resistance of the device starts changing from LRS to HRS. The SET voltage and RESET voltage can also be understood as the threshold voltage values below which no change in the device's state occurs. The peaks in the *R–V* curve that in 0 V region can be attributed to the processing technique of the measurement data should be neglected. Figure 3(b) presents 10 consecutive *I–V* curves which are derived from the *R–V* curves for showing the current that

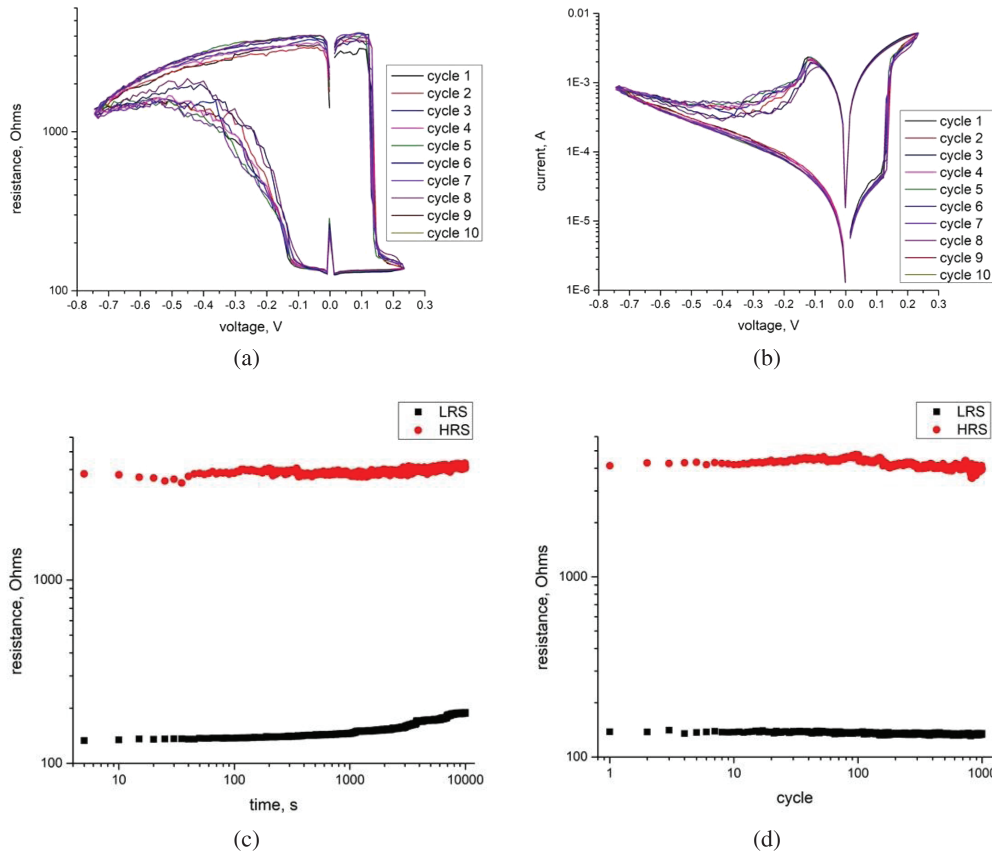



Fig. 3. (a) 10 consecutive *R–V* curves, (b) 10 consecutive *I–V* curves, (c) retention and (d) endurance of the memory cell.

flows through the device in LRS and HRS. The retention and endurance properties of the memory cells were also measured and the results are shown in Figs. 3(c) and 3(d), respectively. One can see that the endurance of this Ag/$GeS_2$/Pt memory structure is very good within the investigated region of 1000 cycles, and the retention is also very good within the investigated time period of 10,000 s with a slight degradation of LRS of the device at the end which may be attributed to accumulated disturbance of the resistance state by the resistance state reading pulses.

Electrode size dependence of HRS and LRS from 100 $\mu$m to 500 $\mu$m was also studied under the same experimental conditions, and the results are shown in Fig. 4(a). As can be seen from the linear fitting curve, LRS of the devices does not depend on the size due to compliance current setting, but HRS of the devices is higher for smaller electrodes, leading to larger memory window. It has been reported that smaller electrodes usually generate smaller CF and smaller resistive switching devices show lower current in HRS. Our results are in good agreement with this theory. However, one may notice that the resistance of each cells with the same size of electrode fluctuates a lot; this poor cell-to-cell uniformity is attributed to microscopic nonuniformity of the film.

### 3.2. *Switching mechanism and switching time*

Based on the electrode materials and the polarity of the operational voltage, we believe that the device is based on the formation and rupture of CF within the dielectric layer under voltage applied between the electrodes,[18–20] and Fig. 5

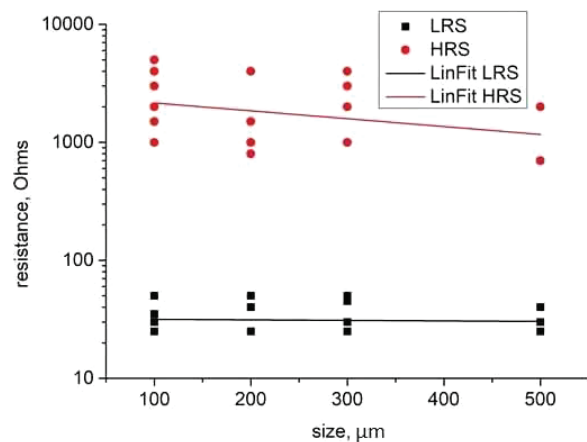



Fig. 4. Dependence of LRS and HRS of the device on the size of electrodes.

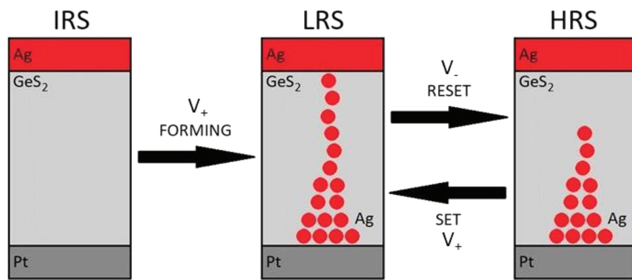



Fig. 5. Illustration of switching schematics of the memory cell.

illustrates this switching process. During the electrical characterization, Pt bottom electrode is kept grounded while potential of either positive or negative polarity is applied to Ag top electrode. When a positive voltage is applied to the Ag electrode which plays a role of the anode, it is expected that its composing atoms undergo a vulcanization reaction and dissolve into $GeS_2$ solid electrolyte. Under electric field driven, the dissolved ions migrate toward the Pt electrode (plays a role of the cathode) where they reduce; this electrochemical process eventually leads to the formation of a highly conductive metallic filament that can bridge the electrodes, and the memory cell is switched into the LRS (or ON state). The process is known as SET or PROGRAM operation. When the applied voltage is reversed, the metallic filament is ruptured and the device resumes to the HRS (or OFF state); this process is known as RESET or ERASE operation. The very first switching of the device from the initial resistance state (IRS) to LRS is called FORMING operation which occurs only once, and after the forming process, the device only switches between LRS and HRS. For our investigated devices, however, there is no difference found between IRS and HRS as well as between FORMING voltage and SET voltage. Therefore, we claim that the device is forming-free which may be attributed to the diffusion of Ag into the dielectric layer.

During switching time measurements conducted with the customized measurement setup, a memory device is connected in series with a reference resistor. The measurement setup is presented in Fig. 6(a) which is identical to the one reported by Onlaor *et al.*[21] and consists of a pulse generator and an oscilloscope. The oscilloscope is connected through its two channels to the device and to the pulse generator. The signal from the reference resistor is not measured, but it can be found as the difference between the voltage from the pulse generator and the voltage across the device. During the measurements, a square wave with amplitude of 0.5 V and duty time of 50% is applied to the device, and an optimal value of 2.2 kΩ of the reference resistor is chosen. The switching time measurements provide data on the switching time of the device and demonstrate the switching dynamics of SET and RESET processes.

Typically, during the switching time measurements, besides SET and RESET processes, two distinct HRS and

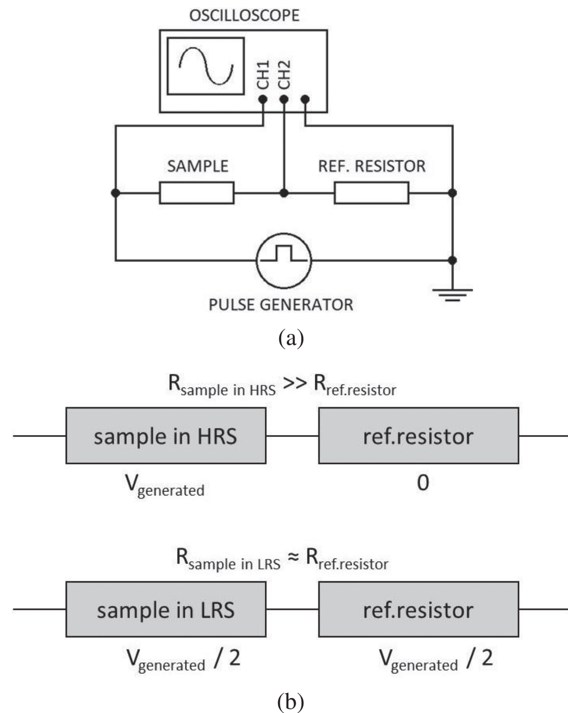



Fig. 6. (a) The setup of the switching time measurement. (b) The diagram of the resistance state and voltage distribution during the measurement.

LRS states of the system can be observed; while the resistance of the reference resistor is a constant. The two states are depicted in Fig. 6(b) as the higher and lower diagram, respectively. When the device is in HRS, its resistance is much higher than the reference resistor and the device carries nearly all the voltage generated by the pulse generator; when the device is in LRS, its resistance is similar to the resistance of reference resistor and they nearly equally share the voltage generated by the pulse generator.

Figure 7(a) demonstrates an example of the measurement data where the frequency of the applied square wave is 10 kHz corresponding to a period of 100 $\mu$s. When the positive and negative voltages are applied to the device, the two distinct LRS and HRS states of the system can be clearly seen. Figure 7(b) illustrates the schematics of the measurement data for stressing the regions where SET and RESET processes occur. The shape of the curve representing the voltage across the sample is derived from the experimental data that follows.

As it is mentioned above, when a positive voltage is applied, the device is in LRS; and when a negative voltage is applied, the device is in HRS. The transition from HRS to LRS (SET process) occurs when the polarity of the applied voltage changes from negative to positive, and the transition from LRS to HRS (RESET process) occurs when the polarity of the applied voltage changes from positive to negative. The enlarged areas in Fig. 7(a) where SET and

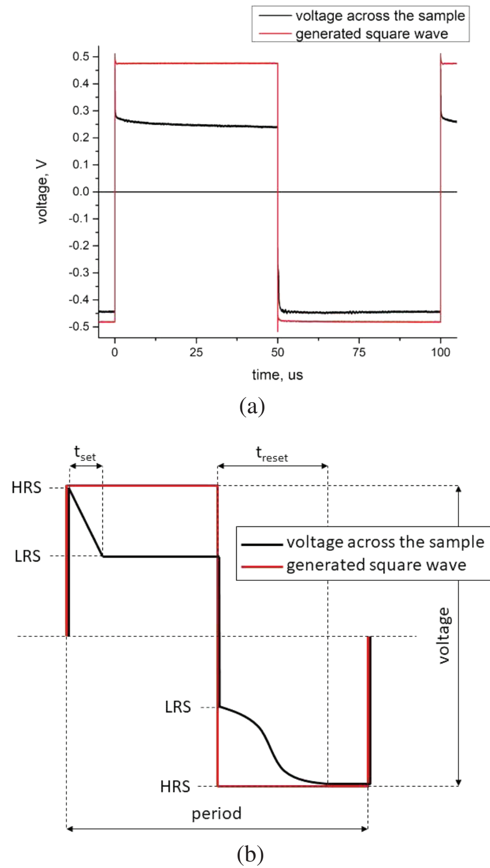



Fig. 7. (a) An example of the measurement data. (b) Schematics of the measurement data.

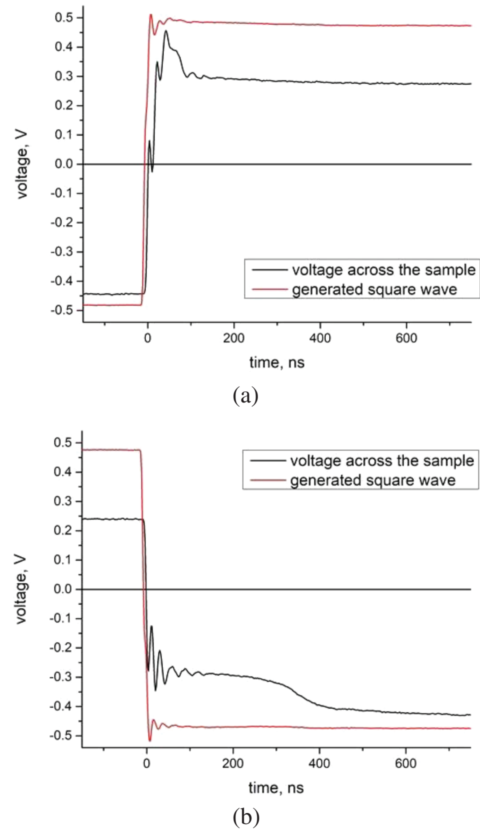



Fig. 8. (a) Enlarged area of SET process. (b) Enlarged area of RESET process.

RESET processes occur are shown in Figs. 8(a) and 8(b), respectively. For this particular case, when the frequency of the applied square wave is 10 kHz, the SET time can be estimated to be around 100 ns and RESET time can be estimated to be around 350 ns. It should be pointed out that the SET and RESET time values depend on the frequency of the applied square wave — for lower frequencies the switching time is longer and for higher frequencies the switching time is shorter. However, the memory window also depends on the frequency. Thus, it is always a compromise between full but slower switching of the device at lower frequencies and faster but partial switching at higher frequencies. For switching energy calculation, the shortest switching time achieved for the investigated device (40 ns and 80 ns for SET and RESET processes, respectively) will be used to estimate its potential.

Based on the results shown in Fig. 8, it is interesting to see that the RESET process always takes longer time than the SET process. The difference between SET time and RESET time can be caused by the difference of CF formation and rupture mechanisms. The SET process might be faster due to CF formation all-at-once, but RESET process is slower due to CF rupture atom-by-atom that obviously takes more time compared to the process of all-at-once. This explanation can be further supported by the shape of SET and RESET processes. As can be seen from Fig. 8, as well as from the shape of $R$–$V$ curves presented in Fig. 3(a) and $I$–$V$ curves presented in Fig. 3(b), the SET process is sharp that can also be attributed to CF formation all-at-once; and RESET process is gradual that can also be attributed to CF rupture atom-by-atom. Different SET and RESET time values for low-voltage region were reported for $GeS_2$ memory cells and were also attributed to different switching dynamics of CF formation and rupture mechanisms.[22–24]

### 3.3. *Switching energy calculation*

Figure 9 shows voltage across the reference resistor and the current as well as power dissipated on the sample. The voltage across the reference resistor $U_{ref}$ (presented in Fig. 9(a)) can be found as the difference between the voltage generated by the pulse generator $U_{gen}$ and the voltage across the sample $U_{sam}$ (presented in Fig. 7(a)) as follows:

$$U_{ref} = U_{gen} - U_{sam}.$$

When the voltage across the reference resistor with $R_{ref} = 2.2\ k\Omega$ is calculated, the current $I$ that flows through

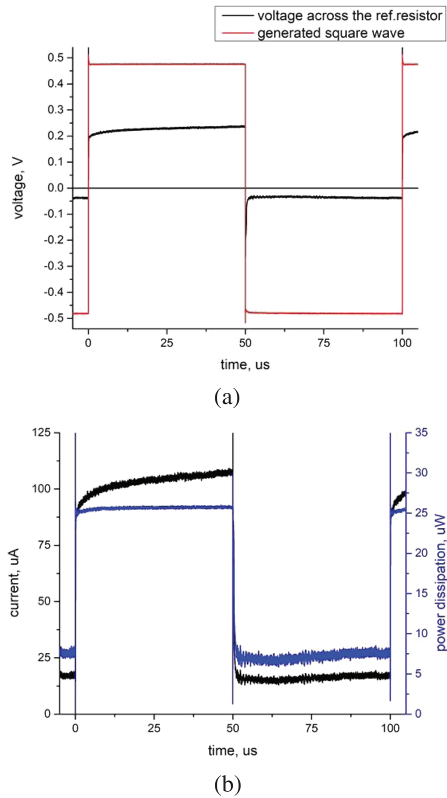



Fig. 9. (a) Voltage across the reference resistor. (b) Current that flows through the system and power dissipated on the sample.

the reference resistor and sample can be found by Ohm's law as follows:

$$I = \frac{U_{\text{ref}}}{R_{\text{ref}}}.$$

Multiplication of the voltage across the sample $U_{\text{sam}}$ and the current $I$ results in the power dissipated on the sample $P_{\text{diss}}$ (shown in Fig. 9(b)):

$$P_{\text{diss}} = U_{\text{sam}} * I.$$

As can be seen from Fig. 9(b), power dissipation on the sample during positive voltage application ($P_{\text{SET}}$) is equal to 25 $\mu$W, while power dissipation on the sample during negative voltage application ($P_{\text{RESET}}$) is equal to 7 $\mu$W. As the SET and RESET time values are both known (40 ns and 80 ns, respectively), SET and RESET energy can be found as the product of the power dissipated on the sample and the switching time:

$$E_{\text{SET}} = P_{\text{SET}} * t_{\text{SET}} \text{ and } E_{\text{RESET}} = P_{\text{RESET}} * t_{\text{RESET}}.$$

Based on this equation, the SET energy is calculated to be 1.0 pJ and the RESET energy is calculated to be 0.56 pJ.

## 4. Conclusion

In this work, we utilized a 10 nm-thick amorphous $GeS_2$ thin film as the functional layer of RRAM in a combination with Ag and Pt electrodes and investigated the structure and memory performance of the $GeS_2$-based RRAM device. The results revealed high on/off ratio, fast switching time, ultralow switching voltage (0.15 V) and power consumption (1.0 pJ and 0.56 pJ for PROGRAM and ERASE operations, respectively). These competitive memory characteristics were attributed to Ag doping phenomena and subsequent formation of Ag nano-islands in the functional layer that occurs due to diffusion of Ag from electrode into the $GeS_2$ thin film. These properties make $GeS_2$-based RRAM suitable for low energy memory applications.

## Acknowledgments

This work was supported by the NSFC/RGC Joint Research Scheme (Grant No. N-PolyU15300619), The Hong Kong Polytechnic University Strategic Development Special Project (Grant No. 1-ZVGH) and internal grant (Grant No. G-UAEZ). N.L. is also grateful for the financial support from the Hong Kong PhD fellowship scheme.

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