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A novel one-time-programmable memory unit based on Schottky-type p-GaN diode

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Abstract: In this work, a novel one-time-programmable memory unit based on a Schottky-type p-GaN diode is proposed. During the programming process, the junction switches from a high-resistance state to a low-resistance state through Schottky junction breakdown, and the state is permanently preserved. The memory unit features a current ratio of more than 10^3, a read voltage window of 6 V, a programming time of less than 10^{-4} s, a stability of more than 10^8 read cycles, and a lifetime of far more than 10 years. Besides, the fabrication of the device is fully compatible with commercial Si-based GaN process platforms, which is of great significance for the realization of low-cost read-only memory in all-GaN integration.

Key words: wide-bandgap semiconductor; one-time programmable; Schottky-type p-GaN diode; read-only memory device

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1. Introduction

Gallium nitride (GaN)-based devices have gained considerable recognition in the field of power electronics, owing to their remarkable attributes such as high electron mobility, high electron saturation drift velocity, and high breakdown electric field[1, 2]. Presently, commercial silicon-based GaN platforms have successfully integrated various electrical components like capacitors, resistors, diodes, and enhancement/depletion (E/D) mode high electron mobility transistors (HEMTs)[3, 4]. However, research on on-chip memory devices remains limited, which is crucial for improving the performance, power efficiency, security, and reliability of all-GaN integrated circuits. It has been reported that some non-volatile memory (NVM) cells use the fast-trap/slowly-detrap of carriers as program/erase behavior of the information[5, 6], some resistive random access memory (RRAM) devices use the switching of high/low resistance state (HRS/LRS) after soft breakdown as a set/reset process[7]. Additionally, static random-access memory (SRAM) arrays have been achieved through the integration of highly uniform E/D mode GaN devices[8]. However, these technologies are either difficult to compatible with the existing GaN process, or are too complex and cost-prohibitive, which limits their large-scale application. The anti-fuse one-time-programmable (OTP) memory device, emerges as a cost-effective read-only memory (ROM), making it an invaluable component in applications emphasizing data security, firmware or configuration storage, and resistance to tampering.

Fortunately, the circuit model of the Schottky-type p-GaN diode (metal/p-GaN/AlGaN/GaN stack)[9], is very similar to the diode-based OTP unit in Si complementary metal-oxide semiconductor (CMOS) technology[10–12]. Thus, for the first time, a p-GaN diode-based anti-fuse OTP device that switches from HRS to LRS by controlling Schottky junction breakdown, is presented in this letter. Besides, p-GaN diode-based OTP devices are fully compatible with commercial p-GaN processes and can achieve high integration at low cost. Furthermore, the unique properties of p-GaN diodes, including their inherent stability, high thermal conductivity, and resistance to harsh environmental conditions, make them an intriguing candidate for OTP memory technology[13].

2. Device fabrication and operation mechanism

In this study, the p-GaN heterostructure is deposited on a 6-inch Si substrate, comprising a GaN buffer layer, a 200 nm unintentionally doped (UID) GaN layer, a 15 nm $Al_{0.22}Ga_{0.78}N$ barrier layer, and a 70 nm p-GaN layer with Mg doping concentration of 3×10^{19} cm^{-3}. The fabrication of the Schottky-type p-GaN gate HEMTs aligns with our previous work[14], as shown in Fig.1, starting with the formation of the p-GaN gate by two-step etching process (a rapid Cl_2/BCl_3-based inductively coupled plasma-etching and a high-selectivity, low-damage self-stopping ICP etching based on $Cl_2/N_2/O_2$), followed by Ti/Al/Ni/Au (20/150/55/45 nm) source/drain Ohmic contacts evaporation. The passivation layer consists of 3 nm atomic layer deposition (ALD)-Al_2O_3 and 200 nm plasma-enhanced chemical vapor deposition (PECVD)-SiO_2. The schematic and the physical image of the fabricated HEMT is depicted in Figs. 2(a) and 2(b), respectively. Devices feature a gate length/width (L_G/W_G) of 4/100 μm and a gate-source/drain separation (L_{GS}/L_{GD}) of 4/4 μm. Fig. 2(c) shows the double-sweep I_D–V_G characteristic and the I_G–V_G curve of the HEMT measured at a V_{DS} of 1 V, the device exhibits a threshold voltage (V_{TH}) of approximately 1 V, confirming the normal electrical characteristics.

The gate region of the Schottky-type p-GaN gate HEMT can be equivalently represented as a series of a Schottky bar-

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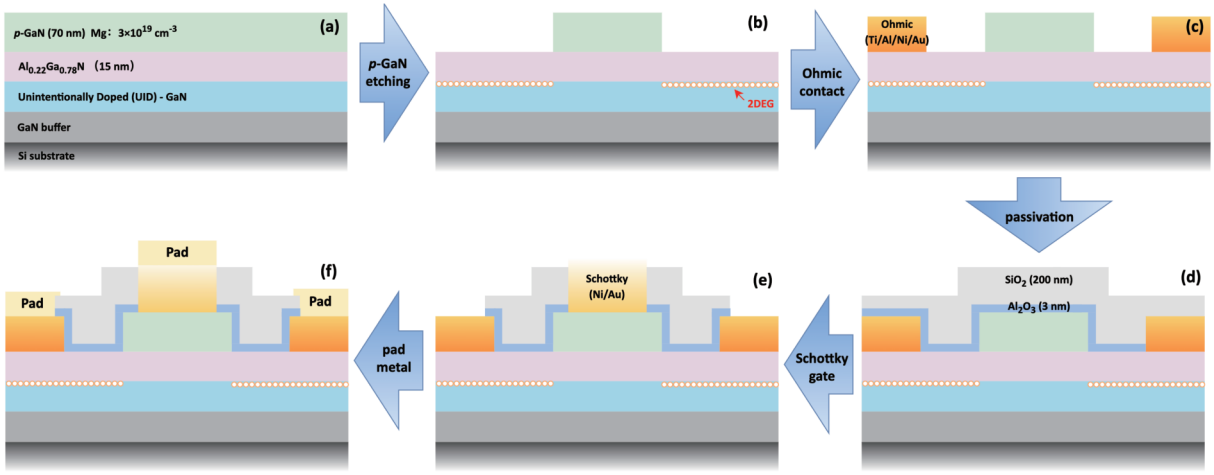

Fig. 1. (Color online) Schematic diagram of the process flow of the Schottky-type p-GaN HEMT.

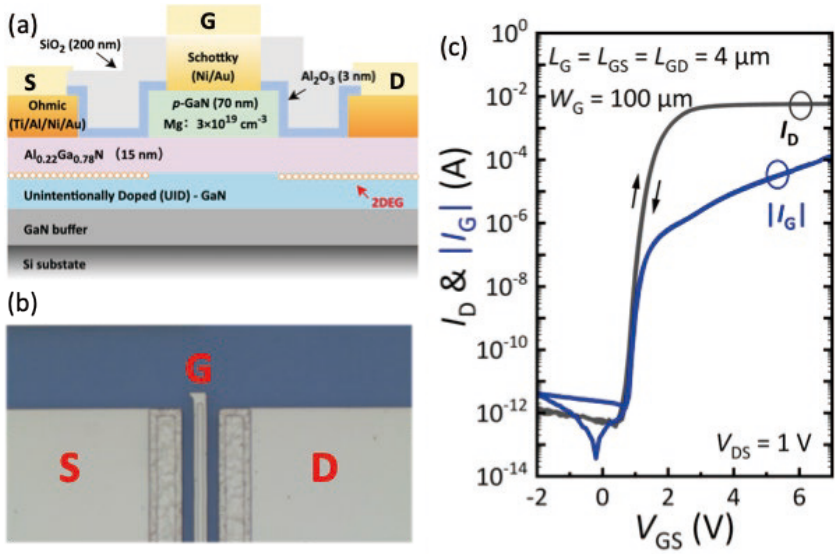

Fig. 2. (Color online) (a) Schematic structure of the Schottky-type p-GaN gate AlGaN/GaN HEMTs. (b) Physical image of the devices under the optical microscope. (c) Double-sweep I_D–V_G characteristic (black) and the I_G–V_G curve (blue) of the HEMT measured at a V_{DS} of 1 V.

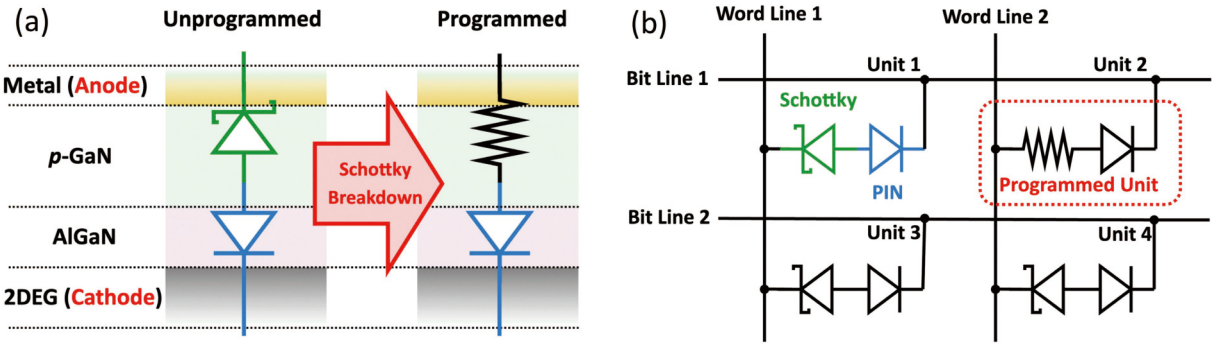

Fig. 3. (Color online) (a) Programming process of the Schottky-type p-GaN diode-based OTP device. (b) The schematic of a 2 × 2 OTP array.

rier diode (SBD) and a PIN diode[9], as illustrated in Fig. 3(a). When the source and drain of the HEMT are shorted, the gate and 2DEG channel can be regarded as the anode and cathode of a diode, respectively (this study aims to verify the feasibility of p-GaN diodes in OTP arrays, and the junction area is approximately 400 μm^2; for practical OTP arrays, reducing the junction area is required to achieve high integration). When a large programming voltage ($V_{program}$) is applied to the anode, the capacitive voltage divider relationship determines that most of the voltage drops on the Schottky junction, leading to its degradation until catastrophic breakdown[15, 16]. At this point, the Schottky junction loses its rectification ability, transitioning from HRS to LRS, and becomes irrecoverable. This naturally forms an anti-fuse structure in the p-GaN system.

3. Performance of the OTP memory

To achieve integration, multiple diodes can be connected with the anodes to the word lines (WL) and the cath-

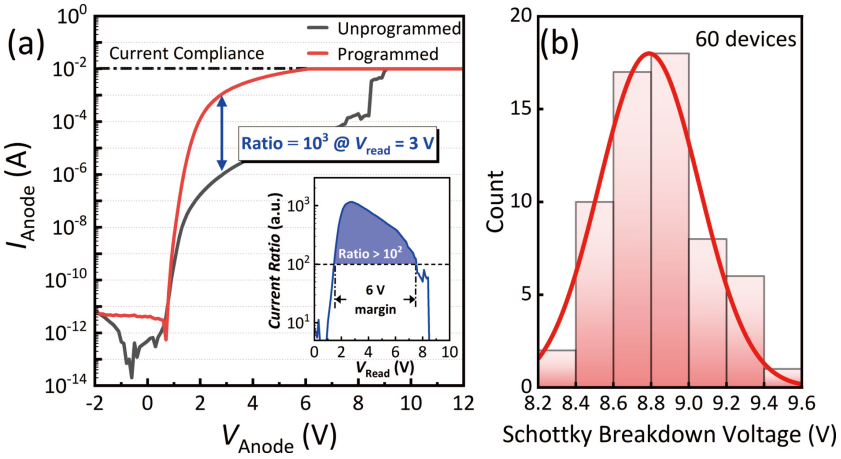

Fig. 4. (Color online) (a) Comparison of the anode current before and after programming (inset shows the read voltage margin). (b) Statistics of programming voltage for 60 devices.

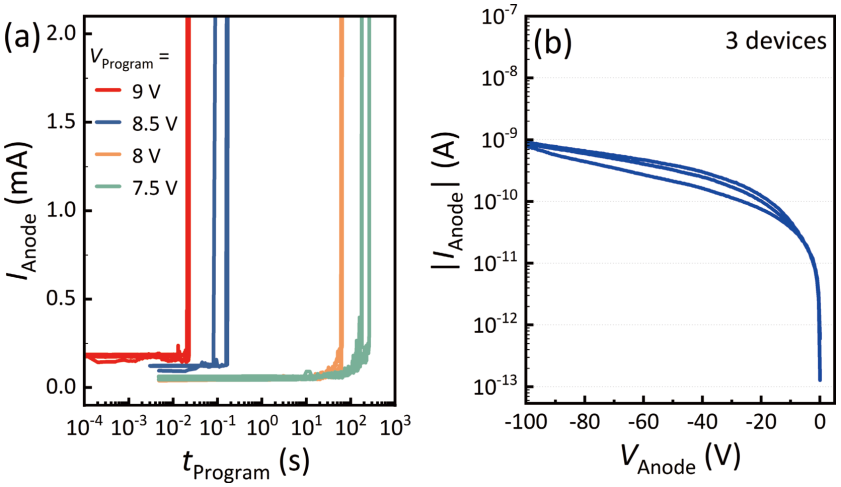

Fig. 5. (Color online) (a) Program time under different program voltages (three devices each) . (b) Breakdown characteristics of the PIN junction of the p-GaN diode.

odes to the bit lines (BL) to create an OTP storage array. Fig. 3(b) displays the schematic of a simplified 2 × 2 OTP array. During the programming of Unit 2, WL2 is pulled up to the $V_{program}$, while BL1 is grounded. A voltage of $V_{program}$–V_{PIN} drops on the Schottky junction, causing the degradation, where V_{PIN} is the forward turn-on voltage of the PIN junction. For read operations, a relatively small read voltage (V_{read}) is applied to WL2. The current through unprogrammed devices is small due to the reverse bias of the Schottky junction, while programmed devices exhibit a significant current as the PIN junction is turned on. Fig. 4(a) shows a comparison of the anode current before and after programming of the p-GaN diode-based OTP device. It is observed that the current ratio ($I_{A\_programmed}/I_{A\_unprogrammed}$) reaches up to 10^3 at V_{read} = 3 V, and the V_{read} window is approximately 6 V when the current ratio is larger than 10^2 (inset of Fig. 4(a)), which indicates that the OTP device provides a sufficient margin to avoid faulty reading. It is worth noting that selecting appropriate high work-function anode metals can increase the Schottky barrier, further reducing the current in unprogrammed devices and increasing the current ratio[17]. The programming voltage distribution of 60 OTP units is shown in Fig. 4(b), revealing a standard deviation of only 0.8 V, demonstrating strict control over programming conditions.

In practical applications, $V_{program}$ is often applied to OTP devices in the form of pulses, therefore, it requires the programming time ($t_{program}$) to align with the clock frequency of the circuit. Fig. 5(a) shows the temporal characteristics of the anode current at different programming voltages. As the $V_{program}$ increases from 7.5 to 9 V, the $t_{program}$ decreases from 10^2 to 10^{-2} s. Increasing the programming voltage can further reduce the programming time (when $V_{program}$ is 9.2 V, the $t_{program}$ is less than the device sampling resolution of 10^{-4} s).

During programming operations on Unit 2, BL2 is raised to $V_{program}$ simultaneously with WL2, while WL1 is grounded along with BL1 to prevent accidental programming of Unit 4 and Unit 1. In this case, Unit 3 requires a strong ability to withstand high reverse bias voltage. Fig. 5(b) illustrates the reverse breakdown characteristics of the PIN junction of the p-GaN diode. Even when the reverse bias voltage is increased to 100 V, the leakage current remains at the level of 10^{-9} A, indicating its reverse voltage blocking ability.

When performing read operations on programmed devices, the PIN junction is in a forward-biased state. Although a small read voltage could hardly induce any degradation of the PIN junction, we still evaluated the device's reliability during read operations, which is akin to retention time. Here, AC pulse signals of 3 and 6 V (pulse duty cycle of 50 %) are applied to the anode of the OTP device to simulate read pulses, respectively. After undergoing varying numbers of

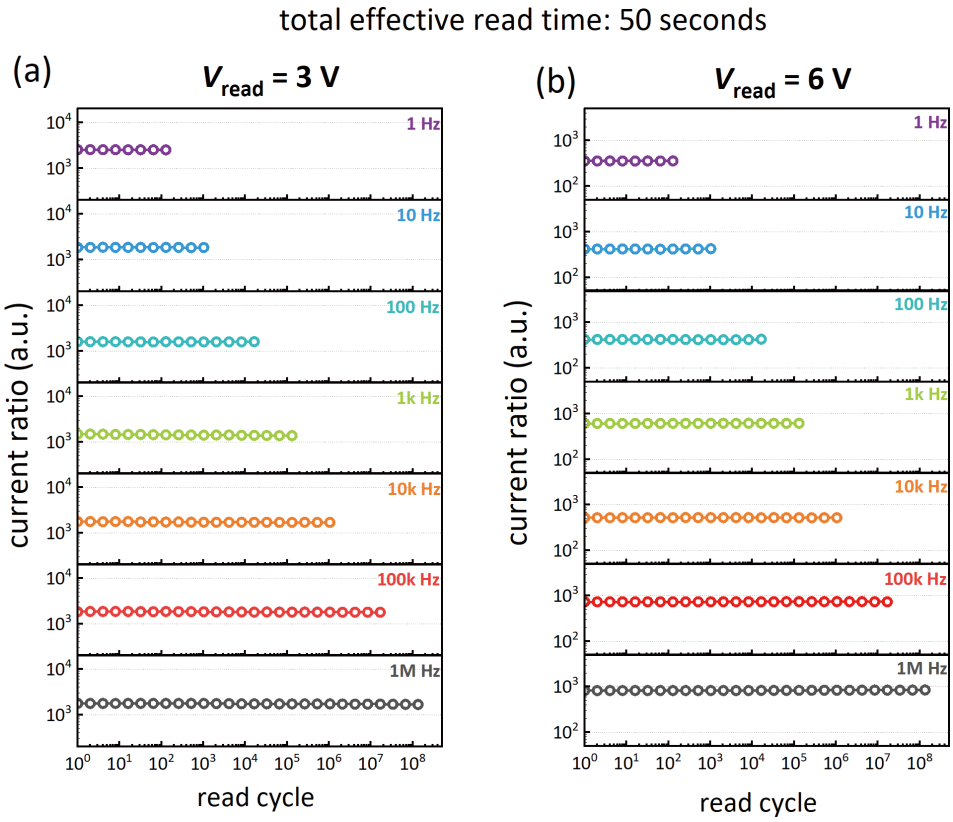

Fig. 6. (Color online) Current ratio after different read cycles at a read voltage of 3 V (a) and 6 V (b). Pulse frequency: 1 Hz to 1 MHz, pulse duty cycle: 50%.

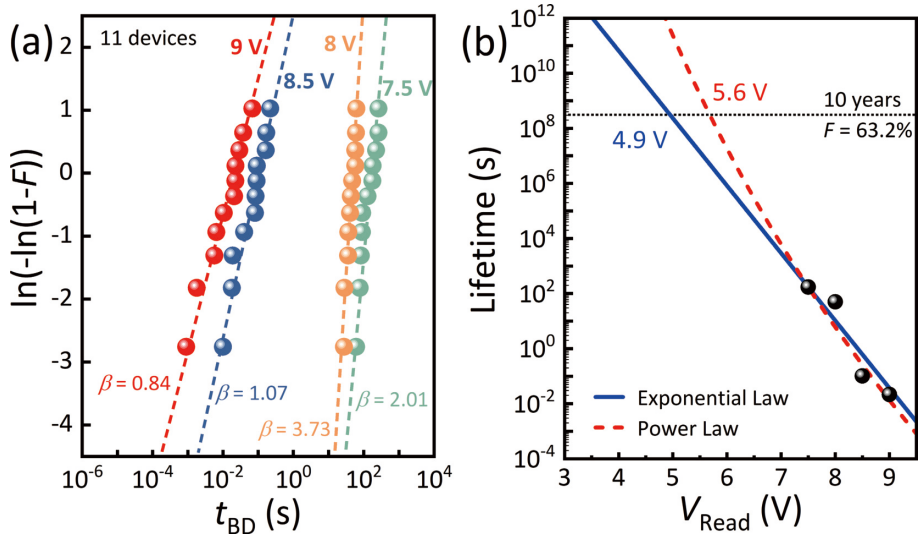

Fig. 7. (Color online) (a) Weibull distribution of the breakdown time of the Schottky junction in the p-GaN diode. (b)Reverse bias voltages for a 10-year lifetime extracted from exponential and power laws at a 63.2% failure rate.

read cycles, the current ratio is extracted, as shown in Fig. 6. At different pulse frequencies (from 1 Hz to 1 MHz), the pulse count is adjusted (from 10^2 to 10^8) to ensure the same effective read time of 50 s. The results indicate that even after 10^8 read cycles at V_{read} = 6 V, the current ratio of p-GaN diode-based OTP devices remains unchanged, demonstrating its stability during prolonged read operations.

During the reading operations of Unit 2, a small read voltage (about 3 V) is applied to WL2 as well. Though the V_{read} is much lower than the $V_{program}$, the Schottky junction of Unit 4 would remain in the reverse bias, posing a risk of unintended programming. Fig. 7(a) demonstrates that the breakdown time of the Schottky junction in the p-GaN diode follows a Weibull distribution, consistent with widely reported gate failure in p-GaN HEMTs[18–20]. At different reverse bias voltages, the shape parameter (β) of the Weibull distribution almost exceeds 1, indicating a significant reduction in externally triggered breakdown mechanisms associated with defects[15]. From exponential and power laws at a 63.2% failure rate, reverse bias voltages for a 10-year lifetime are estimated to be 4.9 and 5.6 V, respectively, as shown in Fig. 7(b). This ensures the reliability of the p-GaN diode-based OTP devices when operating at 3 V read voltage for a longer operation time.

4. Conclusion

In this work, a promising p-GaN diode-based OTP memory device for GaN-based power electronics is proposed. The performance of the OTP device covers a current ratio of more than 10^3, a read voltage window of 6 V, a programming time of less than 10^{-4} s, a strong reverse voltage blocking ability, a stability of more than 10^8 read cycles and a lifetime of over 10 years. Further works, such as improving noise margin, device scaling-down, and integration, are worth carrying out.

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