ARTICLES

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A 24–30 GHz 8-element dual-polarized 5G FR2 phased-array transceiver IC with 20.8-dBm TX OP1dB and 4.1-dB RX NF in 65-nm CMOS

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Abstract: This article presents an 8-element dual-polarized phased-array transceiver (TRX) front-end IC for millimeter-wave (mm-Wave) 5G new radio (NR). Power enhancement technologies for power amplifiers (PA) in mm-Wave 5G phased-array TRX are discussed. A four-stage wideband high-power class-AB PA with distributed-active-transformer (DAT) power combining and multi-stage second-harmonic traps is proposed, ensuring the mitigated amplitude-to-phase (AM-PM) distortions across wide carrier frequencies without degrading transmitting (TX) power, gain and efficiency. TX and receiving (RX) switching is achieved by a matching network co-designed on-chip T/R switch. In each TRX element, 6-bit 360° phase shifting and 6-bit 31.5-dB gain tuning are respectively achieved by the digital-controlled vector-modulated phase shifter (VMPS) and differential attenuator (ATT). Fabricated in 65-nm bulk complementary metal oxide semiconductor (CMOS), the proposed TRX demonstrates the measured peak TX/RX gains of 25.5/21.3 dB, covering the 24–29.5 GHz band. The measured peak TX OP1dB and power-added efficiency (PAE) are 20.8 dBm and 21.1%, respectively. The measured minimum RX NF is 4.1 dB. The TRX achieves an output power of 11.0–12.4 dBm and error vector magnitude (EVM) of 5% with 400-MHz 5G NR FR2 OFDM 64-QAM signals across 24–29.5 GHz, covering 3GPP 5G NR FR2 operating bands of n257, n258, and n261.

Key words: fifth-generation (5G); power amplifier; millimeter-wave; transceiver; phased-array

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1. Introduction

Silicon-based large-scale phased arrays are extensively deployed in millimeter-wave (mm-Wave) wireless communication networks to overcome the high path loss with a low cost[1–9]. With the enhanced effective isotropic radiated power (EIRP) and the improved array gain, the *N*-element phased-array transceivers (TRX) can compensate for the extra path loss of $10\log_{10}N$ dB and, thus, cover long communication distances. Nevertheless, the large-scale phased array faces growing challenges with the rapid development of mm-Wave 5G systems.

To increase throughput, 5G new radio (NR) networks adopt the broadband high-order modulated signals with improved spectral efficiency [e.g., orthogonal frequency division multiplexing (OFDM) 64-/256-quadrature amplitude modulation (QAM) signals]. The maximum bandwidth of a single carrier component (CC) is 400 MHz in frequency range 2 (FR2) networks[10]. With carrier aggregation (CA) techniques, the instantaneous bandwidth of the transmitted signal is up to 16 × 400 MHz. In these scenarios, the beam squint of the large-scale phased array at wide steering angles can be considerable.

At the center frequency f_0 of 26 GHz, Fig. 1(a) depicts the beam deviation across different pointed angles of a phased array. The normalized frequencies f/f_0 of 0.94–1.06 in Fig.1(a) correspond to the maximum signal bandwidth of about 3 GHz. As shown in Fig. 1(a), the phased array with a broadband 5G NR FR2 signal will lead to a severe beam squint of up to ±5° at large angles. Fig. 1(b) depicts the −1-dB and −3-dB beamwidths of the $N \times N$ uniform rectangular array (URA), showing that the −1-dB and −3-dB beamwidths of a 256-URA are less than 4° and 6°, respectively. According to Fig. 1(a) and Fig. 1(b), in the 5G NR FR2 scenario, the beamwidth of a large-scale phased array is comparable with a beam squint at wide steering angles. It leads to significant degradation of TX effective isotropic radiated power (EIRP) and RX gain. Besides, the narrow beamwidth results in the poor single-beam coverage of the large-scale phased array, increasing the design complexity and the implementation cost of the beam control circuits. For these reasons, the advantages of the phased array disappear as the number of elements increases. This motivates the research efforts on high-power, low-cost phased-array transceiver ICs, which can boost the EIRP without increasing the array element. For instance, according to the Friis transmission equation, for a given array size and receiving power, a phased-array

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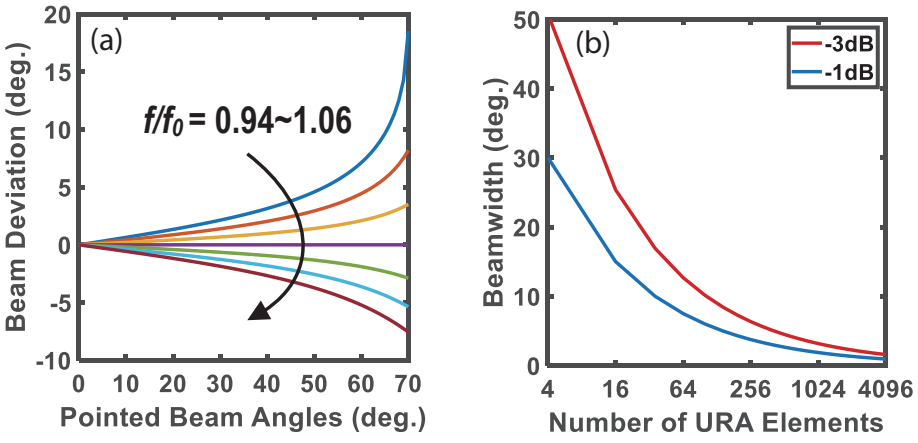

Fig. 1. (Color online) (a) Beam squint of the phased array across different pointed beam angles and (b) −1-dB and −3-dB beamwidth of URA with respect to the number of elements.

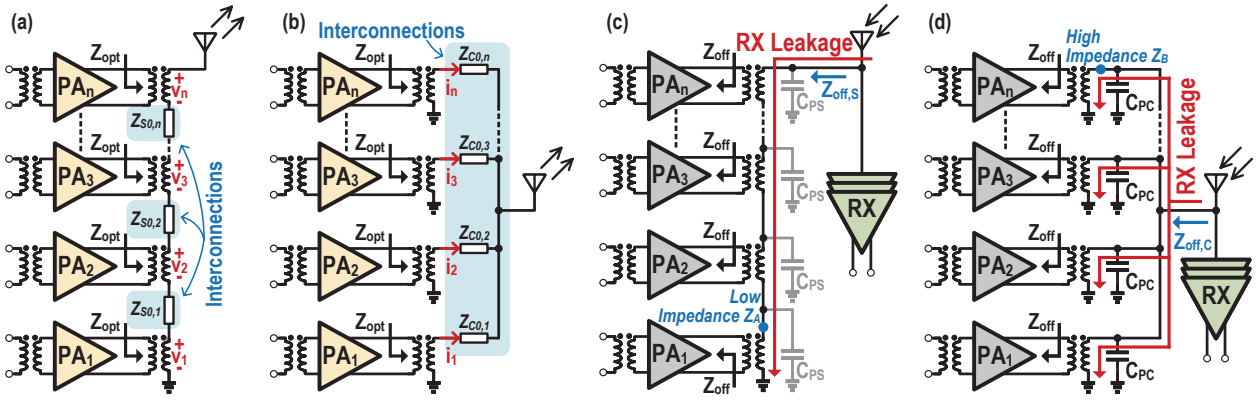

Fig. 2. (Color online) Power-combining PA in TRX: (a) series-combining in TX mode, (b) parallel-combining in TX mode, (c) series-combining in RX mode and (d) parallel-combining in RX mode.

transceiver IC with 3-dB higher output power can increase the communication distance by about 1.4 times without decreasing the beamwidth.

In this work, a 24–30 GHz 8-element dual-polarized phased-array transceiver (TRX) front-end IC for 5G NR FR2 is proposed. Fabricated in 65-nm CMOS, three 3GPP bands (i.e., n257/n258/n261) are fully covered. A two-way combining class-AB PA is integrated to boost the output power. A matching network co-designed (MNCD) on-chip T/R switch is integrated at the antenna interface to support time division duplex (TDD) mode. Section 2 describes the design details of the power-combing PA. The low-noise amplifier (LNA) and MNCD switch is presented in Section 3. Section 4 presents the transceiver architecture and describes other critical phased-array building blocks, including ATT and VMPS. The measurement results and conclusions are presented in Sections 5 and 6, respectively.

2. High-power class-AB power-combining power amplifier

2.1. Power-combining network

The output power of PA can be improved by combining either voltage or current. Fig. 2 depicts the power-combining PA in a phased-array TRX. The *n*-way series-combining PA shown in Fig. 2(a) stacks output voltage of each sub-PA to improve output power. The output-matching network (OMN) of each sub-PA transforms the load impedance Z_L/n to the optimum load impedance Z_{opt}. Hence, the series-combining network reduces the impedance transform ratio of sub-PA OMN. The characteristic impedance of the interconnection transmission line (T-line) should satisfy:

$$Z_{S0,n} = \frac{u_{n-1} + u_{n-1} + \cdots + u_1}{i_n} = \frac{n-1}{n} \cdot Z_L. \quad (1)$$

Otherwise, the impedance mismatching will lead to additional insertion loss of the series-combining network. Different $Z_{S0,n}$ between sub-PAs complicates the design of series-combining PA. The *n*-way parallel-combining PA shown in Fig. 2(b) combines the output current of each sub-PA to improve output power. The OMN of each sub-PA transforms the load impedance $n \cdot Z_L$ to Z_{opt}. The parallel-combining network increases the impedance transform ratio of sub-PA OMN. Unlike the series-combining one, the interconnection T-lines in the parallel-combining network share the same characteristic impedance:

$$Z_{C0,1} = Z_{C0,2} = \cdots = Z_{C0,n} = \frac{u_n}{i_n} = n \cdot Z_L. \quad (2)$$

It eases the design of multi-way, power-combining PA.

In TX mode, these two combining networks present their own advantages: The series-combining network reduces the design complexity of sub-PA OMN; the parallel-combining one reduces the design complexity of interconnection T-lines.

In RX mode, power-combining PA introduces parallel impedances $Z_{off,S}$ and $Z_{off,C}$ at the antenna interface, leading to RX insertion loss [see RX leakage in Figs. 2(c) and 2(d)]. In series-combining PA, the impedance transform ratio of sub-PA OMN is $Z_{opt} : Z_L/n$. As a result, $Z_{off,S}$ in Fig. 2(c) can be addressed as

$$Z_{off,S} = n \cdot Z_A = n \cdot Z_{off} \cdot \frac{Z_L}{nZ_{opt}} = \frac{Z_{off}Z_L}{Z_{opt}}. \quad (3)$$

Similarly, the impedance transform ratio of sub-PA OMN in parallel-combining PA is $Z_{opt} : nZ_L$. Hence, $Z_{off,C}$ in Fig. 2(d) can be addressed as

$$Z_{off,C} = \frac{1}{n} \cdot Z_B = \frac{1}{n} \cdot Z_{off} \cdot \frac{nZ_L}{Z_{opt}} = \frac{Z_{off}Z_L}{Z_{opt}}. \quad (4)$$

According to Eqs. (3) and (4), in the ideal situation, the series- and parallel-combining PA present the same off-mode output impedances in RX mode. However, the two main reasons addressed below lead to the difference between $Z_{off,S}$ and $Z_{off,C}$.

(a) The parasitic capacitance of the transformer in each sub-PA OMN. As depicted in Figs. 2(c) and 2(d), the parasitic capacitances C_{PS} and C_{PC} exist in the series- and parallel-combining networks, leading to the magnitude degradation of Z_A and Z_B. The impedance transform ratio of sub-PA OMN in the parallel-combining network is n^2-times higher than that of the series-combining one. Thus, the implementation of sub-PA OMN in parallel-combining network requires more coils in the transformer, resulting in larger parasitic capacitance (i.e., $C_{PC} > C_{PS}$). On the other hand, according to Eqs. (3) and (4), Z_B is n^2-times higher than Z_A. For these reasons, the product of Z_B and C_{PC} is much higher than that of Z_A and C_{PS}. Consequently, the impedance magnitude of Z_B in parallel with C_{PC} is

$$|Z_{B//C}| = \frac{Z_B}{\sqrt{1+(\omega C_{PC}Z_B)^2}} \xrightarrow{(\omega C_{PC}Z_B)^2 \gg 1} \frac{1}{\omega C_{PC}}. \quad (5)$$

The large product of Z_B and C_{PC} make $Z_{B//C}$ deviate from its ideal value Z_B, and further make $Z_{off,C}$ deviate from its ideal value addressed in Eq. (4). In contrast, the impedance magnitude of Z_A in parallel with C_{PS} is

$$|Z_{A//C}| = \frac{Z_A}{\sqrt{1+(\omega C_{PS}Z_A)^2}} \xrightarrow{(\omega C_{PS}Z_A)^2 \ll 1} Z_A. \quad (6)$$

The small product of Z_A and C_{PS} ensures that $Z_{A//C}$ is close to its ideal value Z_A. As a result, $Z_{off,S}$ is close to its ideal value addressed in Eq. (3).

(b) The interconnections between each sub-PA OMN. In the n-way parallel-combining network, sub-PA OMNs are combined by interconnection T-lines, the characteristic impedance of which is nZ_L [see Eq. (2)]. In RX mode, these interconnection T-lines combine n-way $Z_{B//C}$ in parallel, yielding $Z_{off,C}$. According to Eq. (4), $Z_{B//C}$ is addressed as

$$Z_{B//C} = \frac{nZ_LZ_{off}}{Z_{opt}} // \frac{1}{j\omega C_{PC}} = \frac{nZ_LZ_{off}}{Z_{opt}+n \cdot j\omega C_{PC}Z_LZ_{off}} \neq nZ_L. \quad (7)$$

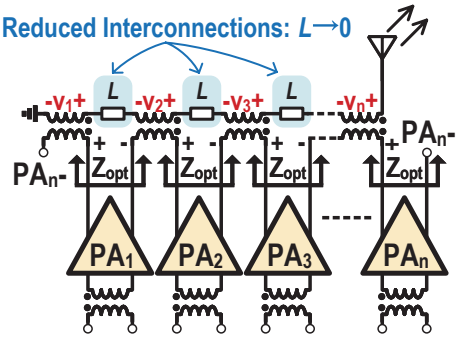

Fig. 3. (Color online) The series-combing power amplifier based on the distributed-active transformer.

Since $Z_{B//C}$ is not equal to the characteristic impedance of nZ_L, the interconnection T-lines will induce impedance transformation. It makes $Z_{off,C}$ deviate from its ideal value addressed in Eq. (4). In contrast, in the n-way series-combining network, $Z_{A//C}$ is in series with each other. The magnitude degradation of impedance induced by interconnection T-line characteristic impedance mismatch is alleviated. Moreover, by optimizing the layout floorplan[11], the length of the interconnection T-lines in the series-combining network can be reduced, ensuring that $Z_{off,S}$ is close to its ideal value, as addressed in Eq. (3).

According to these two reasons addressed above, in RX mode, the off-mode impedance at the antenna interface of the n-way series-combining PA is higher than that of the n-way parallel-combining one (i.e., $Z_{off,S} > Z_{off,C}$), leading to the reduced RX leakage, and, thus, ensuring the lower RX insertion loss. In this work, the proposed PA is implemented with the two-way series-combining network, boosting the output power without inducing significant insertion loss in RX mode.

As depicted in Fig. 2(a), in series-combining PA, the length of interconnection T-lines is mainly decided by the distance between each sub-PA. The active core and supply network of each sub-PA consume chip area, becoming the bottleneck of reducing the length of interconnection T-lines.

To tackle this, the distributed-active transformer[12, 13] (DAT) combining network is proposed. The schematic is depicted in Fig. 3. DAT moves sub-PA differential OMN from PA_n output to the differential terminal between PA_n and PA_{n-1}. Note that the sub-PAs share the same active core. The minus terminal of PA_{n-1} is equivalent to that of PA_n. Hence, as a traditional series-combining network, DAT stacks output voltage of sub-PA to boost the output power. In contrast, as shown in Fig. 3, in DAT, the bottleneck of reducing the length of sub-PA OMN interconnection T-lines is the distance of the differential signal path, which is relatively small. As a result, DAT significantly reduces the length of interconnection T-lines. In this work, the two-way series-combining network is implemented as DAT.

2.2. PA circuit implementation

Fig. 4 depicts the schematic of the proposed four-stage power-combining PA, including the two-stage common-source (CS) amplifier and the two-stage two-way cascode amplifier. The details of the T/R switch will be addressed in the next section.

Each CS transistor pairs in Fig. 4 utilizes the differential capacitive neutralization techniques to improve gain and stability. Inductors 210-pH L_2 and 150-pH L_3 are introduced at the

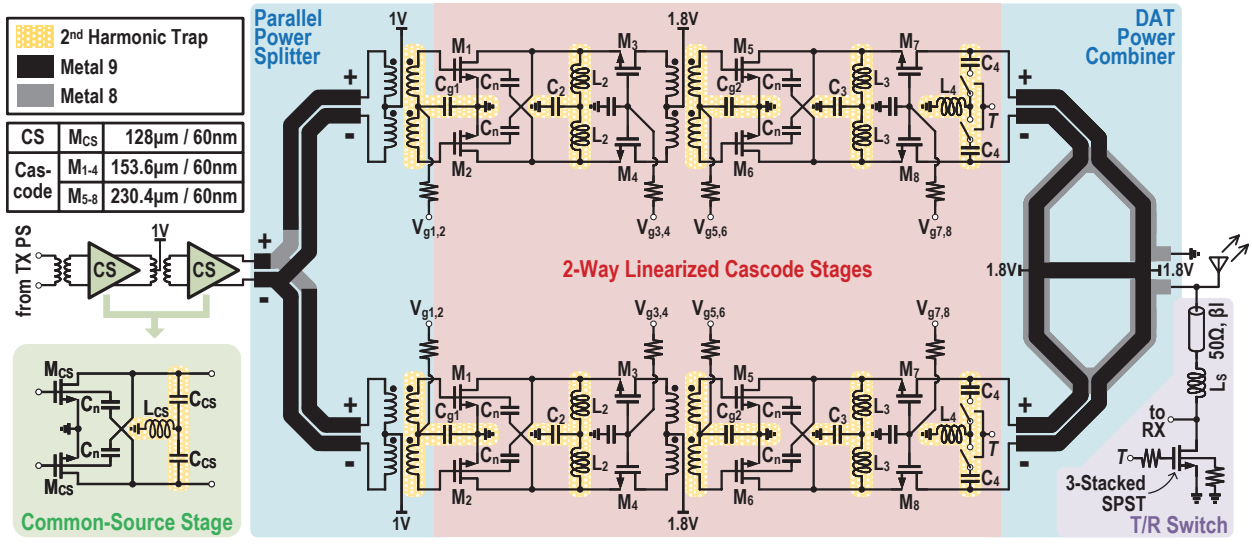

Fig. 4. (Color online) Schematic of differential four-stage two-way power-combining power amplifier.

cascode intermediate nodes of two cascode stages, reducing the amplitude-to-phase (AM–PM) distortions from above 9° to around 3° without degrading PA output power and efficiency[1]. To further reduce the AM-PM distortion, C_{g2}, C_3 and L_4 are introduced at the output stage to enable wideband 2nd harmonic filtering. The layouts of cascode active cores are developed based on Ref. [1], realizing wideband 2nd harmonic filtering with compact size.

Fig. 5 depicts the schematic of the proposed output stage in common mode. Three 2nd harmonic traps provide three signal paths for the 2nd harmonic (i.e., $Z_{in}1$, $Z_{in}2$ and $Z_{in}3$). $Z_{in}1$ consists of C_4 and L_4. $Z_{in}2$ consists of L_3 and C_3. $Z_{in}3$ consists of neutralization capacitance C_n, transistor parasitic capacitance C_{gd}, inductance in the inter-stage transformer L_{MN} and C_{g2}. Note that the common mode capacitance C_{cm} of the transformer is small. Hence, it is omitted in the following discussion. Among these harmonic traps, C_{g2}, C_3, L_4 are blocked by the differential virtual ground at fundamental frequency. As a result, the PA design procedure is: First, complete the design of C_4, L_3, L_{MN}, C_n according to the performance at fundamental frequency; second, adjust the value of C_{g2}, C_3, L_4 to enable wideband 2nd harmonic filtering. The resonant frequency of each harmonic trap is

$$f_{0,Zin1} = f(L_4) = \frac{1}{2\pi\sqrt{2L_4C_4}}, \tag{8}$$

$$f_{0,Zin2} = f(C_3) = \frac{\sqrt{2}}{2\pi\sqrt{L_3C_3}}, \tag{9}$$

$$f_{0,Zin3} = f(C_{g2}) = \frac{1}{2\pi}\sqrt{\frac{4(C_n + C_{gd}) + 2C_{g2}}{L_{MN}C_{g2}(C_n + C_{gd})}}. \tag{10}$$

In this work, the values of C_4, L_3, L_{MN}, C_n are 100 fF, 150 pH, 73.1 fF, and 228.2 pH, respectively. C_{gd} shares the same capacitance with C_n. Based on these parameters, L_4, C_3, C_{g2} are respectively implemented with values of 43.4 pH, 135.1 fF, and 240.5 fF, resulting in the $f_{0,Zin1}$, $f_{0,Zin2}$, and $f_{0,Zin3}$ of 54, 50, and 58 GHz. Hence, three 2nd harmonic traps fully

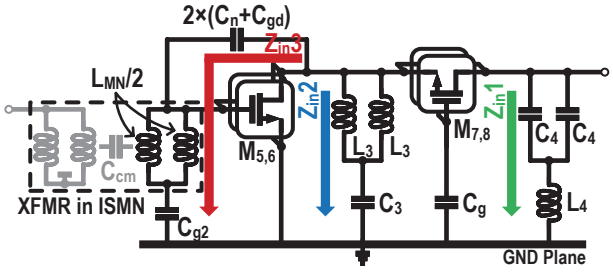

Fig. 5. (Color online) Schematic of the power amplifier output stage in common mode.

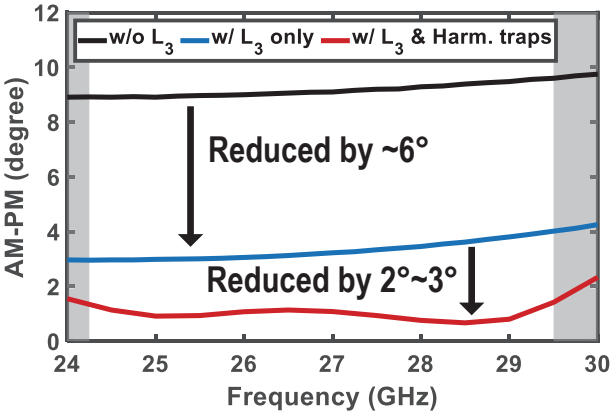

Fig. 6. (Color online) Simulated AM–PM of the proposed cascode cell across frequencies.

cover the band of 2 × 24 GHz to 2 × 30 GHz, enabling the wideband 2nd harmonic filtering. Fig. 6 depicts the simulated AM–PM of the proposed output stage across frequencies. With inductor L_3 and three-stage 2nd harmonic trap, the proposed output stage demonstrates a simulated AM–PM of 0.8°–1.4° across the 3GPP n257/n258/n261 bands. Similar to the output stage, 2nd harmonic traps are also integrated in driver stages to further mitigate the AM–PM.

Based on the proposed active cores, a two-way DAT is designed and integrated at the PA output. Fig. 7 depicts the schematic of the proposed DAT, which serves as both power combiner and OMN. It combines the output power of sub-PA while transforming 50-Ω load impedance to sub-PA Z_{opt} of

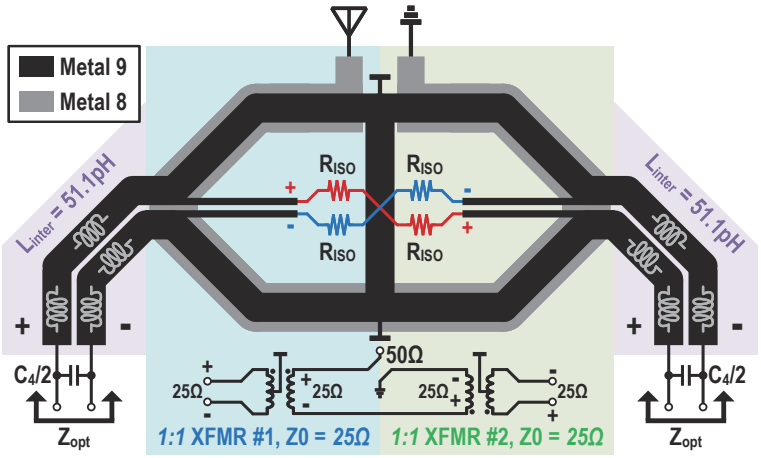

Fig. 7. (Color online) Schematic of the DAT power-combining network.

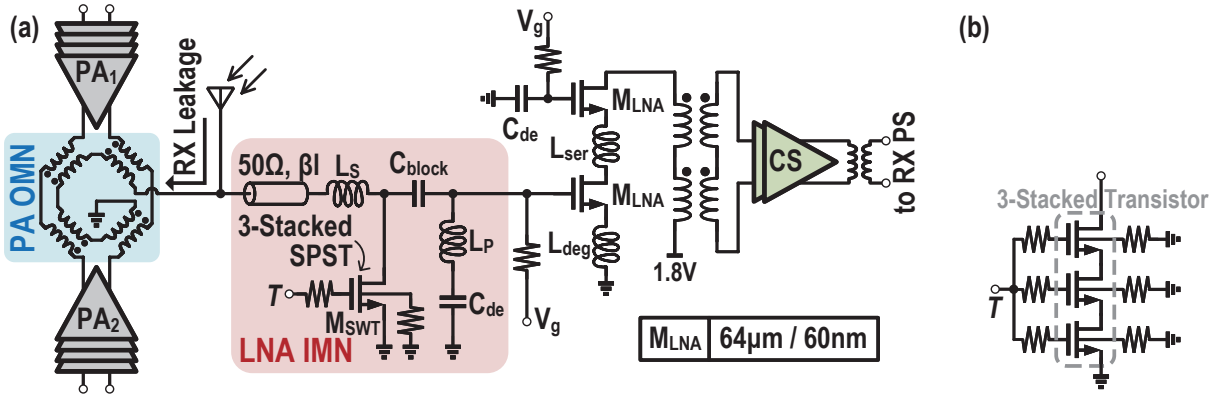

Fig. 8. (Color online) Schematics of (a) the low-noise amplifier and the T/R switch and (b) the three-stacked resistive body-floating switch transistor M_{SWT}.

30 + j × 25 Ω. Hence, the area of power-combining PA is reduced, facilitating the PA integration in the phased-array TRX IC.

As shown in Fig. 7, the proposed DAT consists of two sub-transformers (sub-XFMRs), the impedance transformation ratio and characteristic impedance of which are 1 : 1 and 25 Ω, respectively. The equivalent inductance of interconnections L_{inter} and parallel capacitance C_4 further transform 25 Ω to Z_{opt}. However, the 90° turning of L_{inter} will lead to signal imbalance. To tackle this issue, the isolation resistances R_{ISO} of 12 Ω are introduced, as plotted in Fig. 7. It absorbs the imbalanced signal power, avoiding potential performance degradation. Similar to the isolation resistance in the Wilkinson combiner, R_{ISO} can also improve the isolation between two sub-PAs. With R_{ISO}, EM-simulation results show that the isolation is improved by at least 24 dB. Across 24–30 GHz, the EM-simulated isolation between two sub-PAs is from 31 to 52 dB. High isolation is beneficial for the stability of the power-combining PA.

Across 24–30 GHz, the EM-simulated insertion loss of the proposed DAT is 0.7–0.9 dB. The four-stage power-combining PA demonstrates a simulated power gain of 39.0–39.6 dB with a simulated OP1dB of 20.0–20.9 dBm.

3. Low-noise amplifier and RF switch

Fig. 8(a) depicts the schematic of the proposed LNA and the matching network co-designed (MNCD) on-chip T/R switch. LNA is implemented as one single-ended cascode stage and two differential CS stages. At the input cascode stage, the 114-pH L_{ser} is introduced to boost gain[14]. The 72-pH L_{deg} is introduced to enable inductive source degeneration to facilitate simultaneous noise and gain matchings. EM-simulation results show that the proposed LNA demonstrates a small signal gain of 28.1–28.7 dB and noise figure (NF) of 3.3–3.8 dB across 24–30 GHz.

The RF switch is implemented as the MNCD on-chip T/R switch. The switch transistor M_{SWT} is implemented with three-stacked resistive body-floating technique[15] to sustain large voltage swing and reduce off-mode capacitance C_{off}. The schematic is depicted in Fig. 8(b). In TX mode, M_{SWT} is turned on, LNA is turned off. L_S and the T-line with an electrical length of βl together transform the turn-on resistance of M_{SWT} to high impedance[1], reducing the insertion loss in TX mode. The inductance of L_S is 286.3 pH with a quality factor of above 17.6 across 24–30 GHz. In RX mode, PA and M_{SWT} are both turned off. The input-matching network of LNA consists of C_{off}, L_S, C_{block} and L_P. As depicted in Fig. 8, off-mode PA will induce RX leakage in RX mode, resulting in the additional RX insertion loss.

Fig. 9 depicts the simplified off-mode PA AC model in RX mode. The output impedance of off-mode PA is simplified as a parallel RC tank, which consists of 958-Ω $R_{off,PA}$ and 110-fF $C_{off,PA}$. Sub-XFMRs in DAT are simplified as a T-section model[16], including 110.3-pH L_{S1}, 167.8-pH L_P and 14-pH L_{S2}. L_{S2} is omitted in the following discussion due to the low inductance. As shown in Fig. 9, $R_{off,PA}$, $C_{off,PA}$, C_t and L_{S1} can be the equivalent to C_{eq} in series with R_{eq}. Proper C_t is able to introduce parallel resonance between C_{eq} and L_P, and, thus,

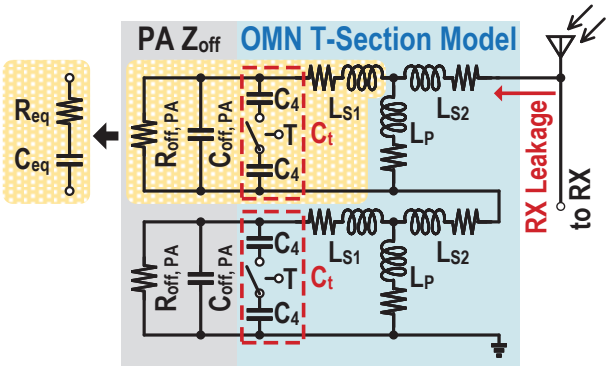

Fig. 9. (Color online) Simplified power amplifier AC model in RX mode.

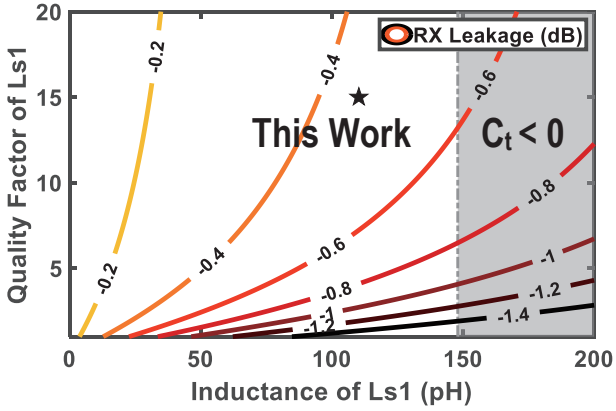

Fig. 10. (Color online) RX leakage contours with different L_{S1} and Q_{LS1}.

reduce the RX leakage induced by off-mode PA. In RX mode, the switched capacitor C_t satisfies:

$$C_t = \frac{1}{\omega^2 (L_P + L_{S1})} - C_{off,PA}. \tag{11}$$

In this work, the capacitances of C_t in RX and TX modes are 14.9 and 50 fF, respectively. It introduces parallel resonance at 27 GHz in RX mode and enables 2nd harmonic filtering and power matching in TX mode. The switch transistor in C_t is implemented with four-stacked resistive body-floating technique[14] to sustain large voltage swing of PA.

Nevertheless, the limited $R_{off,PA}$ and the parasitic resistance of L_{S1} degrades the quality factor of the parallel resonance, and, thus, the off-mode PA still leads to additional RX leakage. To quantify the impact of the lump parameters addressed above on RX leakage, R_{eq} and C_{eq} can be addressed as:

$$R_{eq} = \frac{R_{off,PA}}{1 + Q_C^2} + \frac{\omega L_{S1}}{Q_{Ls1}}, \tag{12}$$

$$C_{eq} = \frac{1 + Q_C^2}{\omega R_{off,PA} Q_C - \omega^2 L_{S1} \left(1 + Q_C^2\right)}, \tag{13}$$

where Q_{LS1} is the quality factor of L_{S1}, Q_C is the total quality factor of $C_{off,PA}$ and C_t:

$$Q_C = \omega R_{off,PA} \left(C_{off,PA} + C_t\right) = \frac{R_{off,PA}}{\omega \left(L_P + L_{S1}\right)}. \tag{14}$$

Combining Eqs. (12)–(14), the quality factor of C_{eq} can be addressed as:

$$Q_{eq} = \frac{1}{\omega R_{eq} C_{eq}} = \frac{\left(Q_C R_{off,PA} / \omega L_{S1}\right) - Q_{LS1}\left(1 + Q_C^2\right)}{\left(R_{off,PA} / \omega L_{S1}\right) + 1 + Q_C^2}. \tag{15}$$

Hence, the minimum RX leakage induced by off-mode PA is

$$\mathrm{RXLeakage[dB]} = 10\log_{10}\left(\frac{2\left(1 + Q_{eq}^2\right)}{2\left(1 + Q_{eq}^2\right) + \omega Z_L Q_{eq} C_{eq}}\right), \tag{16}$$

where Z_L is the load impedance at the antenna interface (i.e., 50 Ω). Eqs. (12)–(16) clearly show that the RX leakage correlates to $R_{off,PA}$, L_{S1}, and L_P. Among these parameters, $R_{off,PA}$ is decided by the transistor size and output power of PA. L_P affects the coupling coefficient and insertion loss of PA OMN. Hence, $R_{off,PA}$ and L_P have been determined during the PA design procedure. The RX leakage is up to L_{S1} and its quality factor Q_{LS1}.

According to Eq. (16), Fig. 10 depicts the simulated RX leakage contours across different L_{S1} and Q_{LS1}, clearly showing that small L_{S1} with high Q_{LS1} results in low RX leakage. As shown in Fig. 7, L_{S1} consists of the equivalent series inductance of sub-XFMR and the interconnection L_{inter}. The former can be reduced by increasing the coupling coefficient of sub-XFMR. Hence, L_{inter} is the bottleneck of reducing L_{S1}.

In this work, L_{inter} is routed in 45° to reduce the electrical length. The spacing is set to 2 μm to reduce the characteristic impedance. Short electrical length and low characteristic impedance result in the low equivalent inductance L_{inter} of 51.1 pH. Besides, L_{inter} and the primary coil of sub-XFMR is implemented with the widest top thick metal to reduce the series parasitic resistance, and, thus, to improve Q_{LS1}. According to the EM-simulation results, in this work, the inductance of L_{S1} is 110.3 pH with a Q_{LS1} of 14.9. Based on this inductance, the off-mode PA introduces a parallel impedance with a peak magnitude of 457 Ω at the antenna interface, leading to a RX insertion loss of 0.45 dB at 27 GHz. With the 0.2-dB insertion loss induced by the "βl T-line" (see Fig. 8), the proposed MNCD switch leads to RX insertion loss of less than 0.7 dB at 27 GHz.

To evaluate the insertion loss of the proposed MNCD switch across frequencies, Figs. 11(a) and 11(b) respectively depict the EM-simulated critical performances of the proposed PA and LNA with or without the proposed MNCD switch. As shown in Fig. 11, across the 3GPP n257/n258/n261 bands, the proposed MNCD switch respectively presents the insertion losses of 0.5–0.7 dB and 0.6–1.0 dB in TX and RX modes, excluding the insertion losses of PA output and LNA input matching networks. With the proposed MNCD switch, the proposed PA demonstrates the simulated power gain of 38.5–39.1 dB with the OP1dB of 19.5–20.4 dBm, the proposed LNA presents the simulated gain of 27.5–27.8 dB with the NF of 3.9–4.7 dB.

4. Phased-array transceiver

Fig. 12 depicts the block diagram of the mm-Wave 5G 8-element dual-polarized phased-array TRX IC. The dual-polarized power distribution network is implemented as two individual differential Wilkinson combiners/splitters. Two baluns are

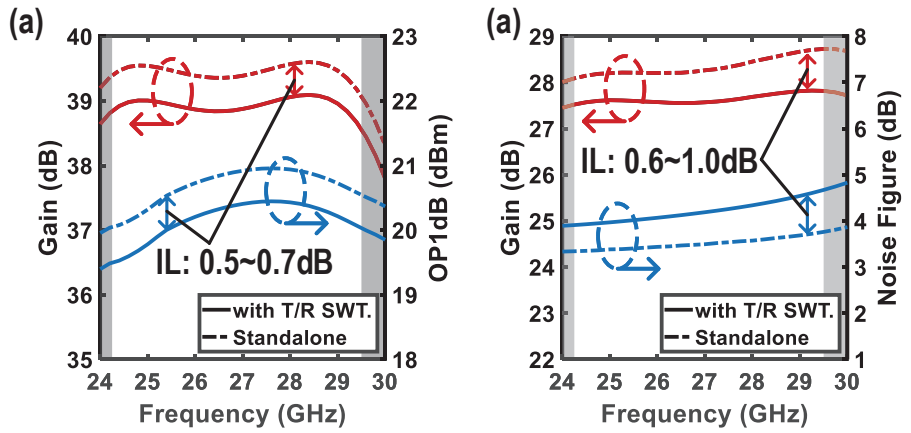

Fig. 11. (Color online) EM-simulated (a) S21 and OP1dB of PA, (b) S21 and NF of LNA.

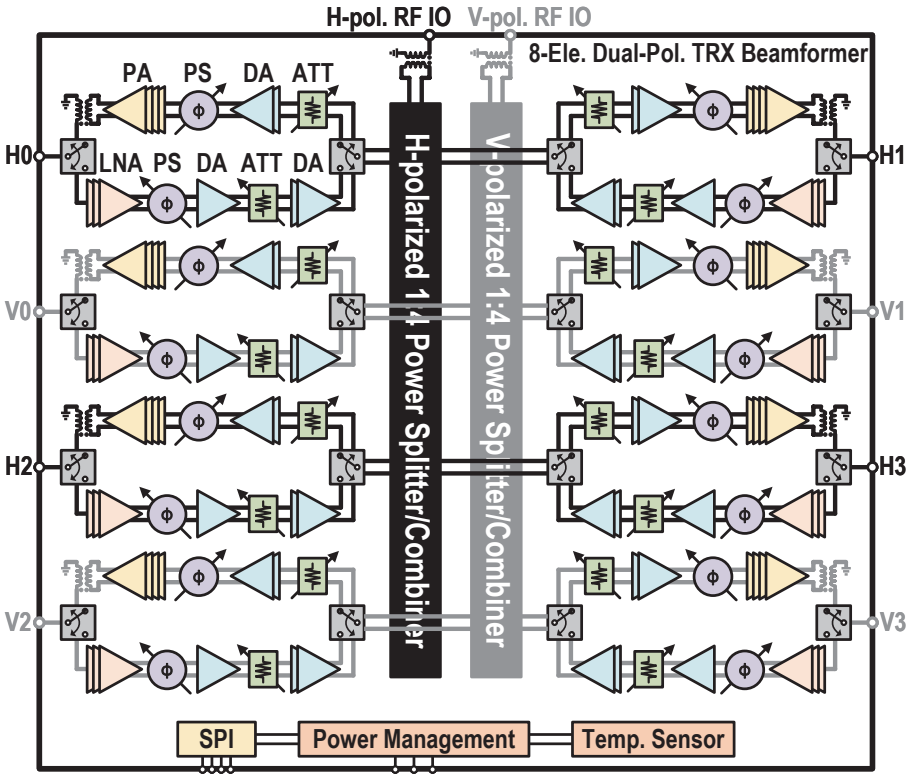

Fig. 12. (Color online) Block diagram of the mm-Wave 5G 8-element dual-polarized phased-array TRX IC.

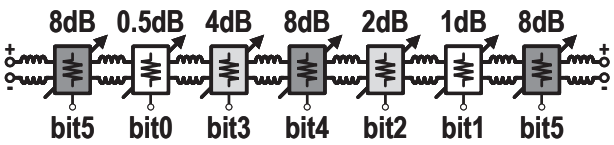

Fig. 13. Simplified schematic of the 6-bit differential switched attenuator.

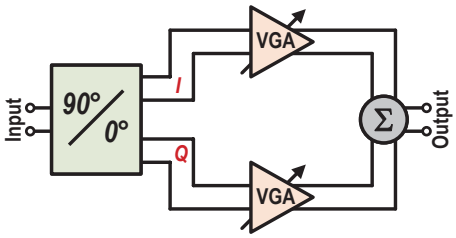

Fig. 14. (Color online) Schematic of the 6-bit differential vector modulated phase shifter.

integrated at the common interface to enable the single-ended RF signal I/O. In each element, the TX chain consists of a four-stage PA, an active PS, a two-stage driver amplifier (DA) and an ATT. The RX chain consists of a three-stage LNA, an active PS, a DA, an ATT, and a two-stage DA. In both TX and RX chains, ATT is integrated far away from the antenna interface to reduce the impact of gain tuning on TX linearity and RX NF. The proposed MNCD switch is integrated at the antenna interface to support TDD mode. Critical building blocks including the temperature sensor and serial peripheral interface (SPI) are integrated as well to support large-scale phased-array applications. The details of ATT and PS are addressed in the following.

4.1. 6-bit differential switched ATT

In this work, gain control is achieved by a 6-bit differential switched ATT[17], enabling the gain compensation and side-lobe suppression. Fig. 13 depicts the simplified schematic.

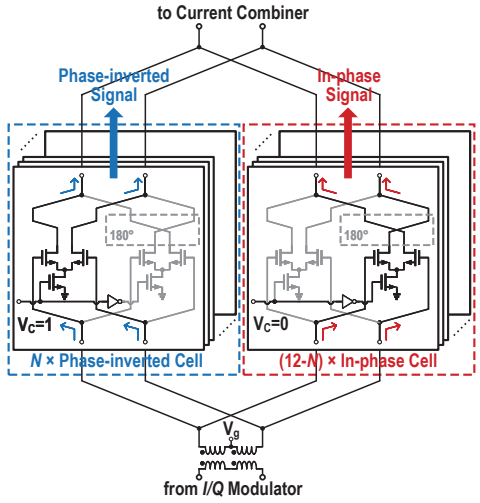

Fig. 15. (Color online) Phase-invariant VGA in the I/Q paths of the VMPS.

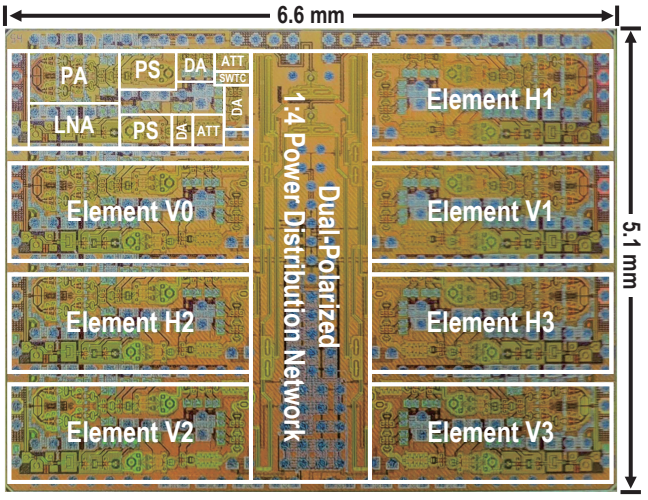

Fig. 16. (Color online) A micrograph of the mm-Wave 5G 8-element dual-polarized phased-array transceiver IC.

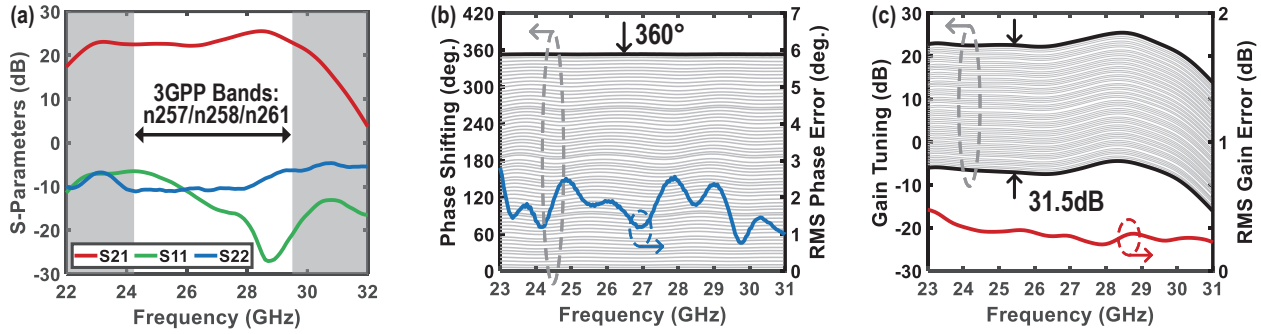

Fig. 17. (Color online) Small-signal CW measurement results in TX mode: (a) *S*-parameters. (b) Phase shifting. (c) Gain tuning.

The proposed ATT consists of seven switched ATT cells, including three Π-type cells for 8-dB step, two T-type cells for 2-/4-dB steps and two simplified T-type cells for 0.5-/1-dB steps. 16-dB step is achieved by cascading two 8-dB cells (i.e., bit5 in Fig. 13). The parallel transistors in ATT are implemented as stacked transistors to improve linearity.

Simulated in the TRX element, the ATT presents a gain range of 31.5 dB and a gain resolution of 0.5 dB in both TX and RX modes. Across 24–30 GHz, the simulated RMS gain errors are less than 0.14 and 0.24 dB in TX and RX modes, respectively.

4.2. 6-bit differential VMPS

In this work, the 6-bit VMPS is utilized to fully cover the 360° phase shifting range with high phase resolution and low additional gain error. Fig. 14 depicts the schematic of the VMPS. The transformer-based I/Q modulator at the input generates in-phase and quadrature (I/Q) signals[18]. Across 24–30 GHz, the phase and magnitude errors are less than 0.5° and 0.3 dB, respectively. Next, the I/Q signals are differently weighted by the variable gain amplifier (VGA) and combined at the output to enable phase shifting. The schematic of VGA is depicted in Fig. 15. The VGA achieves gain control by combining differently weighted in-phase and phase-inverted signals. In either I or Q signal path, the VGA enables the phase-inverted gain tuning when *N* is 7 to 12. When *N* is 0 to 5, the in-phase gain tuning is performed. The proposed phase-inverting VGA ensures the 360° phase shifting range of VMPS. Finally, 64 phase states are selected to cover the 360° phase shifting range with high phase resolution of 5.625° and low additional gain error.

Simulated in the TRX element, the VMPS presents a phase shifting range of 360° and a phase resolution of 5.625° in both TX and RX modes. Across 24–30 GHz, the simulated RMS phase errors are less than 0.9° in both TX and RX modes. The DC power consumption is only 3.8 mW.

5. Measurement results

Fabricated in 65-nm bulk CMOS, the proposed dual-polarized TRX IC occupies a total area of 6.6 × 5.1 mm^2. The die micrograph is shown in Fig. 16. On a millimeter-wave probe station, the continuous-wave (CW) and 5G NR FR2 modulation measurements are both performed with a 1.8-V supply voltage for cascode stages in PA/LNA and a 1-V supply voltage for other RF building blocks. All the DC supplies are wire-bonded to a PCB. And the RF signals are accessed by GSG probes.

The small signal CW measurement results in TX mode, including *S*-parameters, phase shifting and gain tuning, are depicted in Fig. 17. As shown in Fig. 17(a), in TX mode, the proposed dual-polarized TRX demonstrates a peak measured gain of 25.5 dB at the frequency of 28.5 GHz with a −3-dB bandwidth across 22.8 to 29.7 GHz. Across the operating band, the return loss at the antenna interface is from 6.5 to 11.1 dB. The 6-bit phase shifting is measured at the maximum gain mode and depicted in Fig. 17(b). Across the 3GPP n257/n258/n261 bands, the proposed TRX covers 360° shifting range with a phase resolution of 5.625° and a measured

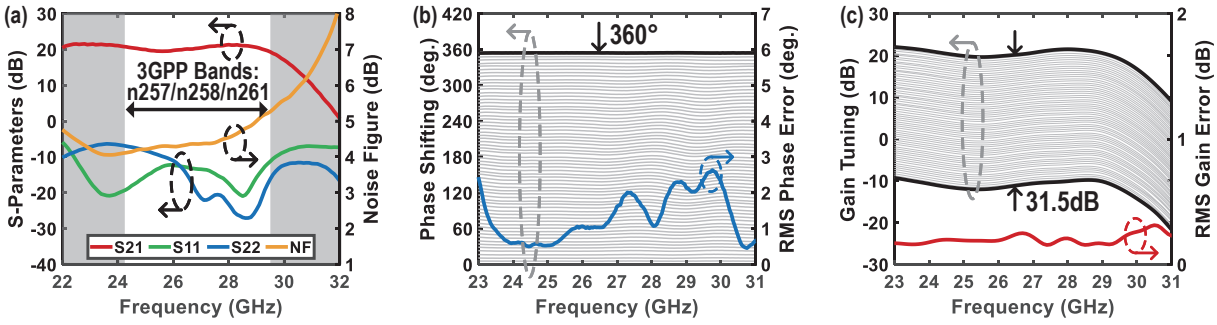

Fig. 18. (Color online) Small-signal CW measurement results in RX mode: (a) *S*-parameters. (b) Phase shifting. (c) Gain tuning.

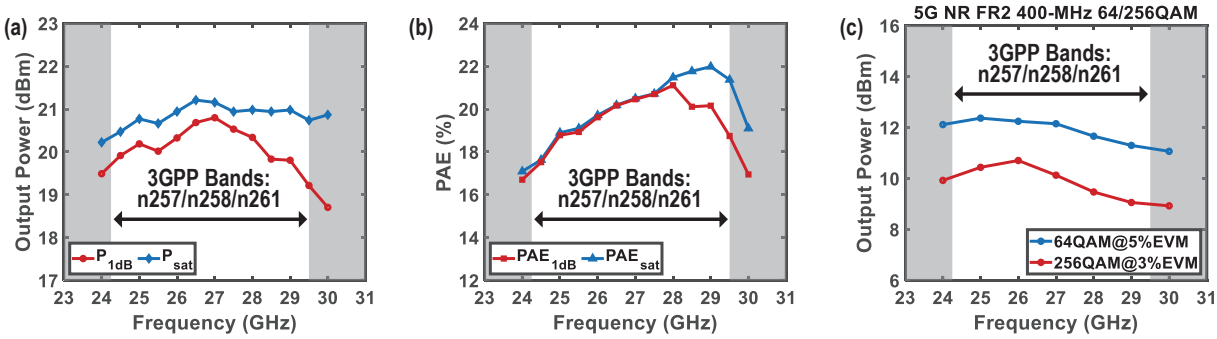

Fig. 19. (Color online) Large-signal measurement results in TX mode: (a) OP1dB and P_{sat}. (b) PAE. (c) Output power in 5G NR FR2 64-QAM and 256-QAM signals.

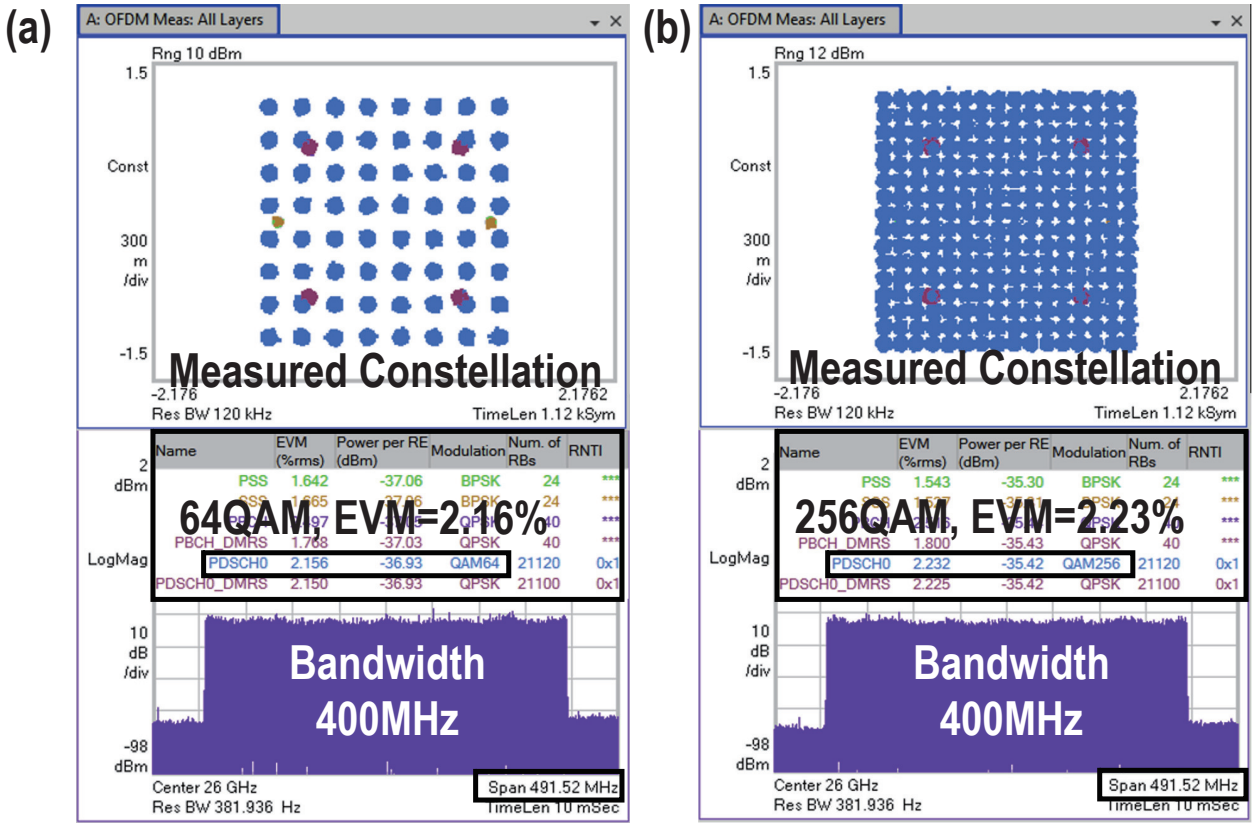

Fig. 20. (Color online) Measured constellations, EVM and spectrum with 400-MHz 5G NR FR2 OFDM signal in TX mode: (a) 64-QAM and (b) 256-QAM.

RMS error of 0.8° to 2.4°. The 6-bit gain tuning is further measured and plotted in Fig. 17(c). A 31.5-dB gain range is achieved with a gain step of 0.5 dB and a measured RMS error of 0.21 to 0.34 dB. The measured coupling between adjacent TRX elements is less than −48.7 dB across 24−30 GHz.

The small signal CW measurements, including *S*-parameters, phase shifting and gain tuning, are further performed in RX mode. The measurement results are depicted in Fig. 18. In RX mode, the proposed dual-polarized TRX presents a peak measured gain of 21.3 dB at the frequency of 28.0 GHz with

Table 1. Comparison of state-of-the-art silicon-based phased-array TRX IC for mm-Wave 5G.

	This work	SEU JSSC'22[1]	Tokyo Tech. JSSC'21[2]	Samsung ISSCC'20[3]	Qualcomm ISSCC'18[4]	IBM ISSCC'22[5]
Technology	65 nm CMOS	65 nm CMOS	65 nm CMOS	28 nm CMOS	28 nm CMOS	130 nm SiGe BiCMOS
Frequency (GHz)	24–29.5	24–29.5	28	37–40	26.5–29.5	24–30
Integration	8CH TRX	4CH TRX	8CH TRX	16CH TRX	24CH TRX	16CH TRX
Supply (V)	1.0/1.8	1.0/1.8	1.0	0.9/1.8	1.0/1.8	1.5/2.7
TX gain (dB)	22.5–25.5	23.0–25.5	25	60[a]	34–44	25–31
TX P_{sat} (dBm)	20.3–21.2	16.8–18.0	16.1	16.5	14	16.9–17.1
TX P_{1dB} (dBm)	19.2–20.8	16.0–17.6	13.7	N/A	12	15.9–16.1
TX PAE_{max} (%)	22.0	20.8	N/A	N/A	20	22.1–23.9
TX PAE_{1dB} (%)	21.1	20.4	N/A	N/A	N/A	N/A
TX P_{DC}/CH (mW)	568(@P_{1dB})	272(@P_{1dB})	186(@P_{sat})	105(@6dBm)	119(@11dBm)	200(@P_{sat})
RX gain (dB)	19.5–21.3	12.3–14.2	18	59[a]	32–34	29–30
RX NF (dB)	4.1–5.2	4.3–6.0	4.9 (28 GHz)	4.2–4.6	3.8–4.6	3–3.8
RX P_{DC}/CH (mW)	89	82	88	39	42	90
Gain range (dB)	31.5	31.5	8	30[a] (*T*)/43[a] (*R*)	7(*T*)/9(*R*)	20(*T*)/27(*R*)
Gain step (dB)	0.5	0.5	0.5	1	1	0.25
RMS gain error (dB)	0.21–0.34(TX) 0.16–0.26(RX)	<0.35(TX) <0.22(RX)	N/A	N/A	N/A	N/A
Phase step (°)	5.625(6 bits)	5.625(6 bits)	11.25(5 bits)	22.5(4 bits)	45(3 bits)	<5.6(~6 bits)
RMS phase error (°)	0.8–2.4(TX) 0.6–2.5(RX)	<1.9(TX) <1.8(RX)	2	3.3	N/A	1.2

[a] Conversion gain.

a −3-dB bandwidth across 21.6 to 29.8 GHz, as shown in Fig. 18(a). The measured NF is from 4.1 to 5.2 dB across the operating band. The measured return loss at the antenna interface is from 12.2 to 20.9 dB. As in TX mode, the 6-bit phase shifting is measured at the maximum gain mode and depicted in Fig. 18(b). Across the 3GPP n257/n258/n261 bands, in RX mode, the proposed TRX covers the 360° shifting range with a phase resolution of 5.625° and a measured RMS error of 0.6° to 2.5°. The 6-bit gain tuning is further measured and plotted in Fig. 18(c). A 31.5-dB gain control range is achieved with a gain step of 0.5 dB and a measured RMS error of 0.16 to 0.26 dB. In both TX and RX modes, the proposed TRX covers the 3GPP n257/n258/n261 bands with flat frequency response, high-resolution 6-bit 360° phase shifting and high-resolution 6-bit 31.5-dB gain tuning.

Large-signal measurements are further performed in TX mode, including CW and modulation measurements. As shown in Fig. 19(a), the proposed TRX delivers a measured TX OP1dB of 19.2 to 20.8 dBm and a measured P_{sat} of 20.3 to 21.2 dBm across the 3GPP n257/n258/n261 bands. As depicted in Fig. 19(b), the corresponding PAEs are 17.0% to 21.1% and 17.3% to 22.0%, respectively. The modulation measurements are performed with 400-MHz 5G NR FR2 OFDM 64- and 256-QAM signal. The peak-to-average power ratios (PAPRs) are 11.6 and 12.0 dB, respectively. Fig. 19(c) depicts the measured output power of the proposed TRX under the 64-QAM signal with 5% EVM (i.e., −26.0 dB) and the 256-QAM signal with 3% EVM (i.e., −30.5 dB). The proposed TRX covers the 3GPP n257/n258/n261 bands with the output power of 11.0 to 12.4 dBm in the 64-QAM signal and 9.0 to 10.7 dBm in the 256-QAM signal.

Fig. 20 depicts the measured constellations, EVM and spectrum with 400-MHz 5G NR FR2 OFDM signal in TX mode. With the 400-MHz bandwidth, the optimal measured EVMs of the proposed TRX are 2.16% for 64-QAM signal and 2.23% for 256-QAM signal.

In Table 1, critical metrics are summarized and compared with recently published state-of-the-art silicon-based mm-Wave 5G TRX ICs. This work successfully covers three 3GPP 5G NR FR2 bands, including n257/n258/n261 bands, with the highest OP1dB of 20.8 dBm and an excellent NF of 4.1 dB.

6. Conclusion

This article presents an 8-element dual-polarized phased-array TRX front-end IC for mm-Wave 5G NR. In the 5G NR FR2 TDD scenario, the impact of PA power enhancement technologies on RX insertion loss are discussed. A four-stage wideband high-power class-AB PA with DAT and three-stage 2nd harmonic traps is proposed, ensuring the mitigated AM–PM distortions across wide carrier frequencies without degrading other TX critical performances. In addition, an MNCD T/R switch is proposed to support TDD mode with reduced insertion loss in both TX and RX modes. Fabricated in 65-nm bulk CMOS, the proposed TRX demonstrates the state-of-the-art TX OP1dB of 20.8 dBm and the RX NF of 4.1 dB among bulk CMOS TRX beamformers. With the 400-MHz 5G NR FR2 OFDM signals, the TRX delivers an output power of 11.0–12.4 dBm in 64-QAM with 5% EVM and an output power of 9.0–10.7 dBm in 256-QAM with 3% EVM, covering 3GPP 5G NR FR2 operating bands of n257, n258, n261.

Acknowledgments

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