REVIEWS

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Advances in mobility enhancement of ITZO thin-film transistors: a review

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Abstract: Indium-tin-zinc oxide (ITZO) thin-film transistor (TFT) technology holds promise for achieving high mobility and offers significant opportunities for commercialization. This paper provides a review of progress made in improving the mobility of ITZO TFTs. This paper begins by describing the development and current status of metal-oxide TFTs, and then goes on to explain the advantages of selecting ITZO as the TFT channel layer. The evaluation criteria for TFTs are subsequently introduced, and the reasons and significance of enhancing mobility are clarified. This paper then explores the development of high-mobility ITZO TFTs from five perspectives: active layer optimization, gate dielectric optimization, electrode optimization, interface optimization, and device structure optimization. Finally, a summary and outlook of the research field are presented.

Key words: thin-film transistor (TFT); indium-tin-zinc oxide (ITZO) TFT; mobility; active matrix (AM) displays

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1. Introduction

Thin-film transistors (TFTs) are essential components in active matrix (AM) displays because they serve as the switch and drive units for pixels[1–5]. TFTs, a type of field-effect transistor, have been used for over 80 years[6] and can be categorized into different types based on the material of the active layer. These types include amorphous silicon (a-Si) TFTs[5, 7, 8], polycrystalline silicon (poly-Si) TFTs[2, 9–12], metal-oxide (MO) TFTs[13–16], and organic TFTs[17, 18]. Meanwhile, a-Si TFT has gained widespread usage in the production of large-sized AM liquid crystal displays (LCDs)[19–22], primarily due to its low-cost manufacturing process. However, as AM displays move toward higher resolution, the limited mobility of a-Si TFTs is no longer sufficient to meet the requirements[23]. MO TFTs, which can offer improved mobility compared to a-Si TFTs while still maintaining a cost-effective manufacturing process, are gaining significant attention from both industry and academia[24–26]. Amorphous indium-gallium-zinc oxide (a-IGZO) TFTs[23, 25] have emerged as the first successful commercialized option among various MO TFTs thanks to their exceptional characteristics, such as high mobility, low leakage current, and steep subthreshold swing. IGZO TFTs are not only utilized in AMLCD panels[24, 25] but are also extensively employed in the drive circuitry of AM light-emitting diode (LED) display panels[26, 27].

The increasing demand for higher-quality displays has led to the need for more advanced TFT technologies to meet the requirements of AM display panels. At the same time, people are becoming increasingly aware of the environmental impact of their devices and are seeking ways to minimize their energy consumption and carbon footprint. Poly-Si TFT, despite its higher leakage current and reliance on expensive laser annealing techniques, provides a brighter screen brightness and vibrant image quality due to its higher driving current. However, using poly-Si TFT throughout the entire screen would result in high power consumption. Furthermore, producing poly-Si TFTs require the use of excimer laser annealing technology, which is expensive and time-consuming. IGZO TFT, despite its incapable of providing a high driving current due to its small mobility (~10 $cm^2/(V{\cdot}s)$)[28, 29], provides a much smaller power consumption due to its extremely low leakage current. However, using IGZO TFT throughout the entire screen could not provide enough current driving capability to realize high-quality AM displays. Therefore, a more advanced TFT technology is needed to meet these demands for performance and environmental protection. Samsung developed low-temperature polycrystalline oxide (LTPO) technology in 2018 to create a more power-efficient display[30]. This technology utilizes a-IGZO TFTs as switch devices for pixels, while low-temperature poly-Si TFTs act as driver devices for LED pixels to overcome the problem of leakage current in low-temperature poly-Si TFTs[31]. However, implementing LTPO technology necessitates the incorporation of two distinct types of TFTs, namely IGZO TFT and poly-Si TFT, on the same panel. Consequently, the LTPO process is complex and costly. Thus, the current challenge for TFTs is to find a technology that provides low leakage current and high-mobility of TFTs with low fabrication cost to meet the demand for higher-quality AM displays.

Indium-tin-zinc oxide (ITZO) TFTs are a promising alternative to IGZO TFT, offering a range of advantages such as superior optoelectronic properties, high carrier mobility, and

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lower consumption. With its larger bandgap[32, 33], ITZO TFT can achieve higher transparency in the visible light range, making it ideal for use in displays and other optoelectronic applications. ITZO TFT features high carrier mobility, facilitated by the direct spatial overlap between the 5 s orbitals of Sn and In[34], which enables easier electron carrier transport. ITZO TFT's low leakage current makes it an energy-efficient option[35], further reducing costs. Additionally, ITZO TFT's use of Sn instead of Ga makes it a more cost-effective material because Sn is more readily available. Furthermore, in terms of manufacturing, ITZO TFT can be easily integrated into existing IGZO TFT production lines, which eliminates the need for additional costs[32]. These factors make ITZO TFT a highly commercially viable option, with the potential to replace IGZO TFTs in various applications, especially in high-quality AM displays. Overall, ITZO TFT represents a significant technological advancement in the field of MO TFTs, offering superior performance and cost-effectiveness.

In the last decade, numerous studies have focused on optimizing and improving ITZO TFT, but a comprehensive review remains lacking. Thus, we have compiled the majority of studies on ITZO TFT from the past decade. With a focus on mobility as the most significant selling point of ITZO TFT, we will provide a thorough overview of the research progress made on this technology in recent years. This paper aims to analyze the advancements made in enhancing the mobility of ITZO TFTs. We will delve into the structure of the TFT and the key parameters utilized to assess its performance, emphasizing the crucial role that high-mobility TFTs play in current technology. We will then present a comprehensive overview of the most recent breakthroughs in ITZO TFT mobility, highlighting the unique innovations featured in each study. Finally, we will conclude with a concise summary and discuss future prospects for the development of ITZO mobility.

2. High-mobility ITZO TFTs and performance evaluation

TFTs typically consist of four main components: a substrate; an active layer; a dielectric layer; and source, drain, and gate components. Weimer's definition[36] classifies TFT devices into two types: coplanar and staggered. Specifically, in a staggered type the gate and source/drain are located on opposite sides of the active layer, while a coplanar type has them located on the same side, as illustrated in Fig. 1. Moreover, TFT structures can also be categorized into top-gate and bottom-gate structures, depending on the location of the gate. As a result, TFTs can be classified into four different structures based on these two classification methods, as shown in Fig. 1. In MO TFTs, the commonly used structures are the bottom-gate staggered type and the top-gate coplanar type.

As a type of field-effect transistor, TFTs can be assessed based on different electrical parameters, mainly including subthreshold swing (SS), on/off ratio, threshold voltage (V_{TH}), and mobility, which can be obtained from the device's transfer curves.

The SS indicates the sharpness of the subthreshold region in the transfer characteristic curve. It is defined as the absolute value of the change in gate-source voltage (V_{GS}) required to produce a tenfold change in drain-source current

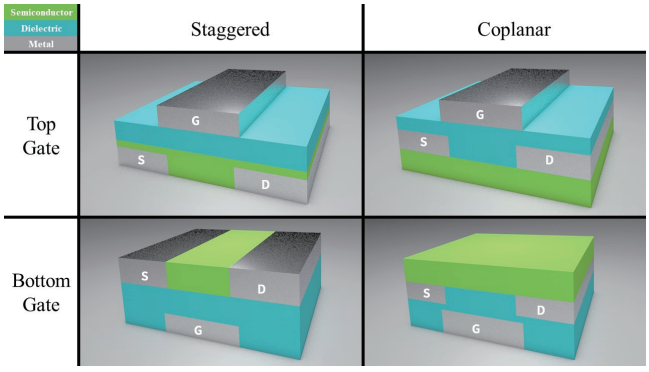


Fig. 1. (Color online) Schematic diagram of TFT structure classified according to Weimer's definition and deposition order.

(I_{DS}) at a fixed value of drain-source voltage (V_{DS}), and is expressed in units of V/decade. The SS reflects the quality of the channel and the interface between the active layer and dielectric. A lower interface defect density results in a smaller SS and faster device switching speed. The formula to calculate subthreshold swing is as follows[35]:

$$\mathrm{SS} = \left(\frac{\partial \log (I_{DS})}{\partial V_{GS}} \bigg|_{\max} \right)^{-1}. \tag{1}$$

The on/off ratio is another essential indicator of a TFT's performance and is normally calculated as the ratio of the maximum I_{DS} (I_{on}) to the minimum I_{DS} (I_{off}) in the transfer characteristic curve[35]. Once the I_{on} and I_{off} are defined, the on/off ratio can be determined.

The V_{TH} is the voltage value that indicates the transition of a device from the off state to the on state. It refers to the V_{GS} at which the device forms a conductive channel. Various methods[37] can be used to determine the V_{TH}, but the most commonly used method defines it as the gate voltage corresponding to a specific I_{DS}. However, the I_{DS} is affected by V_{DS} and the channel's width-to-length ratio (W/L). Therefore, the V_{TH} is usually defined using the following formula:

$$I_{TH} = I_{DS} / \left(\frac{W}{L} \right), \tag{2}$$

$$V_{TH} = V_{GS} \left(I_{TH} = 1\ \mathrm{nA}, V_{DS} = 0.1\ \mathrm{V} \right), \tag{3}$$

$$V_{TH} = V_{GS} \left(I_{TH} = 10\ \mathrm{nA}, V_{DS} = 5\ \mathrm{V} \right), \tag{4}$$

$$V_{TH} = V_{GS} \left(I_{TH} = 100\ \mathrm{nA}, V_{DS} = 10\ \mathrm{V} \right), \tag{5}$$

where I_{TH}, W, and L are, respectively, the normalized I_{DS}, channel width, and channel length.

The parameter of mobility characterizes the movement of charge carriers in the channel, and is primarily influenced by the thin film's quality and the active layer's interface with the dielectric. It can be used to indirectly assess the active layer's quality. There are two commonly used methods[37] for extracting mobility. In the linear region ($V_{DS} \ll V_{GS} - V_{TH}$), the linear field-effect mobility (μ_{fe}) can be calculated using the linear current equation and the transconductance (g_m) of the TFT through:

$$I_{DS} = \frac{W}{L}\mu_{fe}C_{OX}\left[\left(V_{GS} - V_{TH}\right)V_{DS} - \frac{1}{2}V_{DS}^{2}\right], \quad (6)$$

$$\mu_{fe} = \frac{\partial I_{DS}/\partial V_{GS}}{C_{OX}\frac{W}{L}V_{DS}} = \frac{g_m}{C_{ox}\frac{W}{L}V_{DS}}, \quad (7)$$

where C_{ox} is the gate insulator capacitance per unit area. When the device is operated in the saturation region ($V_{DS} > V_{GS} - V_{TH}$), its transfer curve is generally measured at a relatively large V_{DS}. In this case, the saturation region current equation is used to calculate the saturation mobility (μ_{sat}) through:

$$I_{DS} = \frac{1}{2}\frac{W}{L}\mu_{sat}C_{OX}\left(V_{CS} - V_{TH}\right)^2, \quad (8)$$

$$\mu_{sat} = \frac{\left(d\sqrt{I_{DS}}/d\sqrt{V_{GS}}\right)^2}{\frac{1}{2}\frac{W}{L}C_{OX}}. \quad (9)$$

TFTs with high mobility typically exhibit a small SS and a large I_{on}. As depicted in Fig. 2, a traditional two transistors one capacitor (2T1C) pixel driving circuit of AMOLED comprises two TFTs, a capacitor, and an LED. For high refresh rate, high resolution, and high brightness AMOLED displays, the T_1 transistor necessitates fast switching speeds (i.e., a small SS), a large I_{on} for rapid capacitor charging, and a small I_{off} to minimize the potential drop of the capacitor within a single frame time. The T_2 transistor requires a large I_{on} to achieve higher OLED excitation brightness. Both small SS and large I_{on} typically correspond to high mobility. Therefore, ITZO TFTs are well-suited for meeting these requirements.

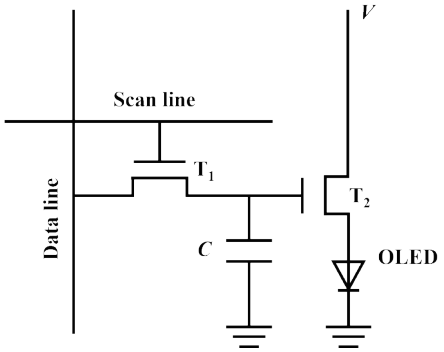


Fig. 2. Schematic of 2T1C.

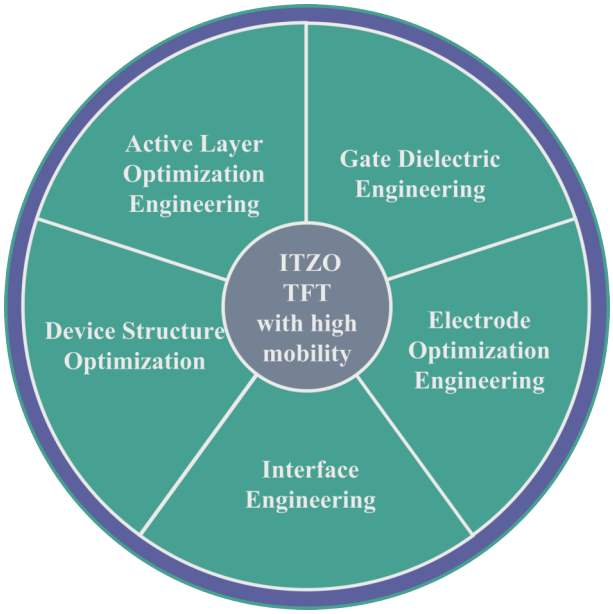


Fig. 3. (Color online) Classification of the method to improve ITZO TFT mobility.

3. Advances in high-mobility ITZO TFTs

As a promising candidate for high-mobility TFTs that could potentially be widely used in the future, ITZO TFT has been extensively studied for performance optimization[38–91]. These efforts, as depicted in Fig. 3, can be broadly categorized into five areas: active layer optimization[38–62], gate dielectric optimization[64–73], electrode optimization[74, 75], interface optimization[77–84], and device structure optimization[85–91].

3.1. Active layer optimization engineering

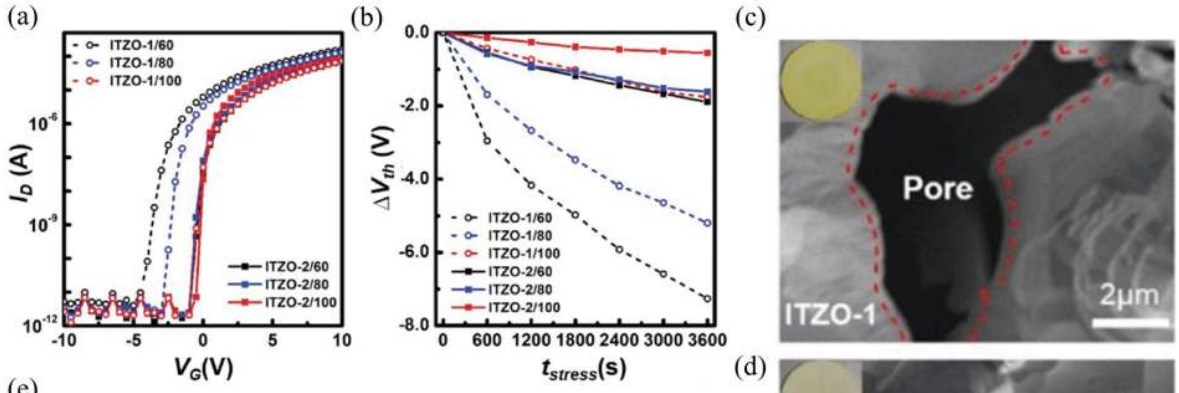
Three main strategies are normally employed to optimize the active layer of ITZO TFTs: optimizing the film preparation process[38–49], doping the film[50–55], and post-treating the film[56–62]. A summary of active layer optimization is shown in Table 1.

3.1.1. Optimization of deposition technology

ITZO film is typically prepared using sputtering deposition[38–43]. Researchers have focused on improving the quality of sputtered ITZO films to enhance their mobility for years. In 2013, Jang *et al.*[38] conducted an experiment that showed the close relationship between the quality of sputtered ITZO films and the oxygen (O_2) ratio in the gas used. Although there were slight differences in the proportions of the three elements in the films sputtered at different O_2 ratios, these differences had a significant impact. The content of In element showed a trend of first decreasing and then increasing with the increase of O_2 ratio. When the proportion of In element was the lowest, the performance of the device obtained by sputtering was the best, with a mobility of 37.2 cm^2/(V·s) and an SS of 0.93 V/dec. In 2014, Kim *et al.*[39] co-sputtered ITZO TFTs using ITO and ZTO targets to further explore the effect of In element on device performance under large variations in content. This experiment showed that increasing In element content improved the device mobility. Furthermore, increasing In element content brought a negative V_{TH} shift. Appropriate In element doping can improve the stability and mobility of the device by promoting the formation of Sn^{2+}–O^{2-} bonds in ITZO films, compensating for the oxygen vacancies in ITZO films. The final prepared ITZO TFT had a mobility larger than 30 cm^2/(V·s). In 2018, Park *et al.*[40] compared ITZO TFT devices sputtered at different O_2 ratios and found that an increase in O_2 ratio significantly inhibited the content of oxygen vacancies in the film. Oxygen vacancies, as common carrier donors in MO films, can make the device easier to turn on and result in a larger negative V_{TH} shift when there are too many oxygen vacancies. In 2021, Wu *et al.*[41] explored the relationship between target quality and device performance. The experimental results showed that using targets with higher density and better crystallinity can achieve high mobility while maintaining good stability for ITZO TFTs. Serious preferential sputtering occurs when sputtering low-density targets, which makes the particles stack on the substrate in a more disorderly manner. By using high-density tar-

Table 1. Summary of active layer optimizations for ITZO TFTs.

	Methods	Material	*W*/*L* (μm)	*T* (°C)	μ (cm²/(V·s))	SS (V/dec)	V_{TH} (V)	Year	Ref.
AC film preparation	Sputtering	ITZO	150/25	350	37.2	0.93	N.A.	2013	[38]
	Sputtering	ITZO	500/50	350	36.9	0.30	3.8	2014	[39]
	Sputtering	ITZO	500/100	350	47.3	1.26	−0.6	2018	[40]
	Sputtering	ITZO	800/400	350	36.1	0.13	−0.03	2021	[41]
	Sputtering	ITZO	1000/200	300	30.8	1.00	0.4	2015	[42]
	Sputtering	ITZO	50/5	300	27.9	0.20	0.52	2017	[43]
	Inkjet printing	ITZO	1400/200	600	30.0	N.A.	2.0	2009	[44]
	Solution	ITZO	200/1000	600	4.36	0.53	2.1	2011	[45]
	Solution	ITZO	20/10	300	9.5	0.08	0.51	2019	[46]
	ALD	ITZO	40/20	350	27.8	0.28	−1.2	2019	[47]
	ALD	ITZO	N.A.	400	22.0	0.15	0.8	2019	[48]
	USPD	ITZO	200/15	N.A.	43.84	0.09	0.5	2020	[49]
Doping	Sputtering	ITZO:Li	70/70	325	39.1	N.A.	0.4	2018	[50]
	Sputtering	ITZO:Li	N.A.	325	39.4	N.A.	2.2	2019	[51]
	Sputtering	ITZO:Y	1000/100	500	0.20	0.07	3.7	2019	[52]
	Sputtering	ITZO:Pr	800/400	350	20.9	0.27	0.39	2022	[53]
	Sputtering	ITZO:N	1500/150	250	17.53	0.36	−8.2	2018	[55]
Post treatment	Sputtering	ITZO	N.A.	400	39.6	0.25	−2.8	2014	[56]
	Sputtering	ITZO	300/300	300	27.4	0.23	−0.64	2018	[57]
	Sputtering	ITZO	1000/50	150	9.8	0.82	1.93	2020	[58]
	Sputtering	ITZO	1000/500	700	33.6	0.26	0.83	2020	[59]
	Sputtering	ITZO	800/600	400	53.2	0.18	−0.21	2021	[60]
	Sputtering	ITZO	60/50	300	83.2	0.15	0.14	2023	[61]



(e)

Target	*P* (W)	V_{th} (V)	*SS* (V/dec)	μ_{FE} (cm²/Vs)	I_{on}/I_{off}	ΔV_{th} (V)
ITZO-1	60	-3.26±0.3	0.37	35.6±1.4	4.52×10^7	-7.26
	80	-2.08±0.6	0.23	29.1±1.1	2.63×10^8	-5.19
	100	-0.23±0.4	0.19	22.7±1.4	1.48×10^8	-1.78
ITZO-2	60	-0.12±0.5	0.38	23.6±0.6	1.69×10^8	-1.89
	80	-0.26±0.7	0.31	26.4±1.0	2.03×10^8	-1.76
	100	-0.03±0.2	0.13	36.1±1.0	2.47×10^8	-0.55

(f)

Target	In:Sn:Zn (at.ratio)	Relatively Density (%)	Resistance (kΩ)
ITZO-1	0.46:1.00:1.00	64	20.1
ITZO-2	0.47:1.01:1.00	83	16.4

Fig. 4. (Color online) (a) Transfer characteristics at V_{DS} = 10.1 V, (b) stress-time dependent variation of ITZO TFTs (fabricated by ITZO-1 and ITZO-2 at different powers (60, 80, and 100 W)) at NBS (–20 V, 3600 s). (c) SEM pattern of ITZO-1. (d) SEM patterns of ITZO-2. (e) Table of film properties and deposition parameters. (f) Table of physical parameters of the target[41]. (a)–(f), © 2021 IEEE. Reprinted, with permission, from Ref. [41].

gets and appropriate power, the final prepared ITZO TFTs had a mobility of up to 36.1 cm²/(V·s) and a V_{TH} shift of only –0.55 V under negative bias stress (NBS) of –20 V for 3600 s (Fig. 4).

Besides the sputtering deposition methods, other methods[44–49] have also been explored for optimizing film quality. In 2009, Lee *et al.*[44] used inkjet printing to prepare ITZO TFT on a glass substrate, with a mobility of 30 cm²/(V·s) and a

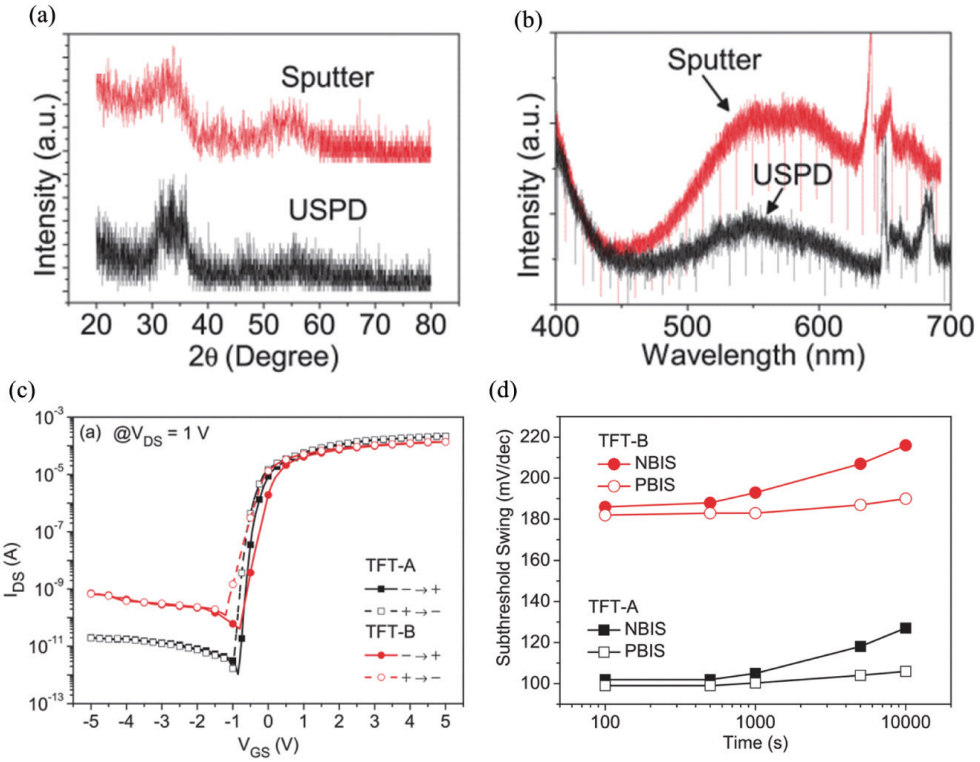


Fig. 5. (Color online) (a) XRD patterns of USPD- and sputter-deposited ITZO films. (b) PL spectra of USPD- and sputter-deposited ITZO films. (c) Hysteretic I_{DS}-V_{GS} characteristics of TFT-A (USPD-deposited) and TFT-B (sputter-deposited). (d) SS versus stress time (NBIS and PBIS) characteristics of TFT-A and TFT-B[49]. (a)–(d), © 2020 IEEE. Reprinted, with permission, from Ref. [49].

V_{TH} close to 2 V. However, its high annealing temperature (600 °C) and poor SS require further optimization. In 2011, Kim *et al.*[45] used the same precursor solution as inkjet printing to prepare ITZO TFT by spin-coating. Its mobility was 4.36 cm^2/(V·s) and the film annealing temperature was still high at 600 °C. Both methods[44, 45] require high V_{DS} > 30 V for better performance. In 2019, Bukke *et al.*[46] found that purifying the precursor solution could improve the performance of ITZO devices prepared by spin-coating, achieving a relatively high mobility of 9.50 cm^2/(V·s), near-zero V_{TH} (0.51 V), small SS (0.087 V/dec), high stability, and a low preparation temperature (300 °C). In 2019, Sheng *et al.*[47] employed atomic layer deposition (ALD) to fabricate ITZO films. They deposited ZnO, SnO, and InO using multiple deposition subcycles. Among the different combinations tested, the ITZO TFTs prepared with one In-O cycle, one Zn-O cycle, and one Sn-O cycle demonstrated the highest performance. These devices exhibited a mobility of 27.8 cm^2/(V·s) and a V_{TH} of −1.2 V. In the same year, Beak *et al.*[48] used ALD to prepare ITZO TFT and found that the device reached optimal performance under the condition of In/Zn/Sn = 10 : 70 : 20 and annealed at 400 °C, achieving a mobility of 22 cm^2/(V·s), an SS of 0.15 V/dec, and a V_{TH} of 0.8 V. In 2020, Liu *et al.*[49] successfully prepared high-quality ITZO TFTs by ultrasonic spray pyrolysis deposition, achieving a high mobility of 43.84 cm^2/(V·s) and an SS of 0.0974 V/dec, exceeding the performance of the traditional spin-coating method and even the widely used sputtering method (Fig. 5).

3.1.2. Doping

On traditional silicon, doping is used to regulate its conductivity[50–55]. However, in MOs, doping plays a different role in balancing mobility and stability. In 2018, Li *et al.*[50] doped lithium (Li) into ITZO thin films and discovered that Li could regulate oxygen vacancies. This reduced scattering centers and increased mobility, resulting in the mobility of 39.1 cm^2/(V·s). However, even after the process was optimized[51], a negative V_{TH} shift remained. In 2019, Zhang *et al.*[52] doped Yttrium (Y) into the active layer of ITZO TFTs using a solution process. Stability tests showed that the stability of ITZO:Y TFTs improved with an increase in the concentration of doped Y, while the mobility decreased. This happened because Y doping suppresses defects, resulting in better SS, but at the cost of reduced mobility due to the consumption of oxygen vacancies. In 2022, Zhang *et al.*[53] doped praseodymium (Pr) into ITZO TFTs using sputtering, significantly improving their stability while sacrificing only a small amount of mobility. In 2017, Jia *et al.*[54] introduced nitrogen (N) during the sputtering of ITZO thin films, resulting in the formation of InN nanocrystalline phases, which increased device mobility. Li *et al.*[55] also found crystallization in ITZO TFTs by introducing nitrogen during their preparation. However, the thick film caused scattering effects from increased carriers, while the presence of oxygen vacancy defects suppressed SS and mobility.

3.1.3. Post-treatment

After the film preparation, post treatments[56–62] are often necessary to repair the thin film and activate the rearrangement of atoms inside it, achieving a more ordered state. Annealing[56–58], as the most commonly used post-treatment, requires optimization in various aspects, mainly including temperature, time, and atmosphere. Fhu *et al.*[56] investigated the relationship between the ITZO TFT prepared by sputtering and the annealing temperature. They observed that as the annealing temperature increases, the degree of repair of

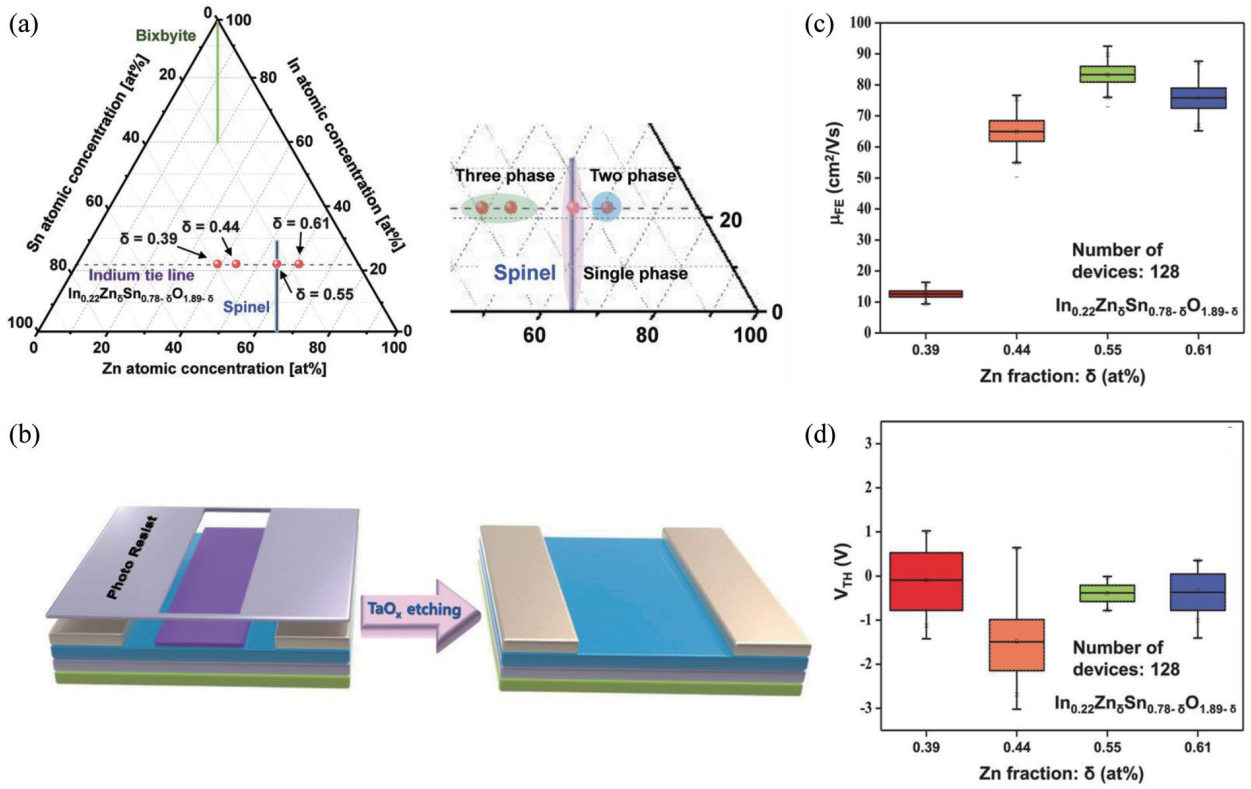


Fig. 6. (Color online) (a) $InO_{0.5}$–ZnO–SnO_2 phase diagram. (b) Schematic of IZTO TFT after RIE etching. Box plots of (c) μ_{fe} and (d) V_{TH} for devices with different Zn fractions[61]. (a)–(d), Ref. [61], John Wiley & Sons. [© 2023 Wiley-VCH GmbH].

internal defects in the thin film gradually increases, which in turn enhances the device mobility. They also found that increasing the temperature inhibits the defect density inside the thin film, leading to a significant increase in the characteristic trapping time of carriers, thereby establishing a proportionality between device mobility and annealing temperature. Furthermore, Zhong *et al.*[57] provided partial evidence supporting this conclusion through X-ray photoelectron spectroscopy (XPS) and photoluminescence (PL) characterization techniques. It has also been observed in experiments that excessively high temperatures can lead to the generation of more defects due to the presence of weak bonds inside the thin film. These bonds can easily be broken at high temperatures, causing the formation of new defects. Ultimately, the optimal annealing temperature for ITZO TFT was determined to be 300 °C, which is also the temperature that is commonly used in most ITZO TFT reports. Devices fabricated under these conditions exhibit a high mobility of 27.4 $cm^2/(V·s)$, a low V_{TH} of 0.64 V, and a steep SS of 0.23 V/dec.

Rapid thermal annealing (RTA), as a relatively new post-treatment technology, has been welcomed because it can reach high temperatures in a short time and control the gas atmosphere more accurately. In 2020, Maeng *et al.*[58] conducted a study on the impact of O_2 pressure during the post-treatment of ITZO TFT by RTA. Their research revealed that the amount of oxygen vacancies is directly proportional to the O_2 pressure, and as a result the device's mobility decreases.

In 2020, Park *et al.*[59] investigated the relationship between the device performance and high annealing temperature. Their study revealed that when the ITZO TFT was annealed at a temperature of 700 °C, clear crystallization phenomena were observed in the transmission electron microscope (TEM) image. TFTs prepared under this condition showed high mobility of 33.6 $cm^2/(V·s)$ and a V_{TH} value very close to 0 V (0.83 V). Although TFTs are typically prepared at low temperatures, Park *et al.*'s research provided initial insights into the mobility and stability of ITZO TFTs after crystallization. Wang *et al.*[60] used a different approach called metal-induced crystallization (MIC) to crystallize ITZO. They coated a 15 nm layer of aluminum (Al) metal on the back-channel surface of the ITZO TFT and annealed it below 400 °C. TEM images showed clear crystallization phenomena. This occurred because Al can easily oxidize and generate aluminum oxide (Al_2O_3) with the O_2 inside the thin film, releasing electrons that break weak internal bonds of the thin film, which then rearrange at higher temperatures to achieve crystallization. The ITZO TFT prepared at 400 °C had a high mobility of 53.2 $cm^2/(V·s)$. Similarly, Kim *et al.*[61] utilized tantalum (Ta) as an inducing element for MIC. As a potent reducing agent, Ta has a comparable effect as Al in breaking weak bonds inside the thin film and rearranging them at high temperatures. Different element ratios tend to produce different types and quantities of crystal lattice structures after rearrangement. Therefore, by optimizing the element ratio of the ITZO thin film, a single orientation of crystallization can be achieved. It was found that the best electrical performance of the device was achieved when the In : Zn : Sn ratio was 22 : 55 : 23, resulting in a mobility of over 80 $cm^2/(V·s)$ and very high stability (Fig. 6).

3.2. Gate dielectric engineering

Gate dielectric, as a critical component that strongly affects the gate control of the channel, has been extensively

Table 2. Summary of gate dielectric engineering for ITZO TFTs.

Methods	Dielectric	W/L (μm)	T (°C)	μ (cm^2/(V·s))	SS (V/dec)	V_{TH} (V)	Year	Ref.
Sputtering	HfO_2	480/120	400	18.9	0.48	−4.64	2022	[64]
Sputtering	Al_2O_3	50/50	350	17.1	0.15	N.A.	2013	[65]
Sputtering	Al_2O_3	200/200	250	31.08	0.096	0.28	2016	[66]
Sputtering	ZrO_2	500/50	300	40.7	0.126	−0.05	2018	[68]
Solution process	ZrO_2	50/10	300	15.42	0.087	N.A.	2018	[69]
Solution process	HZO	50/10	300	4.76	0.07	N.A.	2018	[70]
Sputtering	$ZrSiO_x$	40/20	350	28.6	0.15	−0.4	2019	[71]
Sputtering	ZS8	40/20	N.A.	27.7	0.17	−1.1	2020	[72]
Sputtering	C8-SAM/Al_2O_3	300/300	300	13.7	0.2	1.0	2022	[73]

studied for its impact on the performance of the channel[63], as well as its compatibility with ITZO[64–73]. The high-quality gate dielectric is typically characterized by a higher degree of density and a smoother film surface. Thinning down the gate insulator layer can enhance the gate-control ability over the channel; however, if the layer is too thin, it can result in large leakage currents. Therefore, high-k materials are commonly employed as gate dielectrics. In this section, we will present and discuss the research related to gate insulation layer engineering in ITZO TFTs, as summarized in Table 2.

Al_2O_3 is commonly used as high-k dielectric in ITZO TFTs[65, 66]. In 2013, Jiang *et al*.[65] compared silicon nitride (Si_3N_4) and Si_3N_4/Al_2O_3 as gate dielectrics for ITZO TFTs. Although the two materials have similar relative dielectric constants, Al_2O_3 has a denser and smoother surface due to the fabrication process, resulting in higher device mobility and stability. A smoother and denser surface can introduce fewer defects in the channel, reducing the probability of carrier scattering and thus improving device mobility. In 2016, Raja *et al*.[66] found that soaking the Al_2O_3 thin film in a hydrogen peroxide solution could effectively reduce the defects inside the film, resulting in a certain increase in both mobility and SS.

Zirconium oxide (ZrO_2) has been extensively investigated as an insulating layer in ITZO TFTs[68–72]. This is due to its high relative dielectric constant of 25, which surpasses that of Al_2O_3[67]. In 2018, Ruan *et al*.[68] conducted a study on ITZO TFTs with three different insulating layers: hafnium oxide (HfO_2), ZrO_2, and Al_2O_3. The authors showed that ITZO TFTs with ZrO_2 gate insulators exhibited a steep SS of 0.126 V/dec and a high mobility of 40.7 cm^2/(V·s), while HfO_2, which has a similar dielectric constant, showed a mobility of 16.1 cm^2/(V·s). The ZrO_2 thin film used in the process had more oxygen vacancies, which can capture O_2 from the active layer and increase the oxygen vacancy concentration in the channel after the film is fabricated into a TFT. This leads to a slightly degraded SS in ZrO_2-ITZO TFTs compared to HfO_2-ITZO TFTs. However, this degradation is acceptable compared to the improvement in mobility. In 2018, Bukke *et al*.[69] found that purifying the precursor solution of ZrO_2 and spin-coating it could improve the quality of the gate insulator film in solution-processed ITZO TFTs because the ZrO_2 thin film prepared by spin-coating the purified solution has a smoother surface, which reduces the defects inside the channel and ultimately leads to a significant improvement in mobility. In the same year, Bukke *et al*.[70] also introduced hafnium alloy into ZrO_2 thin films, which also led to a smoother surface and improved mobility. In 2019, Kim *et al*.[71] compared ITZO TFTs fabricated with ZrO_2 and zirconium silicate ($ZrSiO_x$) as gate-insulating layers. They found that although ZrO_2 has a high dielectric constant, its thin film surface is relatively rough, leading to a large leakage current due to crystallization. In $ZrSiO_x$, the introduction of Si can effectively inhibit the crystallization of ZrO_2, resulting in a sufficiently smooth thin film surface. Therefore, ITZO TFTs with $ZrSiO_x$ as the insulating layer had the highest mobility, the smallest SS, and the highest stability among the three materials. Choi *et al*.[72] adopted another approach to address the high surface roughness of ZrO_2 thin films. Although silicon oxide (SiO_2) has a lower dielectric constant, its smooth thin film surface can help to form better-quality conductive channels. Therefore, a series-connected gate dielectric layer consisting of SiO_2 and ZrO_2 was used to obtain a surface-smooth and high-dielectric-constant gate insulator. Ultimately, they found that depositing 8 nm of SiO_2 on ZrO_2 resulted in the highest mobility of 27.7 cm^2/(V·s) and the best stability (Fig. 7). In 2022, Zhong *et al*.[73] used a similar method to spin-coat organic compound triethoxysilane-based self-assembled monolayers with eight alkyl on Al_2O_3, which significantly suppressed the surface roughness of the film, reduced the oxygen vacancies on the film surface, and ultimately improved the mobility and stability of the device to a certain extent.

3.3. Electrode optimization engineering

The contact between the source and drain electrodes and the active layer, serving as the emission and collection ports of channel electrons, is a critical aspect of this debate that is worth exploring. However, there has been little research conducted on this aspect for ITZO TFT electrodes[74, 75]. In 2015, Park *et al*.[74] conducted a comparison of nickel (Ni), indium tin oxide (ITO), and Al electrodes' compatibility with ITZO TFTs. The authors showed that Ni has the smallest contact resistance with ITZO due to the closest work function match, resulting in the best I_{on} performance (Figs. 8(a) and 8(b)). Conversely, the use of Al electrodes resulted in lower open-state current and more severe negative V_{TH} shift. In 2020, the same research group[75] carried out a more detailed investigation into this issue. They discovered that O_2 from the thin film diffuses into the electrode, resulting in the formation of Al_xO_y and nickel oxide (NiO_x) on the contact surface between the electrode and the active layer when using Al as the electrode. Compared to NiO_x, Al_xO_y has a higher oxygen vacancy concentration, which quickly diffuses into the channel after annealing, resulting in a surge in channel carrier concentration and leading to negative V_{TH} shift (Figs. 8(c) and 8(d)).

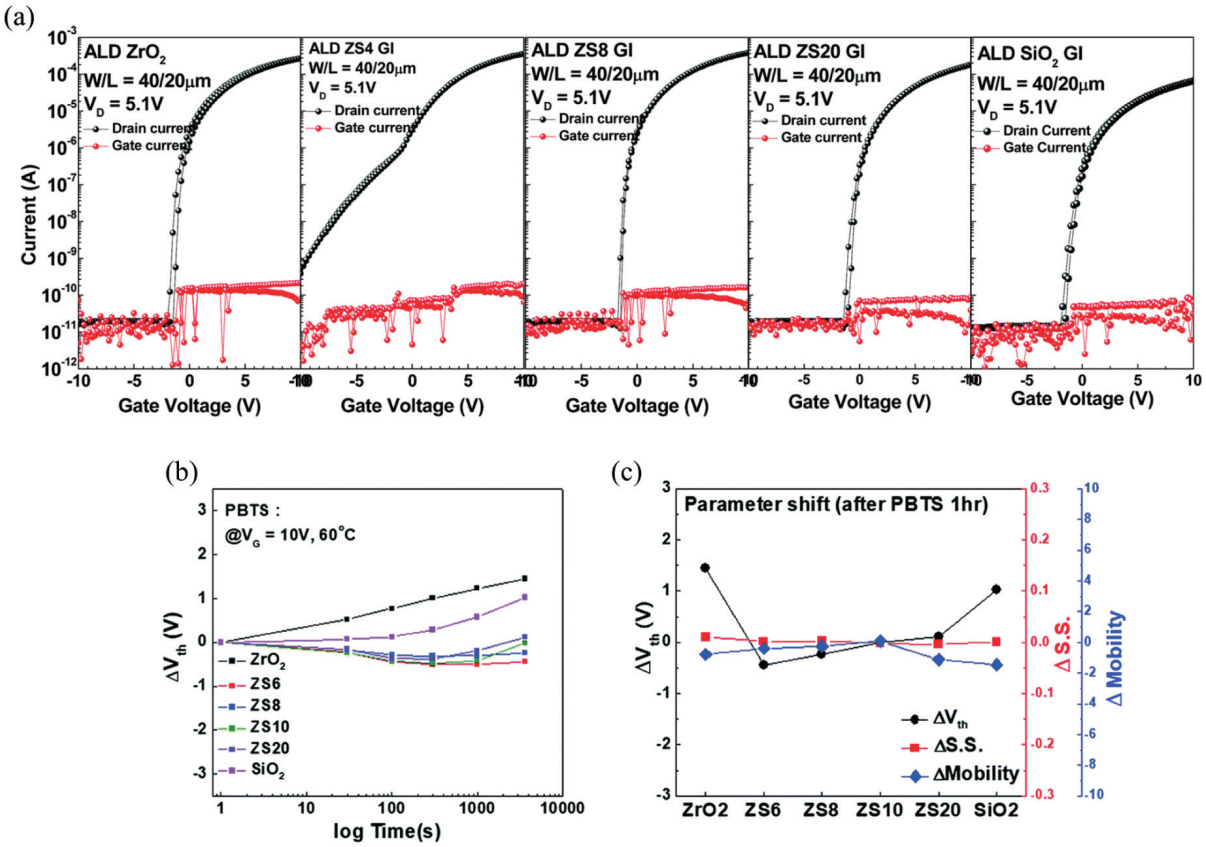


Fig. 7. (Color online) (a) Representative transfer characteristics depending on the thickness combination of ZrO_2/SiO_2 films. (b) V_{TH} shift during PBTS test. (c) Parameter shift of each TFT after 3600 s of PBTS test[72]. (a)–(c), used with permission of Royal Society of Chemistry, reprinted from Ref. [72] , 2020.

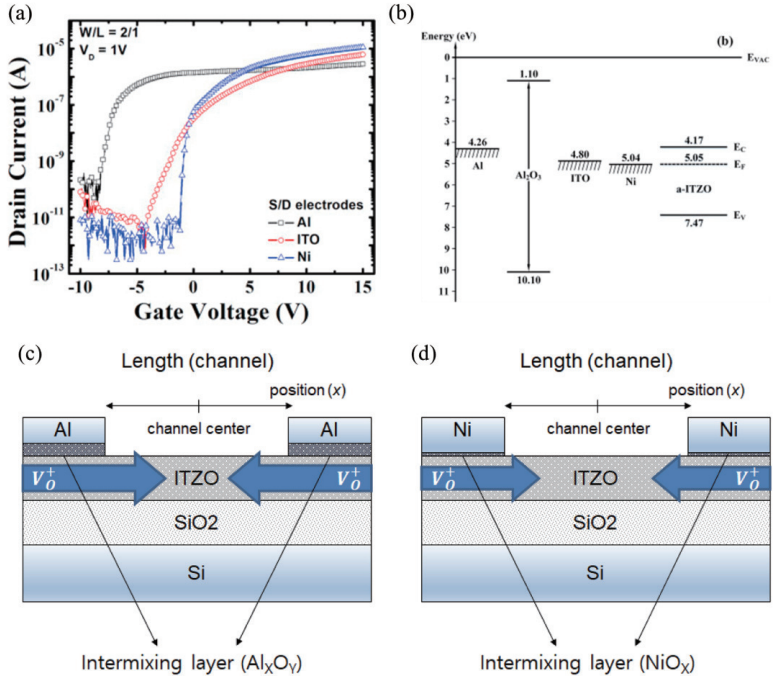


Fig. 8. (Color online) (a) Transfer characteristics (at V_{DS} = 1 V) of ITZO TFTs with different S/D contacts; (b) schematic band diagram for ITZO TFT with Al, ITO, and Ni electrodes[74]. (a) and (b) reprinted from Ref. [74], Copyright (2015), with permission from Elsevier. (c) Schematics of the diffusion of oxygen vacancies in the ITZO layer from Al S/D electrodes[75]. (d) Schematics of the diffusion of oxygen vacancies in the ITZO layer from Ni S/D electrodes[75]. (c) and (d) Reprinted from Ref. [75], Copyright (2020), with permission from Elsevier.

3.4. Interface engineering

High-mobility MO semiconductors tend to have deeper conduction band bottom energy levels[32]. This makes them more vulnerable to impurities and moisture at the back channel, which can reduce stability under continuous stress. Additionally, hanging bonds at the back channel can easily be

Table 3. Summary of backchannel interface optimization for ITZO TFTs.

Methods	Dielectric	Passivation	*W*/*L* (μm)	*T* (°C)	μ (cm²/(V·s))	SS (V/dec)	V_{TH} (V)	Year	Ref.
Sputtering	AlO_x:Nd	C18-SAM	300/300	300	22.9	0.077	−0.1	2018	[77]
Sputtering	AlO_x:Nd	OTES SAMs	300/300	300	19.4	0.09	0.6	2020	[78]
Sputtering	AlO_x:Nd	ODA SAMs	300/300	350	19.89	0.152	−0.6	2021	[79]
Solution process	ZrO_2	Y_2O_3	50/5	350	4.75	0.114	0.42	2016	[80]
Sputtering	AlO_x:Nd	Sc_2O_3	300/300	300	16.4	0.09	1.0	2021	[81]
Sputtering	SiO_2	GaO_x	60/30	400	58.3	0.087	−0.7	2022	[82]
Sputtering	SiO_2	N.A.	60/30	400	~50	N.A.	N.A.	2021	[83]

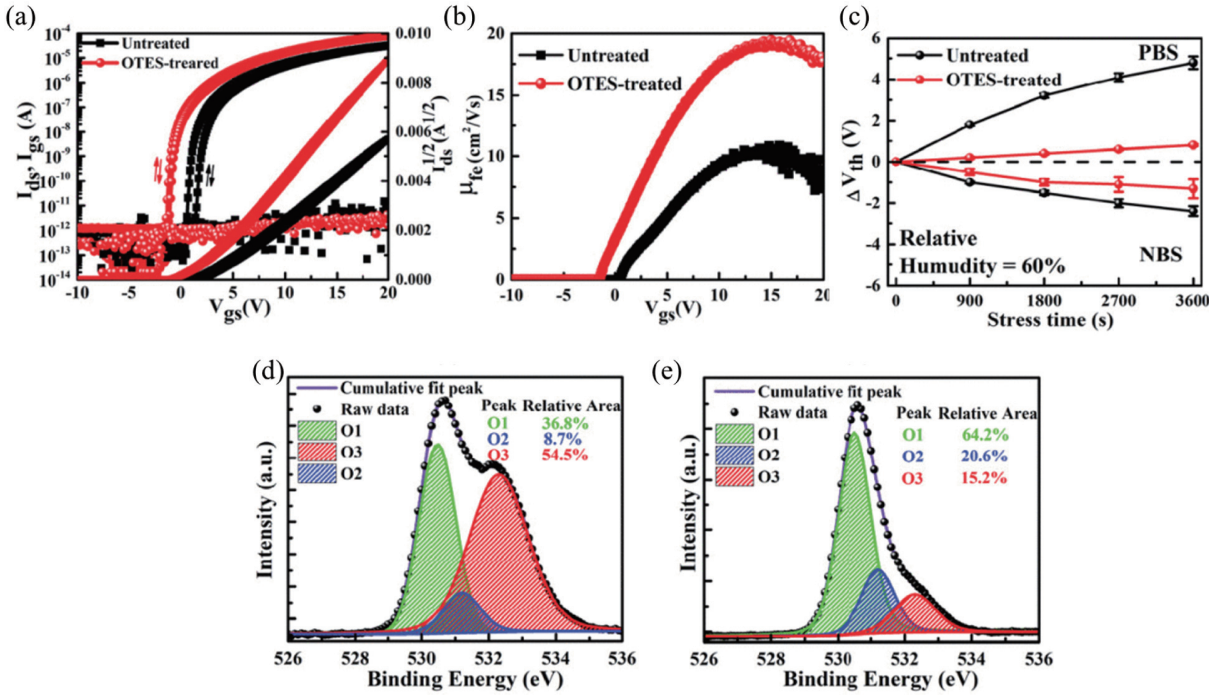


Fig. 9. (Color online) (a) Transfer characteristics of untreated and OTES-treated ITZO TFTs on PI substrates. (b) Plot of μ_{fe} as a function of gate bias. (c) Variations in threshold voltage shift for untreated and OTES-treated ITZO TFTs, as a function of stress time under separate gate bias voltages of 10 and −10 V. XPS spectra of O 1*s* peaks of (d) untreated and (e) OTES-treated ITZO films[78]. (a)–(e), © 2020 IEEE. Reprinted, with permission, from Ref. [78].

trapped by electron traps formed by moisture and other substances in the air, resulting in poor initial device performance. The most common approach to improve the back channel is to add a passivation layer to isolate water and O_2 and eliminate hanging bonds[77–84]. In this section, we will showcase the advancements in optimizing the back-channel interface of ITZO TFTs, highlighting the outcomes of these endeavors (Table 3).

In recent years, numerous studies[77–79] have focused on passivation layers to improve the stability of high-mobility MO semiconductors, which are often prone to the effects of impurities and moisture at the back channel. Among these studies, self-assembled monolayers (SAMs) have emerged as a promising option due to their chemical and physical resistance, and ability to withstand thermal annealing and plasma treatment[76]. However, the most suitable type of SAMs for passivation layers in ITZO TFTs remains an area of ongoing research. In 2018, Zhong *et al.*[77] investigated the feasibility of using three different alkyl chain length triethoxysilane-based SAMs as passivation layers for ITZO TFTs. They found that hydrophobic SAMs spin-coated at the back channel can effectively block the adhesion of moisture and other substances, leading to improved stability of the device. In 2020, they used the method of gas-phase deposition to prepare n-octyltriethoxysilane SAMs (OTES) as a passivation layer and obtained similar results[78] (Fig. 9). In 2021, Chen *et al.*[79] prepared octadecylamine as the passivation layer on the back-gate channel of ITZO TFT using evaporation and explored the relationship between evaporation time and the device's electrical properties and stability. They found that longer evaporation times improved hydrophobicity, mobility, and stability, but also caused a negative V_{TH} shift. It should be noted that the SAMs are usually organic, which is incompatible with the industry production lines of AM displays.

Apart from SAMs, many inorganic materials can also be utilized as passivation layers to enhance the performance of ITZO TFTs[80–82]. In 2016, Bukke *et al.*[80] prepared Yttrium oxide (Y_2O_3) as a passivation layer by spin-coating it onto the back-gate channel of ITZO TFTs. The authors found that Y_2O_3 not only served as a passivation layer but also diffused Y elements partially into the ITZO thin film, playing a doping role. XPS characterization results indicated that Y_2O_3 passivation reduced the oxygen vacancy of the device, increased the M–O–M bond content, and suppressed oxygen vacancy defects by doping Y elements, thereby improving the mobility and SS of the device. In 2021, Zhong *et al.*[81] investigated

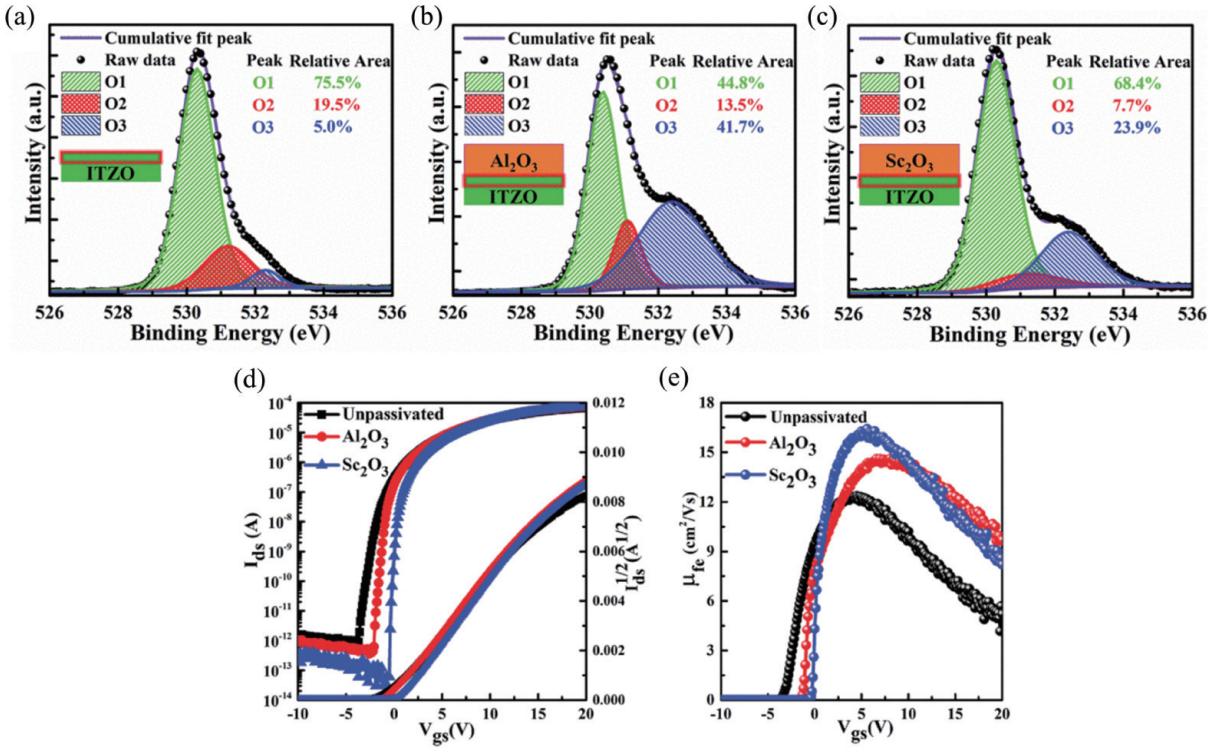


Fig. 10. (Color online) O 1*s* spectra of the back channel of the ITZO TFTs (a) without a PVL, (b) with an Al_2O_3 passivation layer, and (c) with a Sc_2O_3 passivation layer. (d) Transfer characteristics of the ITZO TFTs with no passivation layer, Al_2O_3 passivation layer and Sc_2O_3 passivation layer. (e) Plot of μ_{fe} as a function of gate bias[81]. (a) –(e), © 2021 IEEE. Reprinted, with permission, from Ref. [81].

the use of Al_2O_3 and scandium oxide (Sc_2O_3) as passivation layers for ITZO TFTs and compared their performance. The results showed that Sc_2O_3 had a greater ability to isolate water vapor and air than Al_2O_3 and had fewer oxygen vacancies at the back-gate channel interface (Fig. 10). Thus, ITZO passivated by Sc_2O_3 had higher mobility and stability. In 2022, Shi *et al*.[82] used GaO as a passivation layer for ITZO TFTs and developed a tetramethyl ammonium hydroxide (TMAH) developer that could simultaneously etch ITZO and GaO. The TMAH developer's development reduced the preparation process's complexity by reducing the two mask patterns to one. The mobility and stability of the device were also significantly enhanced due to the coverage of the GaO passivation layer.

In 2021, Shiah *et al*.[83] found that impurities on the surface of the back channel also need to be removed before adding a passivation layer. They found that C-related impurities, originating from photoresist and remaining at the back channel during lithography, are the main cause of NBS instability in these devices. The study suggests that these impurities can be eliminated by additional UV ozone treatment (Fig. 11).

3.5. Device structure optimization

Another major research focus is to enhance device performance by modifying the device structure. There are diverse solutions in this field, which can generally be divided into two categories: the first is to make structural adjustments only on the simple ITZO TFT[85–88], and the second is to introduce other materials as auxiliaries[89–91].

When reducing the size of device features, device performance, such as mobility, can often deteriorate. Structural optimization can help to improve this. In 2017, Xia *et al*.[85] developed the elevated-metal metal-oxide (EMMO) structure for ITZO TFTs. This structure cleverly utilizes the difference in permeability between SiO_2 and MO. After depositing a layer of SiO_2 on IGZO and defining the source-drain metal, O_2 enters the ITZO through the permeable SiO_2 to repair defects, while the non-permeable metal covering ITZO exhibits very low resistivity and becomes conductive (Fig. 12(d)). In contrast to the original etch stop (ES) structure, defining the *L* through the distance between the electrodes can not only retain the ES layer to reduce the degradation of device performance but also obtain a smaller *L*, thereby reducing the device area (Figs. 12(a)–12(c)). However, shortening *L* can cause hydrogen in the passivation layers, such as alumina, to diffuse into the channel after annealing. When the *L* is too short, the gate loses its ability to control the channel due to the increased conductivity of the active layer. In 2021, Kim *et al*.[86] addressed this issue by developing a self-aligned ITZO TFT with a trench structure. Due to the roughness inside the trench, especially the sidewalls, the interior of the groove still maintains a high resistivity. At higher temperatures, the device can still maintain its switching performance. The mobility of the device can reach nearly 100 $cm^2/(V{\cdot}s)$ at 270 °C annealing while still maintaining high stability (Figs. 12(e) and 12(f)).

As AM displays continue to advance with high resolution, the pixels shrink in size, necessitating the scaling down of MO TFTs. Therefore, studying the scaling behavior of ITZO TFTs is of great importance. This analysis would provide valuable insights into the performance and limitations of these devices as they are miniaturized. Factors like *L*, contact resistance, and gate insulator thickness can have a significant impact on the device characteristics at smaller dimensions. Understanding the scaling behavior is crucial for optimizing device performance and addressing potential challenges asso-

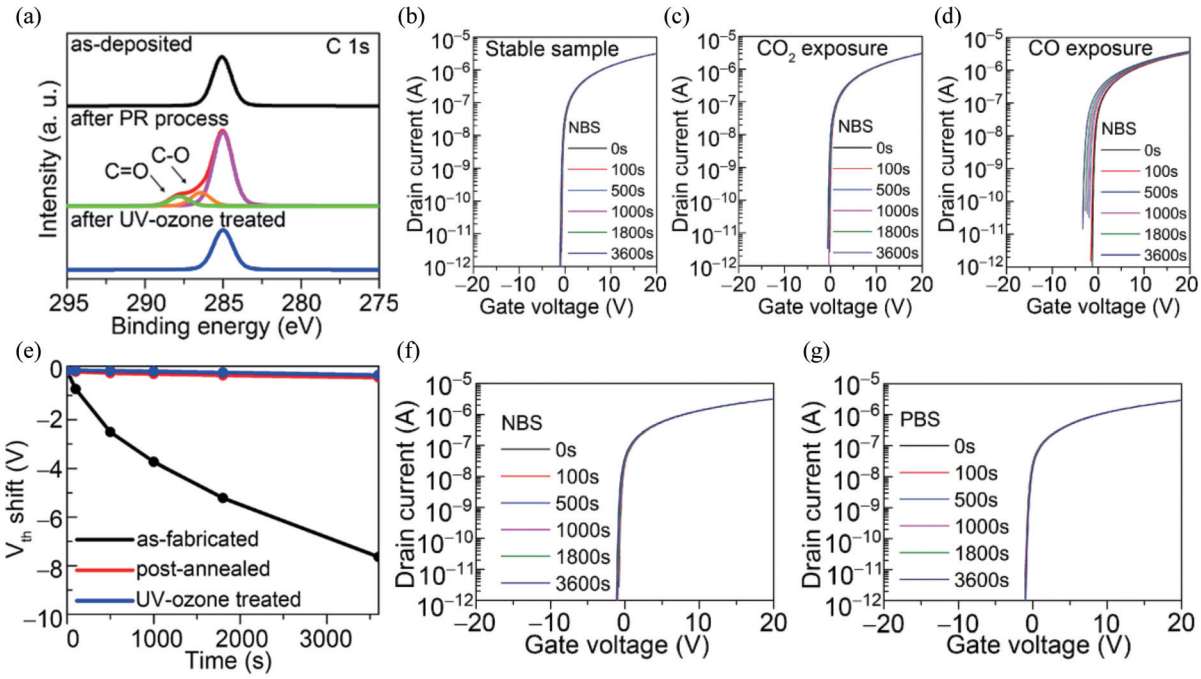


Fig. 11. (Color online) (a) Carbon 1*s* HAX-PES spectra of as-deposited and post-treated ITZO films. NBS stability of ITZO TFTs (b) without CO exposure, (c) with CO_2 exposure, and (d) with CO exposure. (e) Threshold voltage shift of TFTs with different treatment under NBS. (f) NBS stability and (g) PBS stability of UV ozone treated ITZO TFT[83]. (a)–(g) , © 2021 IEEE. Reprinted, with permission, from Ref. [83].

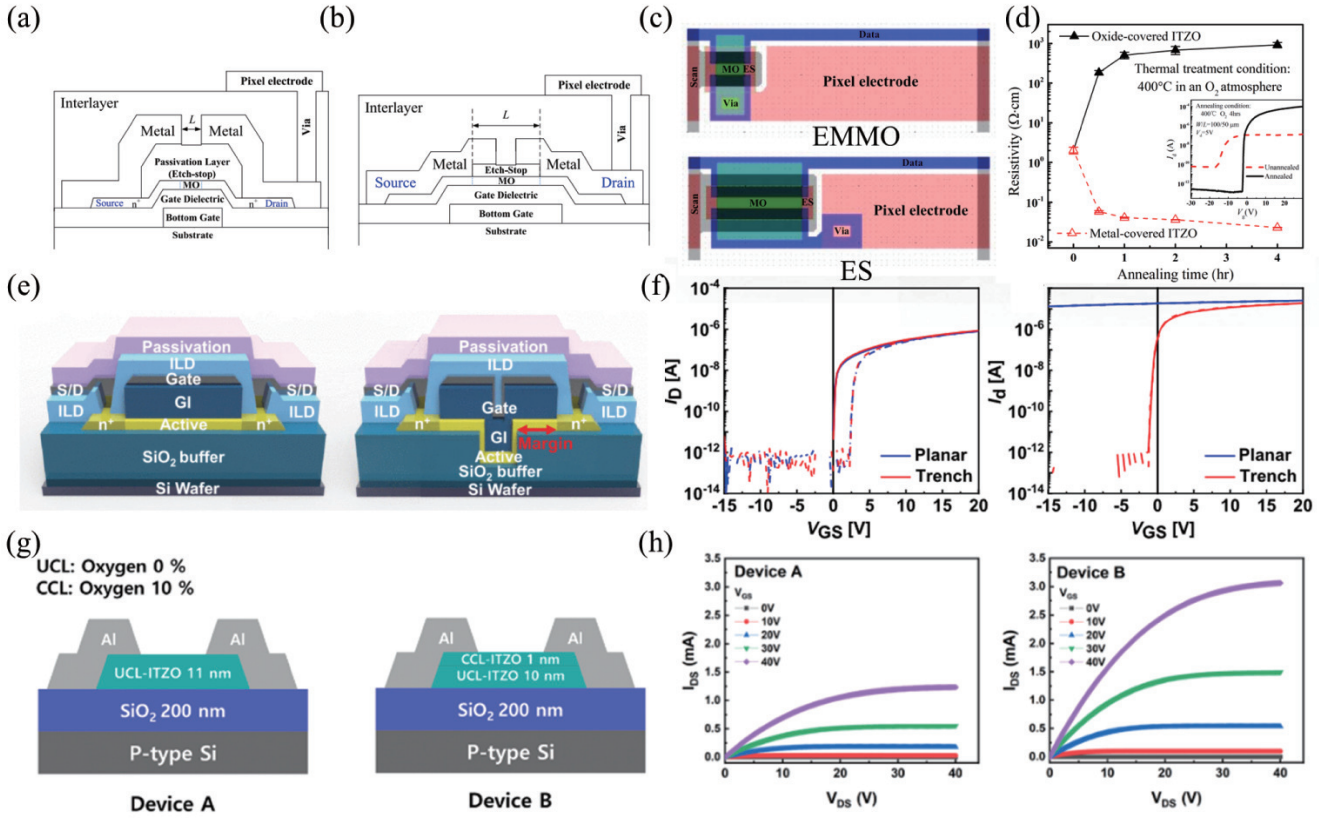


Fig. 12. (Color online) The cross-sectional schematics of (a) an EMMO and (b) an ES TFT and the corresponding layouts of a 500-ppi AMLCD subpixel based on (c) an EMMO and an ES TFT with a *W*/*L* of 2.5 and a design-rule of 2 μm. (d) The dependence of the resistivity values of metal- and oxide-covered ITZO on thermal treatment time. Shown in the inset are the transfer characteristics of EMMO ITZO TFTs with and without going through a thermal annealing process[85]. (a)–(d), © 2017 IEEE. Reprinted, with permission, from Ref. [85]. (e) Schematic diagrams of planar SA TFT (left) and trench SA TFT (right). (f) Transfer curves of planar and trench TFTs before annealing (left-hand panel) and after annealing at 270 °C (right-hand panel)[86]. (e)–(f), © 2021 IEEE. Reprinted, with permission, from Ref. [86]. (g) ITZO TFTs with different channel structures: device A contains an oxygen-uncompensated channel layer (UCL) and device B contains a bilayer channel, which is an oxygen-compensated channel layer (CCL) and an oxygen-uncompensated channel layer (UCL). (h) Output characteristics of device A and device B[87]. (g)–(h) , reprinted with permission from Ref. [87]. Copyright 2022, American Chemical Society.

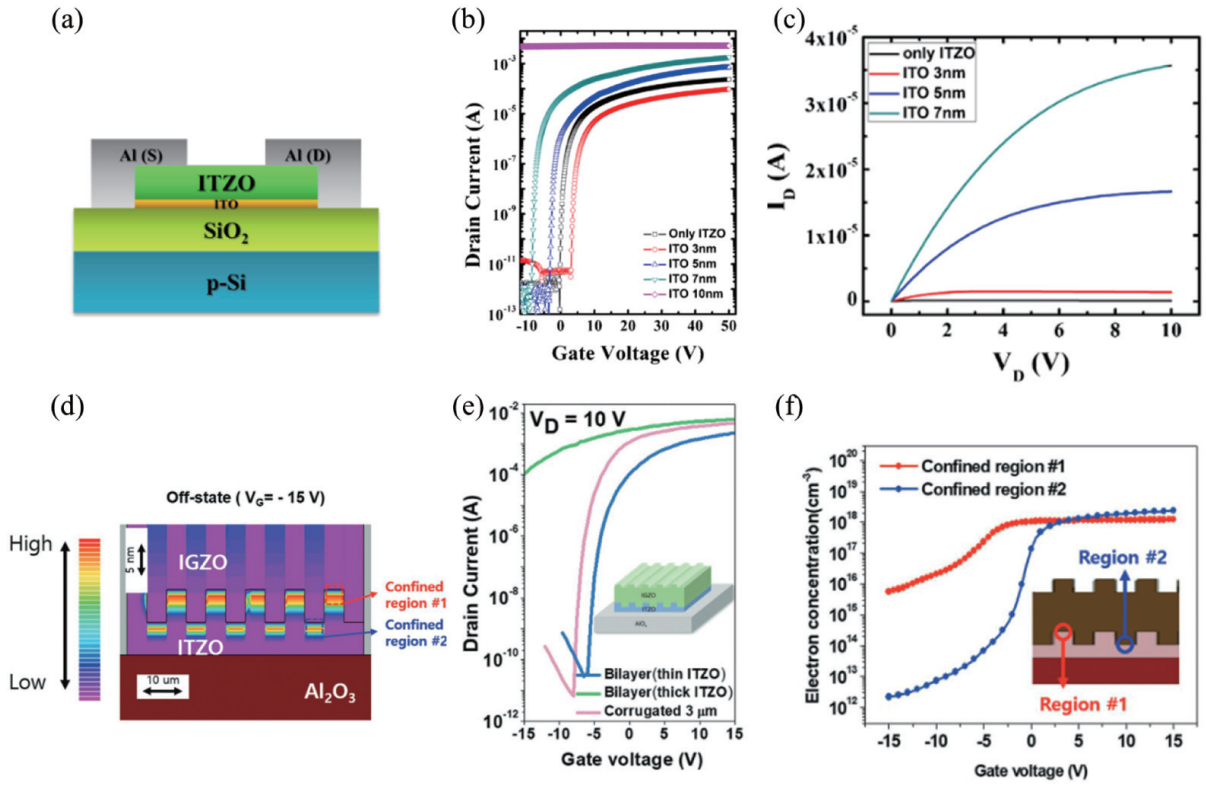


Fig. 13. (Color online) (a) Device structure of the bilayer ITO/ITZO TFT device. (b) Transfer characteristics of TFT devices with different ITO thicknesses. (c) Corresponding output characteristics of ITO/ITZO TFT devices[89]. (a)–(c), Reprinted from Ref. [89], Copyright (2016), with permission from Elsevier. (d) Contour of current density for off state. (e) Transfer characteristics of corrugated heterostructure ITZO (5.4 nm)/IGZO (20 nm) heterostructure, ITZO (10 nm)–IGZO (20 nm) heterostructure. (f) Electron concentration as a function of the gate voltage sweep (−15 to 15 V) in the indicated thick- (region #1) and thin-ITZO/IGZO heterointerface (region #2)[90]. (d)–(f) Ref. [90], John Wiley & Sons. [© 2018 Wiley-VCH GmbH].

ciated with miniaturization. However, there are currently limited reports available on the scaling behaviors of ITZO TFTs, which highlights the need for further exploration in this direction.

Mobility of ITZO TFT can be also improved by adjusting the device structure[87, 88]. Lee *et al*.[87] achieved significant improvements in mobility and stability by covering a 1 nm oxygen-rich ITZO film on top of the ITZO channel in a similar way to the passivation layer (Figs. 12(g) and 12(h)). The XPS characterization results showed that the oxygen vacancy content of the oxygen-rich ITZO layer was significantly lower than that of the low-oxygen layer, and the proportion of O–M–O bonds increased significantly. Thus, the oxygen-rich layer was less sensitive to air and water vapor and could act as a passivation layer. Additionally, oxygen from the oxygen-rich layer entered the low-oxygen layer to repair defects, further improving the film's quality. The performance improvement from this structure was ultimately reflected in a significant increase in mobility and stability.

By incorporating other materials, the performance of ITZO TFT can be enhanced[89–91]. In 2017, Nguyen *et al*.[89] introduced a very thin layer of ITO into the channel of ITZO TFT, resulting in a significant improvement in the device's mobility. However, if the ITO layer was too thin, then an island-like structure that was not fully formed could result in too many heterojunctions in the channel, which increases the likelihood of carrier scattering and ultimately leads to a decrease in mobility. When the inserted ITO layer reached a thickness of 5 nm, it provided more carriers, resulting in a significant increase in mobility (Figs. 13(a)–13(c)). Further increasing the thickness of the ITO layer would produce too many carriers, decreasing the gate-control capability and causing the device to directly conduct. Ultimately, after inserting a 5 nm ITO layer, the double-layer ITZO TFT reached a high mobility of 95 $cm^2/(V{\cdot}s)$ while still maintaining excellent stability.

In 2018, Lee *et al*.[90] reported on an IGZO/ITZO TFT with a corrugated heterojunction channel structure. Due to the heterojunction's diode-like characteristics, when under negative gate voltage, the carriers become trapped at the heterojunction interface, similar to a diode's reverse bias. Conversely, when under positive gate voltage, the heterojunction barrier is flattened, releasing a large number of electrons into the channel, greatly enhancing channel conductivity. However, in a planar structure heterojunction, the heterojunction is horizontally continuous, and the device's leakage current can easily increase due to the heterojunction continuously providing carriers to the source electrode when turned off. The corrugated structure of the heterojunction interface breaks the horizontal continuity of the heterojunction, so it does not continuously provide carriers to the source electrode, greatly reducing the off-state current of the device (Figs. 13(d)–13(f)).

4. Conclusion

Over the past decade, significant progress has been made in improving the performance of ITZO TFT through process optimization. This article reviews the various methods that have been used to prepare ITZO films and optimize the active layer, with a focus on sputtering. We also explore dop-

ing methods, post-treatment techniques, and high-*k* dielectrics. Ni has been identified as a suitable electrode material, and the role of passivation layers in optimizing back-channel surfaces is emphasized. Structural optimization has also been discussed from two perspectives: solo ITZO structure and introducing other materials. Despite progress in improving mobility, stability remains a challenge. There is a trade-off between mobility and stability, which must be addressed after achieving high mobility levels. Nonetheless, several methods that can improve mobility while maintaining high stability have been identified. The next step is to continue improving mobility while ensuring device stability within an acceptable range. Although many problems remain, ITZO TFT devices have surpassed traditional IGZO TFTs in terms of performance. The development in ITZO TFT-related technologies will undoubtedly contribute to future high-quality display panels.

Acknowledgments

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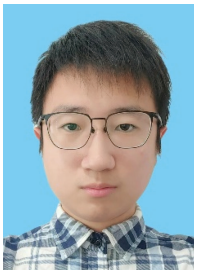

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