REVIEWS

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Low-temperature metal–oxide thin-film transistor technologies for implementing flexible electronic circuits and systems

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Abstract: Here we review two 300 °C metal–oxide (MO) thin-film transistor (TFT) technologies for the implementation of flexible electronic circuits and systems. Fluorination-enhanced TFTs for suppressing the variation and shift of turn-on voltage (V_{ON}), and dual-gate TFTs for acquiring sensor signals and modulating V_{ON} have been deployed to improve the robustness and performance of the systems in which they are deployed. Digital circuit building blocks based on fluorinated TFTs have been designed, fabricated, and characterized, which demonstrate the utility of the proposed low-temperature TFT technologies for implementing flexible electronic systems. The construction and characterization of an analog front-end system for the acquisition of bio-potential signals and an active-matrix sensor array for the acquisition of tactile images have been reported recently.

Key words: flexible electronics; metal–oxide semiconductor; thin-film transistor; dual gate; fluorination; analog front-end system; sensors

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1. Introduction

Besides their deployment in a flat-panel information display[1], low-temperature thin-film transistors (TFTs) have been used to construct flexible electronic systems such as radio-frequency identification tags[2], bio-sensor interface circuits[3] and microprocessors[4], etc. Offering relatively higher field-effect mobility (μ_{FE}) than that of the TFTs built on hydrogenated amorphous silicon and significantly lower off-state currents than that of those built on low-temperature polysilicon, TFTs built on metal–oxide (MO) semiconductors such as indium-gallium-zinc oxide (IGZO)[5] and indium-tin-zinc oxide (ITZO)[6] have been intensely investigated.

Donor-species, such as hydrogen (H)[7, 8] or those derived from oxygen deficiency[9, 10], when residing in excess in the channel region of a TFT lead to variation and negative shift of the turn-on voltage (V_{ON})[11] of a TFT. These often result in degradation in the performance, such as a reduced noise margin[12], attenuated gain[13] and reduced output voltage swing[14] of a circuit constructed of the TFTs. While thermal annealing is deployed to suppress the population of such species[10], the accessible conditions of a heat-treatment process are constrained by the material properties of the flexible substrate on which the TFTs are constructed. For a popular substrate such as polyimide (PI), these constraints include a maximum process temperature of below 400 °C that further reduces with increasing transparency of the PI; a mismatch between the thermal expansion coefficient of the PI and that of its glass carrier substrate leading to possible cracking of the PI after an extended heat-treatment[15]; and introduction into a TFT of H originating from the decomposition of hydrocarbon or hydroxyl species in the PI during its laser lift-off (LLO) from its carrier substrate[16], etc.

A series of studies addressing issues concerning the design and construction of circuits and systems based on MO TFTs are reviewed here. The topics include how the variation of TFT electrical parameters affects the performance of a circuit; how fluorination is deployed to suppress such variation and enhance the stability of a TFT[17]; and how dual-gate (DG) TFTs, with at least a part of its channel region sandwiched between two parallel gate electrodes, allow the modulation of the effective V_{ON} referred to as one gate by a bias applied on the other. Given the inevitable variation of the electrical parameters of TFTs, DG TFTs can be deployed as signal-acquisition devices in a sensor array and applied in a scheme for mitigating the detrimental effects of such variation. Finally, the construction and characterization of an integrated analog front-end circuit built using a single-gate (SG) IGZO TFT technology and an active-matrix tactile sensor array built using a DG ITZO TFT technology are reviewed.

2. Low-temperature MO TFT technologies

2.1. Fluorination-enhanced MO TFT

On the starting 0.5-mm-thick glass carrier substrate coated with a 10-μm-thick PI, the preparation of MO TFTs (Fig. 1(a)) starts with the formation of a stack of buffer layers consisting of 200-nm-thick silicon nitride (SiN_y) under 300-nm-thick silicon oxide (SiO_x), where both are deposited at 300 °C in a plasma-enhanced chemical vapor deposition (PECVD) system. A 100-nm-thick molybdenum (Mo) layer is sputtered and patterned in an aqueous mixture of phosphoric, nitric, and acetic acids to form the bottom gate (BG) electrodes. A 75-nm-thick PECVD SiO_x on a 50-nm-thick PECVD

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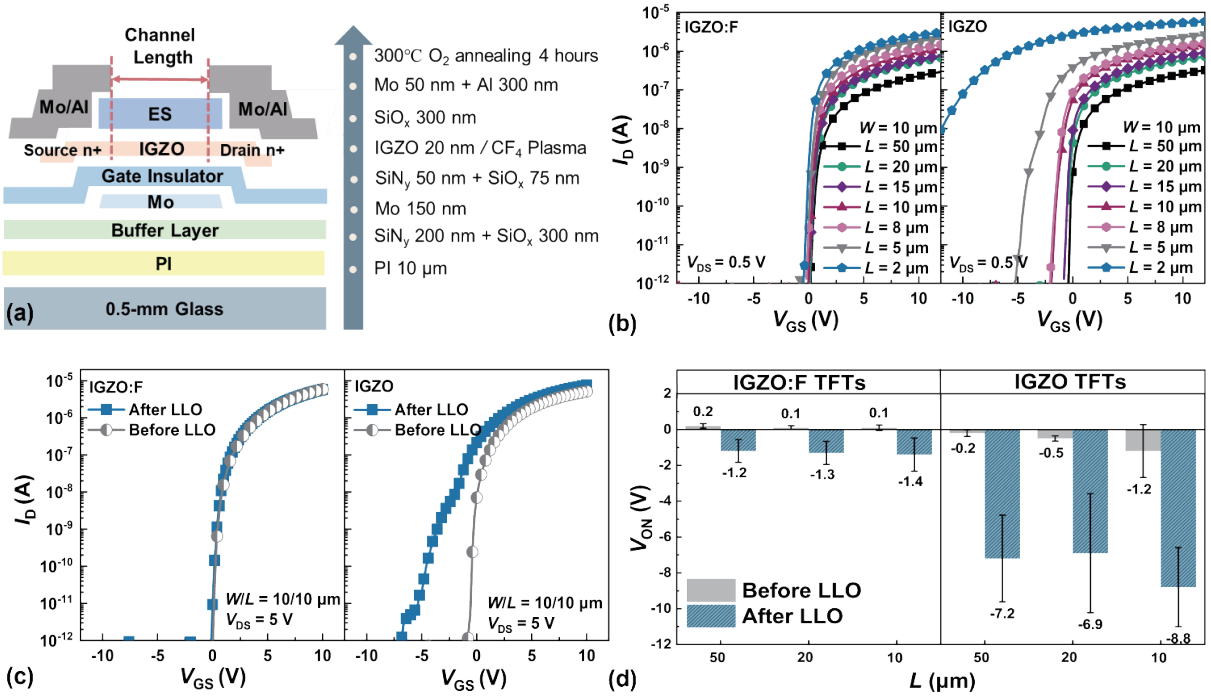

Fig. 1. (Color online) (a) A schematic cross-section of an IGZO or IGZO:F TFT. (b) Comparison of the measured transfer characteristics of IGZO:F and IGZO TFTs with W = 10 μm and L decreasing from 50 to 2 μm. (c) Comparison of the measured transfer characteristics of IGZO:F and IGZO TFTs before and after LLO. (d) Measured statistical distributions of the V_{ON} of IGZO:F and IGZO TFTs before and after LLO[17]. Copyright 2021 IEEE.

SiN_y stacked dielectric is next formed at 300 °C. A 20-nm-thick amorphous IGZO active layer is then sputtered at room temperature using an $In_2O_3 : Ga_2O_3 : ZnO = 1 : 1 : 1$ target in an atmosphere of 90% argon (Ar) and 10% oxygen (O_2). Some of the samples are next treated in a tetrafluoromethane (CF_4) plasma for 10 min in the PECVD chamber at 300 °C to form IGZO:F[9], i.e. fluorinated IGZO. Active islands are patterned by etching in a 1/2000 hydrofluoric acid solution before a 300-nm-thick PECVD SiO_x etch-stop (ES) layer is deposited. The contact holes to the BG and source/drain (S/D) regions are opened in an inductively coupled plasma etcher running a sulfur hexafluoride chemistry. Electrodes are constructed of sputtered and patterned stacks of 300-nm-thick aluminum (Al) on 50-nm-thick Mo. During a subsequent annealing process at 300 °C in O_2 for 4 h, portions of the active island covered by the gas-impermeable Al/Mo electrodes become the conductive S/D regions, while the portion covered by the exposed gas-permeable SiO_x becomes the channel region of a TFT[18]. LLO to separate the TFT-carrying PI from the carrier substrate is accomplished using a 308 nm XeCl excimer laser irradiated through the substrate.

The transfer characteristics, i.e. the dependence of the drain current (I_D) on the gate-to-source voltage (V_{GS}), of two sets of IGZO and IGZO:F TFTs are shown in Fig. 1(b). Each set consists of 7 TFTs, with a channel width (W) of 10 μm and channel length (L) reducing from 50 to 2 μm. Defined as the V_{GS} required to induce an I_D of 1 pA at a drain-to-source voltage (V_{DS}) of 0.5 V, the V_{ON} of the IGZO:F TFTs with different L cluster around 0 V, while that of an IGZO TFT shifts negatively with decreasing L–thus exhibiting significant apparent short-channel effects (SCE). The reduced vulnerability of IGZO:F TFTs to apparent SCE is attributed to the suppressed population of donor-species in a fluorinated channel.

Comparisons are made of the performance of TFTs before and after LLO. It can be seen in Fig. 1(c) that the characteristics of the IGZO:F TFT remain unchanged, while those of the IGZO TFT exhibit a negative shift in V_{ON} and the appearance of a weak hump after LLO. The statistical variations of the V_{ON} of IGZO:F and IGZO TFTs with L = 50, 20 and 10 μm before and after the LLO are shown in Fig. 1(d). Ten TFTs are measured for each L. The negative shift in V_{ON} and the corresponding standard deviation of the V_{ON} of the IGZO:F TFTs are significantly smaller than those of the IGZO TFTs. The degradation of the performance of the IGZO TFTs after LLO is attributed to the generation of donor-species, such as water molecules evolving from the PI or H generated during the LLO, and their subsequent diffusion into the channel region. The improved performance of the IGZO:F TFT is consistent with their reported resilience against H-induced degradation[7].

2.2. DG MO TFT

The evolution of the cross-section of a DG ITZO TFT through its process of construction is shown in Fig. 2. On a similar substrate as the 0.5-mm-thick glass carrier substrate coated with a 10-μm-thick PI, a stack of buffer layers consisting of 200-nm-thick SiN_y under 300-nm-thick SiO_x was deposited at 300 °C in a PECVD system. A 100-nm-thick Mo layer is sputtered and patterned as the BG electrode before the PECVD of a bottom gate-insulator (GI) stack consisting of 75-nm-thick SiO_x on 50-nm-thick SiN_y. Following a 2-h furnace anneal in O_2 at 300 °C, a 20-nm-thick ITZO active layer is sputtered in an atmosphere of 60% Ar and 40% O_2. After patterning the ITZO layer to form an active island, a 100-nm-thick SiO_x is deposited as the top GI. Following another furnace anneal at 300 °C for 6 h in O_2, a 150-nm-thick Mo is sputter-deposited and patterned to form the top-gate electrode (TG) before the deposition of a 200-nm-thick SiO_x. This is followed by a furnace anneal for 8 h in O_2 at 250 °C. Formation of the S/D regions self-aligned to the edges of the TG is accom-

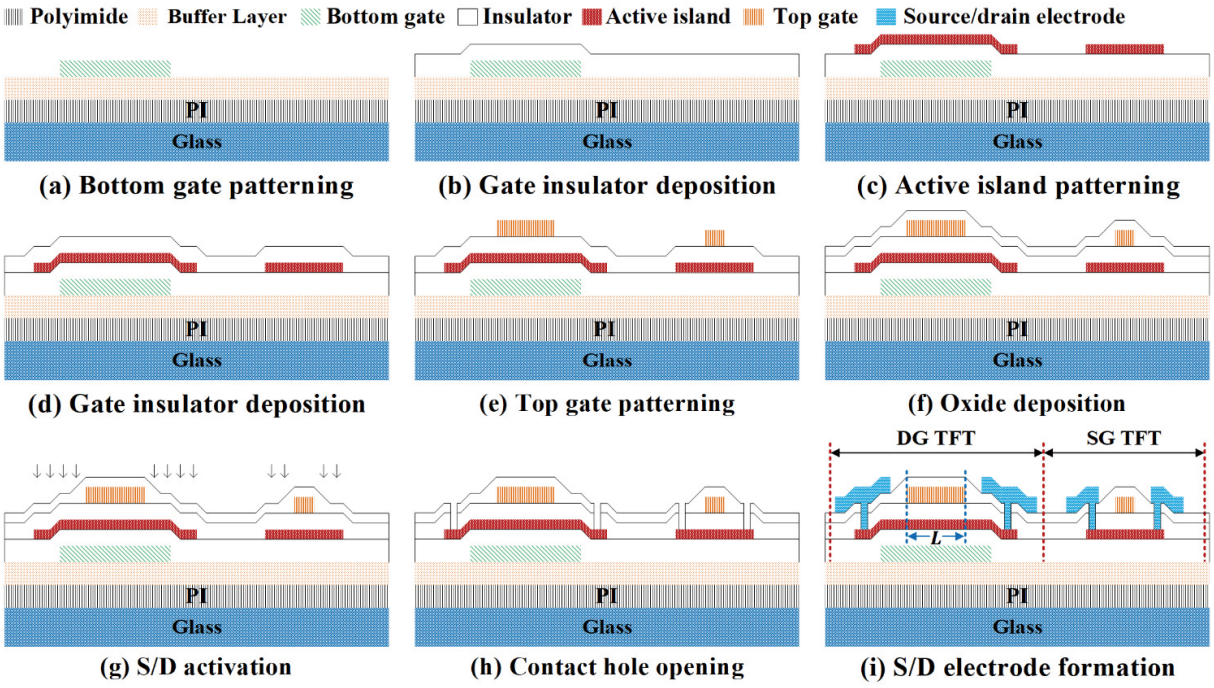

Fig. 2. (Color online) The fabrication process of SG and DG ITZO TFTs.

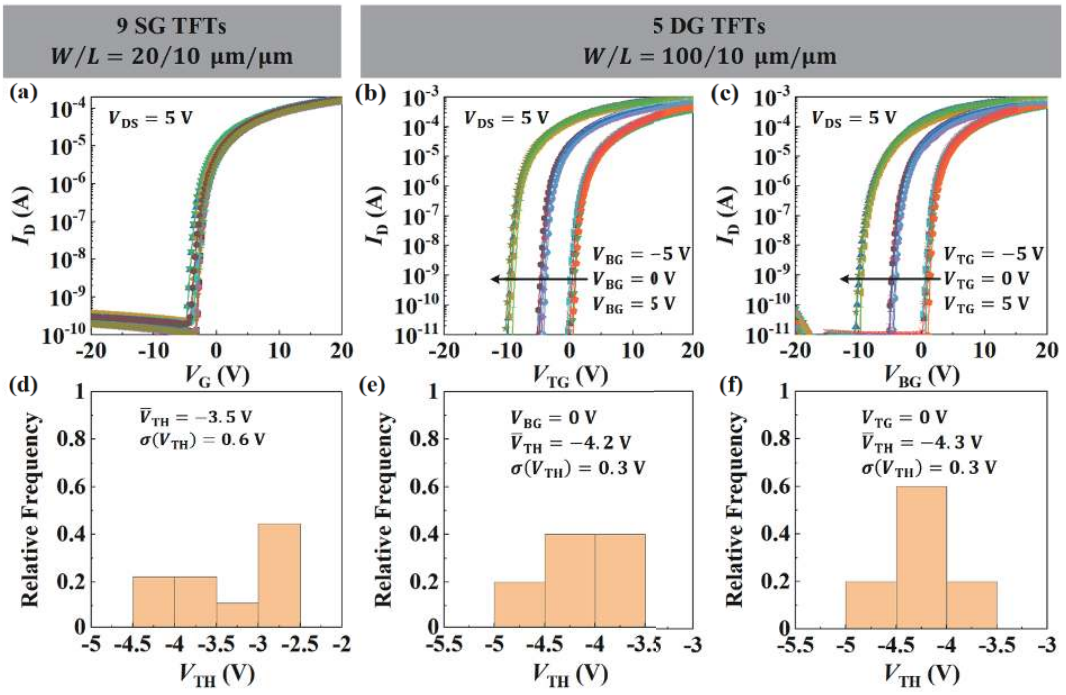

Fig. 3. (Color online) Transfer characteristics of (a) SG TFTs, (b) DG TFTs with BG as the MG and TG as the OG, and (c) DG TFTs with TG as the MG and BG as the OG; extracted V_{TH} of (d) SG TFTs, (e) DG TFTs with BG as the MG and TG as the OG, and (f) DG TFTs with TG as the MG and BG as the OG.

plished by exposure to an O_2 plasma[19], while the portion of the active island covered by the TG retains its semiconducting property and becomes the channel region. Contact holes to access the TG, S/D, and BG layers are subsequently opened before a stack of 200-nm-thick Al on 150-nm-thick Mo is deposited and patterned to form the electrodes.

The transfer characteristics of 9 SG ITZO TFTs with W/L of 20/10 μm/μm, randomly selected over a 4-inch substrate, are shown in Fig. 3(a). The "modulating gate (MG)" of a DG TFT is the BG or the TG connected to a fixed bias, the remaining gate connected to a variable bias is called the "operating gate (OG)". Shown in Figs. 3(b) and 3(c) are the I_D *vs*. OG voltage (i.e. V_{BG} or V_{TG}) curves of six DG TFTs with W/L of 100/10 μm/μm at MG voltage (i.e. V_{TG} or V_{BG}) of −5, 0, and 5 V. Shown in Fig. 3(d) is the statistical distribution of the extracted threshold voltage (V_{TH}) of the SG ITZO TFTs, where V_{TH} is defined as the gate voltage required to generate an I_D of 1 nA at V_{DS} = 5 V. The mean ($\bar{V}_{TH}$) and standard deviation ($\sigma(V_{TH})$) of V_{TH} are respectively −3.5 and 0.6 V. For the DG ITZO TFTs with TG as OG and BG as MG, the corresponding $\bar{V}_{TH}$ and $\sigma(V_{TH})$ values shown in Fig. 3(e) are respectively −4.2 and 0.3 V at V_{BG} = 0 V. Exhibited in Fig. 3(f) is the statistical dis-

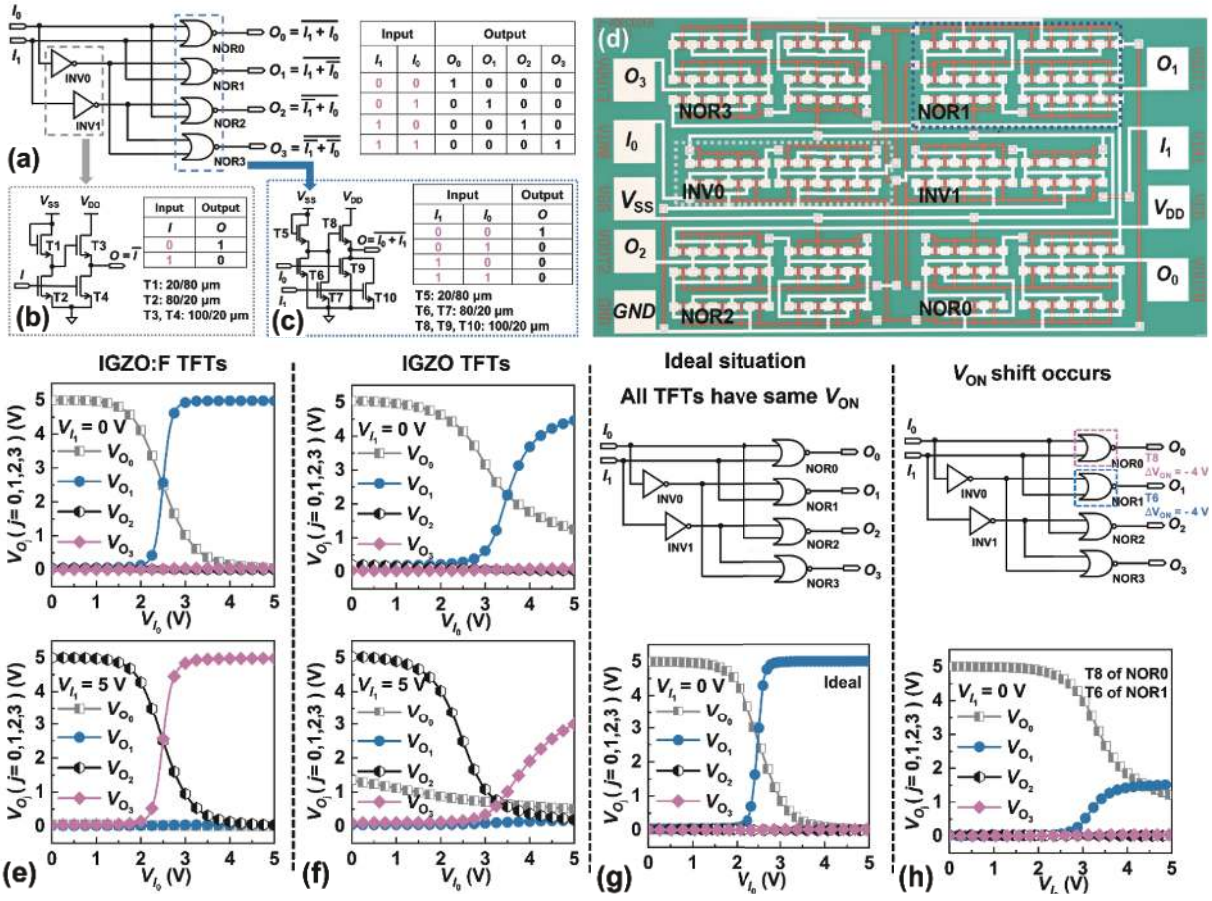

Fig. 4. (Color online) Fluorination-enhanced 2-4 decoder[17]. (a) Gate-level schematic and truth table of a 2-4 decoder. (b) TFT-level circuit diagram and truth table of an INV. (c) TFT-level circuit diagram and truth table of a NOR. (d) A photograph of a fabricated 2-4 decoder on PI. (e) Measured VTCs of 2-4 decoders fabricated using IGZO:F TFTs. (f) Measured VTCs of 2-4 decoders fabricated using IGZO TFTs. (g) Simulated VTCs of ideal implementation with the same V_{ON} ~ 0 V for all TFTs. (h) Implementation with V_{ON} shifts of −4 V for both TFT T8 of the NOR0 gate and the pull-down TFT T6 of the NOR1 gate[17]. Copyright 2021 IEEE.

tribution of V_{TH} of the DG ITZO TFTs with BG as the OG and TG as the MG. The $\bar{V}_{TH}$ and $\sigma(V_{TH})$ are respectively −4.3 and 0.3 V at V_{TG} = 0 V. Clearly, both SG and DG ITZO TFTs exhibit non-uniformity in their electrical parameters.

3. Circuit building blocks

Converting an n-bit digital input to one of a maximum of 2^n unique digital outputs, a binary decoder is used to demonstrate the utility of fluorination in improving circuit performance[17]. Shown in Fig. 4(a) is the gate-level schematic, consisting of 2 inverters (INV) and 4 NOR gates, and the truth table of a 2-4 decoder with 2 inputs (I_0 and I_1) and 4 outputs (O_0, O_1, O_2 and O_3). Designed in the "pseudo-CMOS" style[20], the TFT-level schematics and the truth tables of INV and NOR are shown respectively in Figs. 4(b) and 4(c). V_{SS} is an additional voltage source required by the pseudo-CMOS design style to ensure full swing of the output signal from the ground *GND* to the supply voltage V_{DD}. A photograph of a fabricated decoder on the PI is shown in Fig. 4(d).

With V_{DD}, V_{SS} and *GND* set respectively to 5, 12 and 0 V, the voltage-transfer characteristics (VTCs) of decoders implemented using IGZO:F and IGZO TFTs are shown respectively in Figs. 4(e) and 4(f), where the voltage levels corresponding to the respective logic inputs $I_i : i = 0, 1$ and logic outputs $O_j : j = 0, 1, 2, 3$ are denoted by V_{I_i} and V_{O_j}. Logic states "0" and "1" correspond respectively to the voltage levels of *GND* and V_{DD}. It can be seen from Fig. 4(e) that the decoder built using IGZO:F TFTs operates in a manner close to that of an ideal decoder, i.e, only one output exhibits logic "1", while the rest exhibits logic "0" for any given input configuration. However, the behavior of the decoder shown in Fig. 4(f) build using IGZO TFTs deviates from that of an ideal decoder: a) When V_{I_1} = 0 V and V_{I_0} = 5 V, V_{O_1} fails to reach 5 V and V_{O_0} fails to reach 0 V. b) When V_{I_1} = 5 V, V_{O_0} is well above 0 V. c) V_{O_3} fail to reach 5 V, when $V_{I_0} = V_{I_1}$ = 5 V.

The simulated VTCs of a 2–4 decoder when V_{I_1} = 0 V are shown in Figs. 4(g) and 4(h). The measured VTCs of a decoder built using IGZO TFTs are closer to the simulated VTCs when a negative shift of V_{ON} is imposed. By suppressing the negative shift of V_{ON} of TFTs, fluorination improves the performance of the decoder. Consequently, the measured VTCs of a decoder built using IGZO:F TFTs is much closer to the simulated VTCs shown in the ideal case when variation is suppressed and all the TFTs in the decoder have the same V_{ON}.

4. Demonstration flexible electronic systems

4.1. Analog front-end system

Based on the fluorinated SG IGZO TFT technology, an analog front-end (AFE) system for the acquisition of bio-potential signals is designed, fabricated, and characterized[21]. The architecture of the AFE system is shown in Fig. 5(a), consisting of three sub-systems of (Ⅰ) bias-filters to remove the half

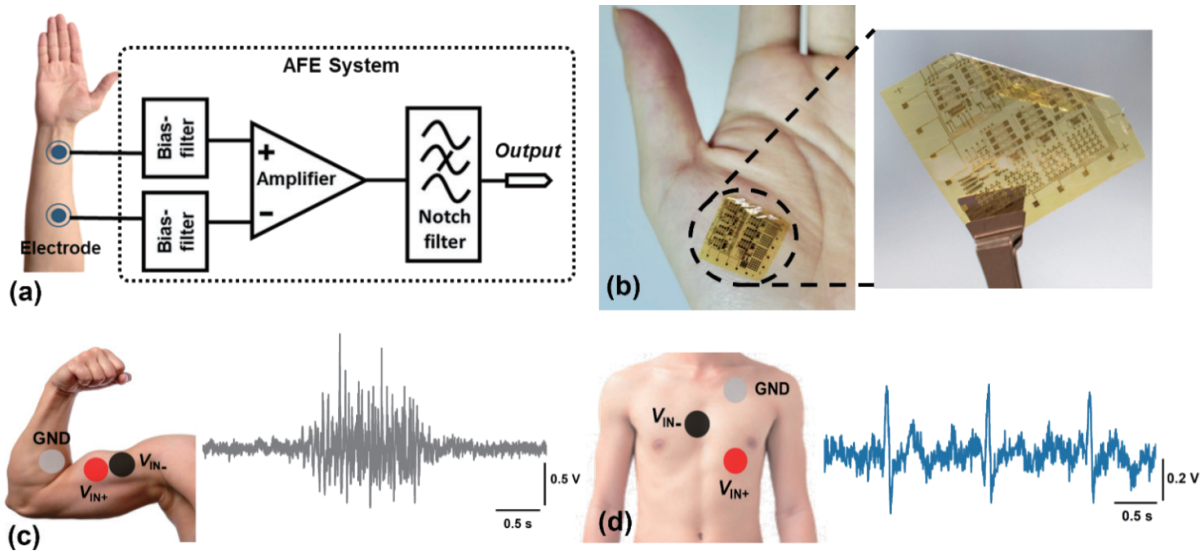

Fig. 5. (Color online) An AFE system for the acquisition of bio-potential signals. (a) System architecture. (b) PI carrying AFE systems placed on the thenar muscle of a hand. *In-vitro* measurements of (c) EMG and (d) ECG[21]. Copyright 2023 Wiley.

cell-potential generated at the contacts between the sensing electrodes and the skin, and to bias the bio-potential to match the operating point of (Ⅱ) a differential amplifier deployed to magnify the bio-potential signal and to suppress the common-mode noise, and (Ⅲ) a notch filter to suppress the power line noise. A fabricated AFE system on the PI placed on the thenar muscle of a hand is shown in Fig. 5(b). IGZO TFTs serve not only as active devices but are also deployed to realize physically small resistors with high resistance. Additionally, the combination of a thermally induced IGZO conductor and the thin gate insulator allows the realization of a physically small capacitor with a large capacitance per unit area. It is the combination of these small components in the bias and notch filters that makes it possible to realize an AFE with a small footprint of ~11 mm^2. With two of the three electrodes connected to the two inputs V_{IN+} and V_{IN-}, and the remaining one to the ground node of the AFE, *in-vitro* measurements of electromyogram (EMG) and electrocardiogram (ECG) have been performed. The respective electrode connections and the traces of the EMG and ECG are shown in Figs. 5(c) and 5(d).

4.2. Tactile sensor array

Using thin-film piezoelectric polyvinylidene fluoride (PVDF) as a sensing medium, an active-matrix tactile sensor array[22] has been implemented using the DG ITZO TFT technology. Shown in Fig. 6(a) is the circuit schematic of an in-pixel amplifier consisting of a DG driving TFT M1, a diode-connected SG load TFT M2, and a switching TFT M3. One gate of M1 is employed as an input gate terminal to receive the input signal V_I and the other gate is employed as an MG terminal biased at a voltage V_B. The corresponding amplified voltage is contained in the output signal V_O. The timing diagram associated with the active-matrix addressing of the tactile sensor array is shown in Fig. 6(b). With V_{DD} = 10 V, V_{LL} = 4 V and a constant V_B = 8 V (Fig. 6(c)), the dependence of the voltage gain A_V on V_I for 40 in-pixels amplifiers are characterized and shown in Fig. 6(d). Exhibited in Fig. 6(e) are the corresponding A_V at V_I = 0 V, showing a relatively wide range of 1.5 V/V between −0.5 and −2 V/V.

The circuit schematic and timing diagrams of an in-pixel amplifier are shown in Figs. 6(f) and 6(g), allowing the application of a compensation scheme. Shown respectively in Figs. 6(h) and 6(i) are photographs of a 625 × 625 μm tactile pixel and a 16 × 16 tactile sensor array with compensation. With a global compensation signal CMP, the compensation and signal-acquisition scheme operate in two stages: Stage 1 is the compensation phase for setting $V_B = V_O$ and Stage 2 is the acquisition phase for acquiring the signal V_I. During Stage 1, the threshold voltage of M1 in every pixel is modulated by switching on M4 and M5 to allow M1 to be consistently biased in the saturation mode. During Stage 2, the compensated V_B generated in Stage 1 is stored on the capacitor C_S by switching off M4 and M5. The compensated V_B shown in Fig. 6(c) ranges between 6.6 and 7.5 V, reflecting the non-uniformity of TFT parameters. The resulting $A_V \approx -2$ V/V varies over a much tighter range of 0.1 V/V, as shown in Figs. 6(j) and 6(k).

A constant V_B of 8 V for an uncompensated array and the self-biased V_B extracted from a compensated array are shown respectively in Figs. 7(a) and 7(b). V_B in Fig. 7(b) gradually increases from the upper right to the lower left corner of the array, reflecting a systematic trend of the variation of the parameters of the TFTs across the corresponding diagonal of the array. Obtained with the arrays loaded with a letter stamp "O", respective tactile images w/o and w/ compensation are displayed in Figs. 7(c) and 7(d). Sharper edges corresponding to better uniformity are observed for the compensated image exhibited in Fig. 7(d). The tactile images acquired using a smaller 8 × 8 tactile sensor array[23] are shown in Fig. 7(e), with the mass of the 3D-printed letter and number stamps in the range of dozens of milligrams.

5. Future perspectives

While oxygen deficiency is reported to be responsible for the generation of carrier donors in the S/D regions of a SG TFT processed at 400 °C, a recent kinetic model[8] suggests the generation of such donors should be negligible at 300 °C. Consequently, the mechanism responsible for the formation

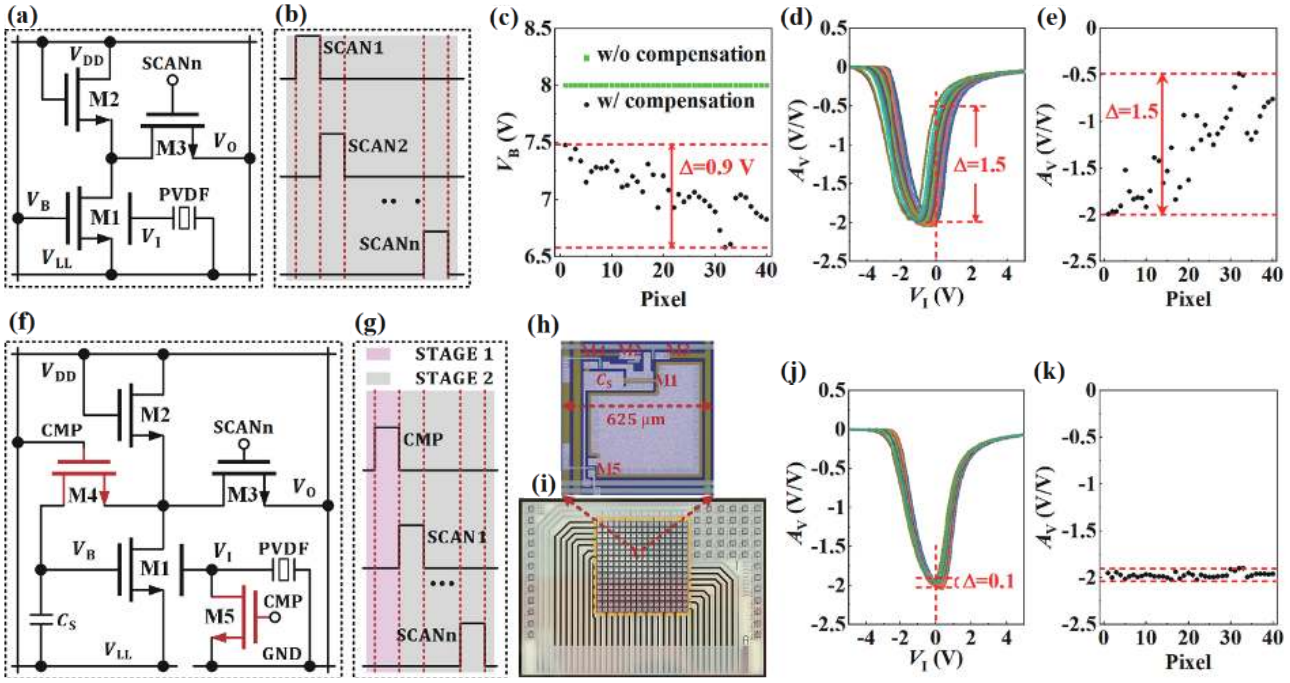

Fig. 6. (Color online) DG ITZO TFT-based in-pixel amplifiers w/ and w/o provision for compensation of TFT parameter variation: (a) circuit schematic and (b) timing diagram; (c) distribution of MG voltage V_B for 40 pixel circuits w/ and w/o compensation; (d) dependance of A_V on V_I and (e) distribution of A_V at V_I = 0 V for 40 amplifiers w/o compensation. In-pixel amplifiers w/ provision for compensation of TFT parameter variation: (f) circuit schematic and (g) timing diagram; (h) microscope image of a tactile pixel and (i) photograph of a 16 ×16 active-matrix tactile sensor array; (j) dependance of A_V on V_I and (k) distribution of A_V at V_I = 0 V for 40 amplifiers w/ compensation[22]. Copyright 2023 IEEE.

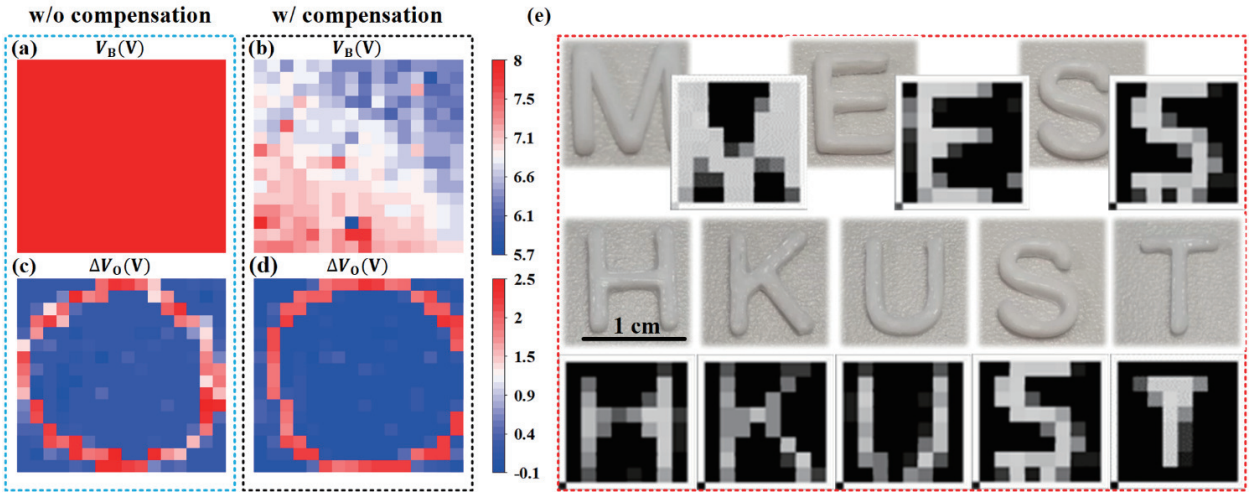

Fig. 7. (Color online) MG voltage V_B distribution over a 16 ×16 tactile sensor array (a) w/o and (b) w/ compensation[22]; tactile images from arrays (c) w/o and (d) w/ compensation when loaded with a letter stamp "O"; (e) tactile images acquired from an 8 × 8 tactile sensor array[23]. Copyright 2022 and 2023 IEEE.

of the conductive S/D regions at 300 °C needs to be clarified. Furthermore, the principle behind the O_2-plasma induced activation of the S/D regions in DG TFTs is currently unknown and needs to be investigated.

A schematic system diagram of a more capable bio-potential acquisition system is shown in Fig. 8. In addition to the bias filter, differential amplifier and notch filter are reviewed in the present work, an analog-to-digital converter (ADC) for converting the acquired bio-potential from an analog signal to a digital signal, a wireless module for transmission of the converted signal to a terminal for further data processing and display, and a power management module could also be integrated.

A bionic "smart" system consisting of a tactile sensor array and an artificial neural network is shown in Fig. 9. The flexible tactile sensor array based on the integration of PVDF film and DG MO TFTs could be applied to health monitoring, such as pulse-wave measurement. Near-sensor and in-sensor neuromorphic computing were achieved by the artificial neural network which could enable flexible electronic skin with bionic tactile perception.

6. Conclusion

300 °C MO TFT technologies based both on IGZO and ITZO for the implementation of flexible electronic systems have been reviewed. Fluorination has been reported to sup-

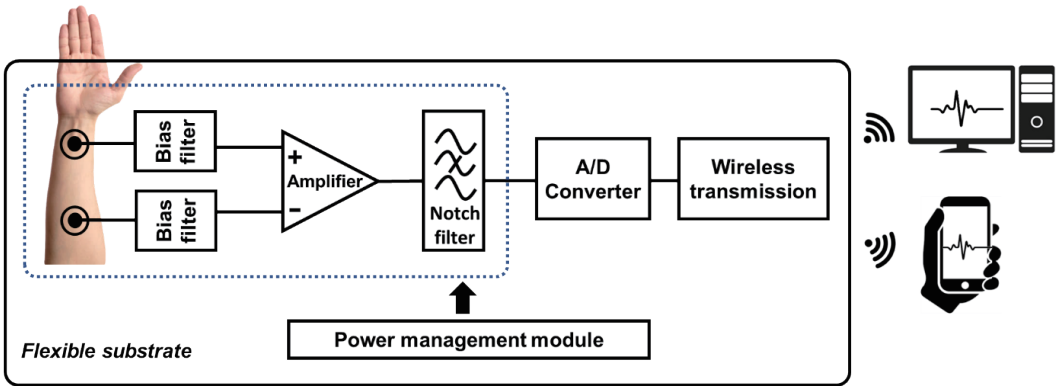

Fig. 8. (Color online) A schematic system diagram of a more capable bio-potential acquisition system on a flexible substrate.

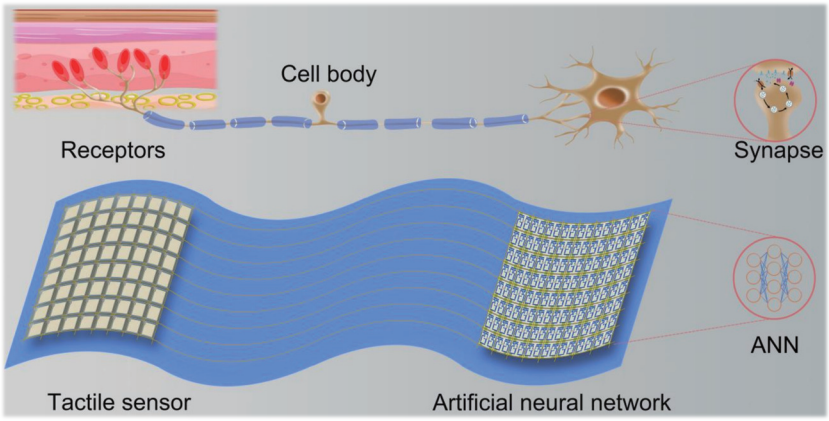

Fig. 9. (Color online) Flexible tactile sensor array integrated with an artificial neural network as a bionic "smart" system.

press the variation and shift of V_{ON}, and DG TFTs have been deployed to modulate the V_{ON} and to acquire sensor signals. Both are found to improve the robustness and performance of the systems in which they are deployed. Demonstrating the utility of the TFT technologies to the construction of flexible electronic systems, an analog front-end system for the acquisition of bio-potential signals and an active-matrix sensor array for the acquisition of tactile images have been reported.

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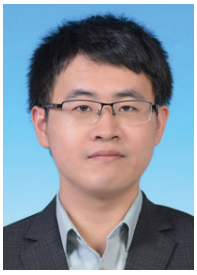

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