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High threshold voltage enhancement-mode GaN p-FET with Si-rich LPCVD SiN_x gate insulator for high hole mobility

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Abstract: In this work, the GaN p-MISFET with LPCVD-SiN_x is studied as a gate dielectric to improve device performance. By changing the Si/N stoichiometry of SiN_x, it is found that the channel hole mobility can be effectively enhanced with Si-rich SiN_x gate dielectric, which leads to a respectably improved drive current of GaN p-FET. The record high channel mobility of 19.4 $cm^2/(V{\cdot}s)$ was achieved in the device featuring an Enhancement-mode channel. Benefiting from the significantly improved channel mobility, the fabricated E-mode GaN p-MISFET is capable of delivering a decent-high current of 1.6 mA/mm, while simultaneously featuring a negative threshold-voltage (V_{TH}) of −2.3 V (defining at a stringent criteria of 10 μA/mm). The device also exhibits a well pinch-off at 0 V with low leakage current of 1 nA/mm. This suggests that a decent E-mode operation of the fabricated p-FET is obtained. In addition, the V_{TH} shows excellent stability, while the threshold-voltage hysteresis ΔV_{TH} is as small as 0.1 V for a gate voltage swing up to −10 V, which is among the best results reported in the literature. The results indicate that optimizing the Si/N stoichiometry of LPCVD-SiN_x is a promising approach to improve the device performance of GaN p-MISFET.

Key words: p-channel; GaN p-FET; LPCVD; channel mobility; hole mobility; enhancement-mode

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1. Introduction

GaN high-electron-mobility transistors (HEMTs) have developed rapidly in the last decade. Thanks to the high-density and high-mobility 2-D electron gas, the commercialized GaN HEMTs are competitive and emerging transistors for next generation high-performance power electronics, RF, and harsh environment electronics[1, 2]. However, they are limited by parasitic effects and unmatched robustness of Si-based peripheral circuits. Therefore, the potential of GaN HEMTs is not fully unleashed, and the monolithic integration of GaN-based analog integration circuit (IC) and power devices is highly demanded[3, 4].

GaN complementary logic (CL) based on n-channel HEMTs and p-channel field-effect-transistors (p-FETs) has recently been demonstrated[5–8]. Nevertheless, the performance of the reported GaN p-FETs is still far behind the counterpart of n-channel HEMTs. The wide-energy-band achieves the high critical electric field. However, it also leads to the heavy valence bands, which results in substantially low hole mobility in Ⅲ-nitride heterostructures to date[9]. The reported hole mobilities in the as-grown p-GaN/(UID-GaN)/AlGaN heterostructures are less than 16 $cm^2/(V{\cdot}s)$[8–16]. The channel mobilities are even lower in the recessed gate[16–18]: the highest channel mobility was reported to be a mere 11.8 $cm^2/(V{\cdot}s)$ in the UID-GaN channel[16]. This low hole mobility leads to a significantly increased on-resistance (R_{ON}) of GaN p-FETs. Moreover, the CL integration requires GaN p-FETs to deliver enhancement-mode (E-mode) operation, which enables the high performance GaN CMOS single-chip integration to eventually be achieved. In this manner, a deep gate trench is necessary to shift the threshold-voltage (V_{TH}) into negative, which in turn further reduces the on-state drain current (I_D) of GaN p-FETs[17]. This gate trench structure is further detrimental to the gated channel mobility, which is the current focus of GaN community to improve the current conduction capability of GaN p-FETs. The significantly low hole current of the p-FETs may cause unfavorable current-conduction capability mismatch with the mainstream n-channel HEMTs, which feature relatively high on-state electron current of hundreds mA/mm. This on-state current mismatch inevitably results in absonant large periphery layout of GaN p-FETs, which requires a large chip size. This hinders the realization of a high performance and compact GaN single-chip IC.

There have recently been many reports on enhancing the conduction current of GaN p-FETs. One approach is to construct the Ⅲ-nitride epi-structure featuring a multiple-channel, which enables higher overall hole density to increase the hole current density[9, 10]. A p-GaN/UID-GaN/AlN heterostructure has been utilized for GaN p-channel metal-oxide-semiconductor field-effect-transistors (MOSFETs)[11], which achieved 10 mA/mm on-state current with depletion-mode (D-mode) operation, while the device cannot be pinched-off at 0 V. The self-alignment process was proposed to minimize the device

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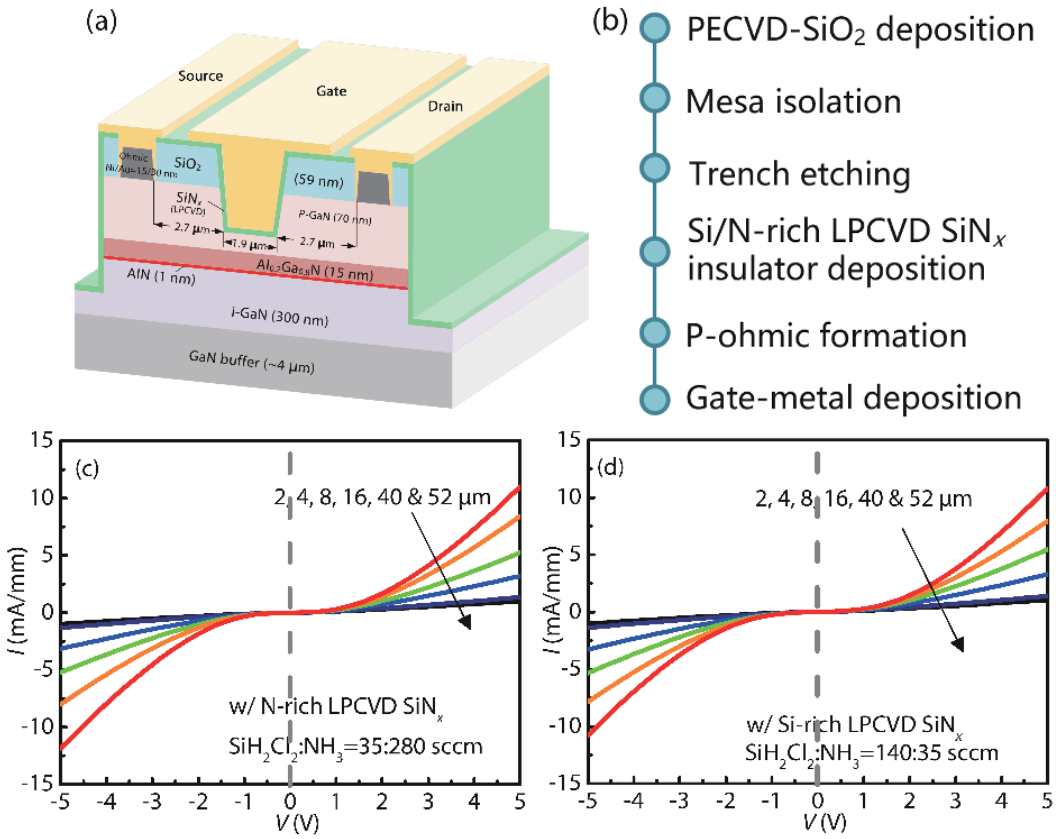

Fig. 1. (Color online) (a) Epitaxial structure and schematic of the proposed device. (b) The fabrication procedure. The *I*–*V* characteristic measured from TLM for the samples with (c) N-rich LPCVD SiN_x and (d) Si-rich LPCVD SiN_x.

dimensions on a p-GaN/unintentionally doped (UID) GaN/AlGaN platform to reduce the parasitic resistance of the access region. Although 25 mA/mm on-state current is obtained in the tungsten-Gated device with 2 μm gate length, the device features D-mode function with a positive V_{TH} of +3.5 V[12]. In addition, the Fin-FET structure was further developed by using the identical self-alignment process to increase the hole current. Nevertheless, the Fin-FET still delivered the D-mode operation, while the device pinched off at a positive gate bias of ~+5 V[13]. Similarly, the p-channel Fin-FET was demonstrated on p-GaN/AlN/AlGaN platform[14], although the high hole current of 18 mA/mm is obtained, the device pinched-off at +8 V. Despite the high on-state current reported in the previous literature, these Ⅲ-nitride heterostructures are incompatible with the matured commercialized n-channel HEMTs on p-GaN/AlGaN platform. To overcome this obstacle, the p-MOSFET on p-GaN/AlGaN platform is demonstrated. By combining the gate trench and oxygen plasma treatment, the E-mode functionality with a pinch-off voltage of ~0 V and an on-state current of 3.38 mA/mm was realized[15].

This work based on the p-GaN/AlGaN platform, the Si-rich low-pressure chemical vapor deposition (LPCVD) SiN_x was used as a gate insulator in the GaN p-channel metal-insulator-semiconductor field-effect-transistors (p-MISFETs). A record high channel hole mobility of 19.5 $cm^2/(V{\cdot}s)$ is measured. In addition, the fabricated p-MISFET delivers excellent E-mode operation with V_{TH} as negative as –2.3 V @ 10 μA/mm with a decent on-state current of 1.61 mA/mm, while the channel can be well pinched-off at 0 V (w/. low leakage current of ~1 nA/mm). A high I_{ON}/I_{OFF} = 5 × 10^5 was achieved. Moreover, the V_{TH} exhibits good stability, with hysteresis as low as 0.1 V for the gate swing up to –10 V.

2. Epitaxial structure and device fabrication

Fig. 1(a) shows the device schematic and epitaxial layers grown on a 6-inch Si substrate by metal organic chemical vapor deposition (MOCVD). The epi-structure consists a ~70 nm *p*-GaN (Mg: 3 × 10^{19} cm^{-3}), a 15-nm $Al_{0.2}Ga_{0.8}N$ barrier layer, a 1 nm AlN spacer layer, a 300 nm UID GaN channel layer, and a 4.5 μm GaN buffer layer. The epi-structure is fundamentally compatible with the mainstream that is used for n-channel p-GaN gate HEMTs[12, 13], which paves the way for potential single-chip CMOS integration.

The fabrication process is shown in Fig. 1(b). The samples were passivated with ~59 nm SiO_2 by plasma-enhanced chemical vapor deposition (PECVD). The mesa isolation was then formed using the combination of SF_6/CH_3F/He reactive ion etching (RIE) and Cl_2/BCl_3 by inductive-coupled plasma-reactive ion etching (ICP-RIE). After that, the gate was exposed by SF_6/CH_3F/He RIE to remove SiO_2, and then the p-GaN was partly removed by the optimized low-damage and low-etching-rate BCl_3 RIE. The processed samples with identical gate trench were cut into small pieces for the different gate insulators. The ~16.4 nm LPCVD-SiN_x were deposited at 785 °C, 300 mTorr. Two different gate insulators with different SiN_x stoichiometry were deposited by changing the gas flow rate of the precursors of SiH_2Cl_2 and NH_3. The SiH_2Cl_2/NH_3 flow ratios are 140/35 sccm and 35/280 sccm for Si-rich and N-rich sample, respectively. The refractive indices were measured to be 2.11 and 2.03 for Si- and N-rich sample, respectively, the higher refractive index revealed the higher

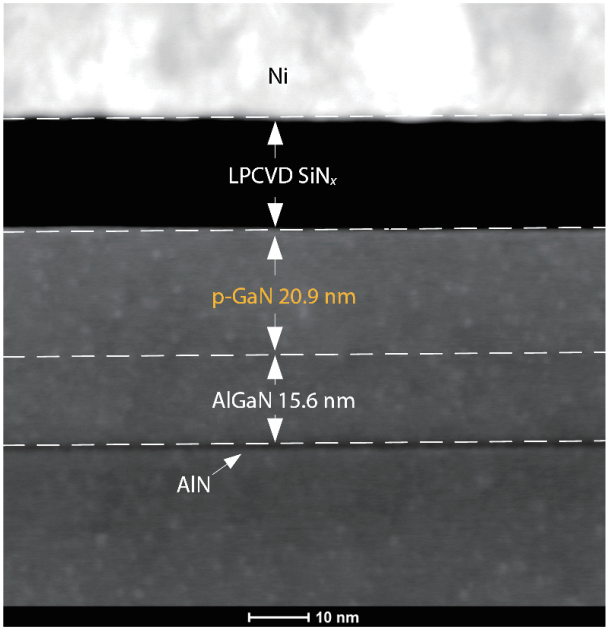

Fig. 2. (Color online) The focused ion beam section of ~22 nm channel.

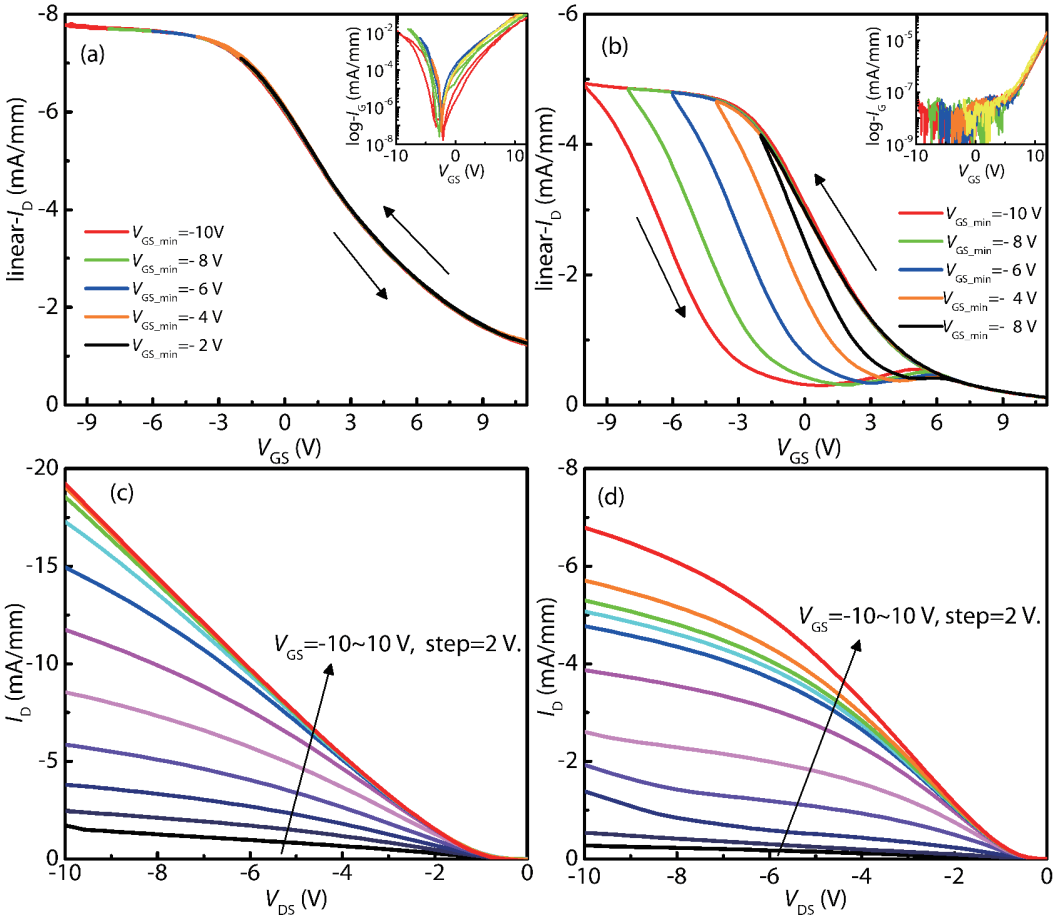

Fig. 3. (Color online) The transfer characteristic of (a) Si-rich sample and (b) N-rich sample. The output characteristic of (c) Si-rich sample and (d) N-rich.

Si/N ratio[20]. To avoid possible plasma damage on p-GaN surface, only the LPCVD-SiN_x in ohmic-window was carefully etched by SF_6/CH_3F/Ar RIE, and the rest of the SiO_2 passivation was removed in buffered-oxide-etchant (7 : 1). The ohmic contact was then formed by the evaporation of Ni/Au (15/30 nm) and annealed in O_2 ambient for 5 min at 550 °C. The gate electrode was finally formed with Ni/Au (20/150 nm) metal stacks.

Figs. 1(c) and 1(d) show the *I*–*V* characteristics of the ohmic contact by transfer-line-method (TLM) for N-rich and Si-rich samples, respectively. Both samples exhibit quite similar *I*–*V* characteristics, which suggests that the transport prop-

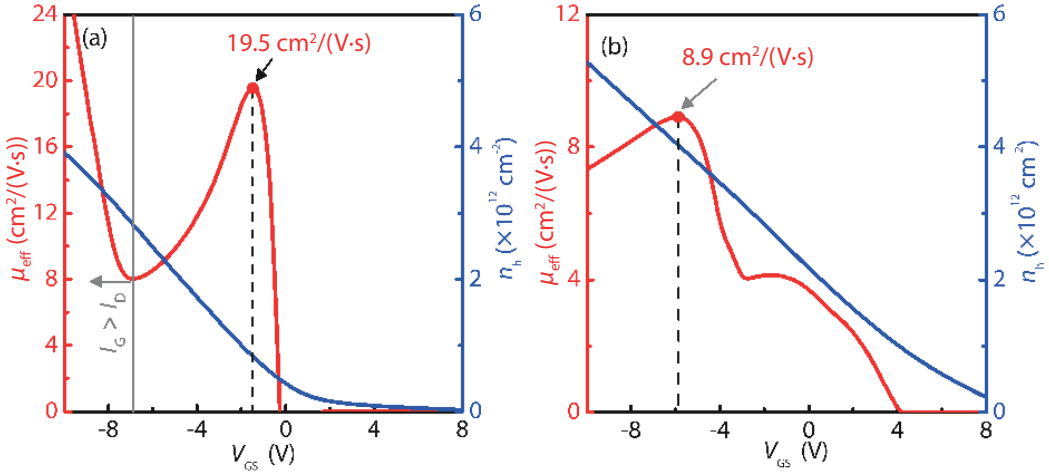

Fig. 4. (Color online) The μ_{eff} and the n_h of (a) Si-rich and (b) N-rich sample with ~48 nm trench.

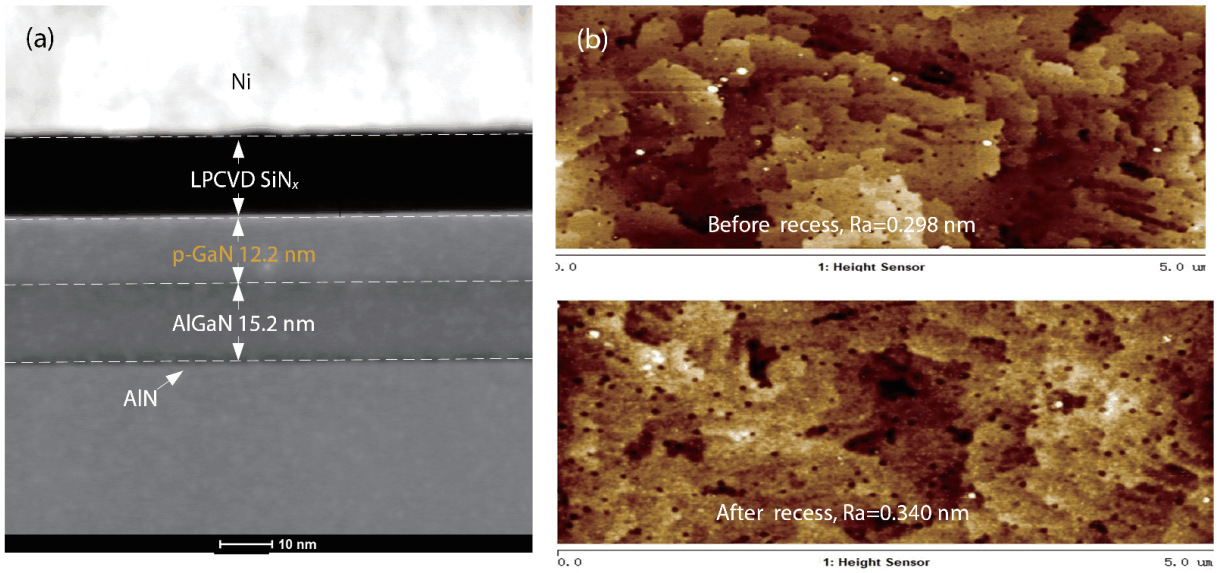

Fig. 5. (Color online) (a) The focused ion beam section of ~12 nm channel. (b) The surface morphology characterized before/after recess.

erty in the as-grown epi-structure (w/o. Ⅲ-nitride etch) is marginally affected by the stoichiometry of LPCVD-SiN_x with the SiO_2 passivation. A mobility of 16.5 cm/(V·s), hole density (n_h) of 1×10^{13} cm^{-2} and R_{sheet} of 37.5 kΩ/sq were measured by Hall measurement.

3. Results and discussion

Samples with two different gate trench depth of ~48 nm and ~58 nm were fabricated, respectively. Fig. 2 shows the cross-section view of the gate trench area with ~21.9 nm p-GaN channel (i.e., ~48 nm gate trench). The transfer characteristics are shown in the Figs. 3(a) and 3(b). The I_D of 7.78 mA/mm (@V_{GS} = −10 V, V_{DS} = −5 V) in the Si-rich sample is much higher than 4.95 mA/mm in the N-rich sample. It can be noticed that the V_{TH} hysteresis (ΔV_{TH}) was well suppressed by the Si-rich gate insulator, even for the high gate swing up to V_{GS} = −10 V. Meanwhile, the device with N-rich SiN_x gate insulator exhibited substantial ΔV_{TH}, which increased from ~−1.8 V for V_{GS} = −2 V to ~−8.0 V for V_{GS} = −10 V. The well-suppressed ΔV_{TH} in the device with Si-rich SiN_x gate insulator is attributed to the screen of the deep-level surface states at the dielectric/Ⅲ-nitride interface. Due to the insufficient gate trench depth, the devices exhibit D-mode operation. The output characteristics are shown in the Figs. 3(c) and 3(d), a R_{ON} = 0.623 kΩ·mm (@V_{DS} = 6 V) was achieved in Si-rich devices, which is lower than the 1.48 kΩ·mm of N-rich sample. This improved current conduction performance originates from the increased channel hole mobility (μ_{eff}) in the trench gate region, which was extracted from the FAT-FET (L_G/W_G = 64/100 μm) and given by the Eq. (1)[19].

$$\mu_{eff} = \frac{L_G G_{ch}}{W_G Q_h}, G_{ch} = \frac{\partial I_D}{\partial V_{DS}} I_{V_G}, \quad (1)$$

the drain–source conductance (G_{ch}) was measured at V_D = 0.2 V and the n_h was given by integration of C–V results (not shown). As shown in Figs. 4(a) and 4(b), a much higher channel mobility of 19.5 cm²/(V·s) is measured in the Si-rich sample, while the channel mobility is only 8.9 cm²/(V·s) in the N-rich sample. The measurements reveal that the Si-rich gate insulator can effectively improve the channel hole mobility in the p-GaN/AlGaN heterostructure, which can be further used to improve the current conduction capability of E-mode GaN p-FET. The measured μ_{eff} shows anomalous characteristic for V_{GS} < −7 V (Fig. 4(a)), owing to the increased gate leakage (I_G)

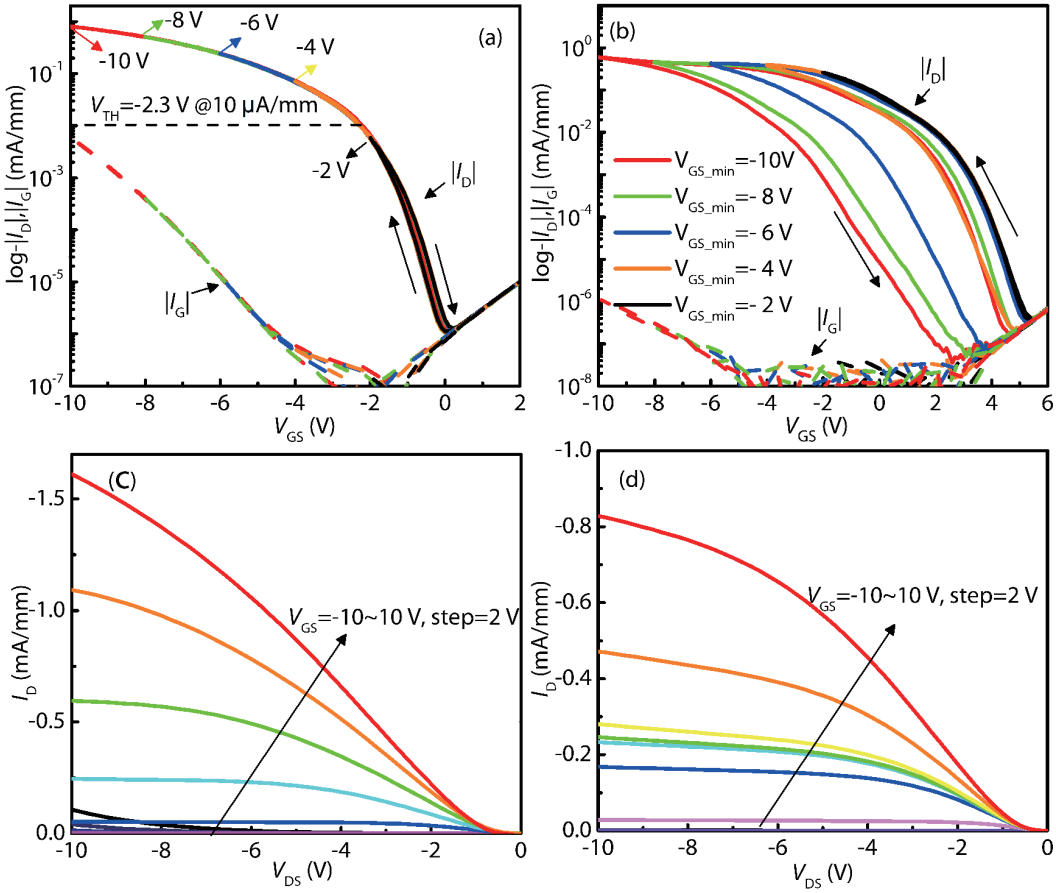

Fig. 6. (Color online) The transfer characteristic of (a) Si-rich sample and (b) N-rich sample. The output characteristic of (c) Si-rich sample and (d) N-rich.

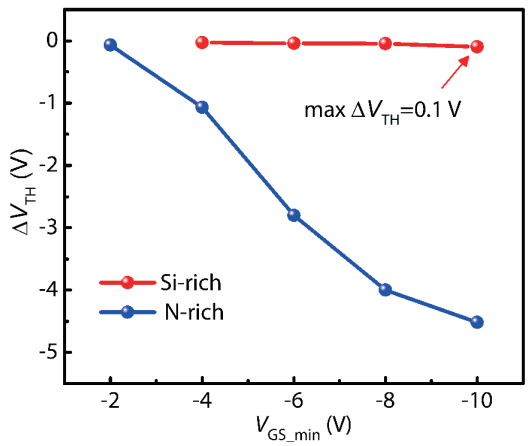

Fig. 7. (Color online) The ΔV_{TH} with different V_{GS} sweep ranges.

in the FAT-FET with a large gate length (i.e., 64 μm) at a more negative V_{GS}.

Given that the mobility modulation effect has been observed in the D-mode Si-rich samples, the sample with deeper gate trench of ~58 nm, as shown in the Fig. 5(a), was further processed to realize the E-mode p-MISFETs. The device dimensions are $L_G/L_{GS}/L_{GD}$ = 1.9/2.7/2.7 μm. Fig. 5(b) shows the surface morphology characterized by atomic force microscope (AFM) before and after gate recess. Benefiting from the optimized low damage and low etch-rate gate recess process, the recessed surface roughness is well suppressed and quite comparable to the as grown p-GaN/AlGaN surface. The transfer characteristic shows that a respectable negative V_{TH} = −2.3 V (@ I_D = 10 μA/mm) was achieved in the Si-rich sample (Fig. 6(a)), while the device features an excellent pinch-off at 0 V with a low leakage current of ~1 nA/mm. These device characteristics demonstrate that the device delivers an excellent E-mode operation. Meanwhile, a high ON/OFF current ratio (I_{ON}/I_{OFF}) of 5 x 10^5 is obtained. More importantly, the sufficiently negative V_{TH} exhibits good stability with ΔV_{TH}, as small as 0.1 V under V_{GS} sweep to −10 V (Fig. 7). Even though previous studies have reported that V_{TH} stability is critical for p-MISFET to deliver proper and stable operation, which determines the decent functionality of GaN CMOS integration circuits, the V_{TH} stability of GaN p-MISFET has rarely been reported to date[16, 22–24]. The extremely small ΔV_{TH} measured in this work is among the best reported results[16, 24].

The excellent V_{TH} stability benefits from the Si-rich LPCVD-SiN_x used for gate dielectric. The Si-rich LPCVD-SiN_x leaves high-density Near-Conduction-Band (NCB) Si-rich LPCVD-SiN_x/Ⅲ-V interface states, which are ionized and act as fixed positive charges[21]. As illustrated in Fig. 8(a), the high-density positive charges enable the energy-band to bend more downward near the SiN_x/p-GaN interface, which presents a potential hole barrier. More importantly, the downward band bend keeps the hole traps at the LPCVD-SiN_x/p-GaN interface away from the Fermi-level (E_F). In contrast, owing to the lower density NCB interface states and the corresponding fixed positive charges, the N-rich sample exhibits less downward band bend, as shown in Fig. 9(a). The ΔV_{TH} is induced by trapping/de-trapping of hole traps located at

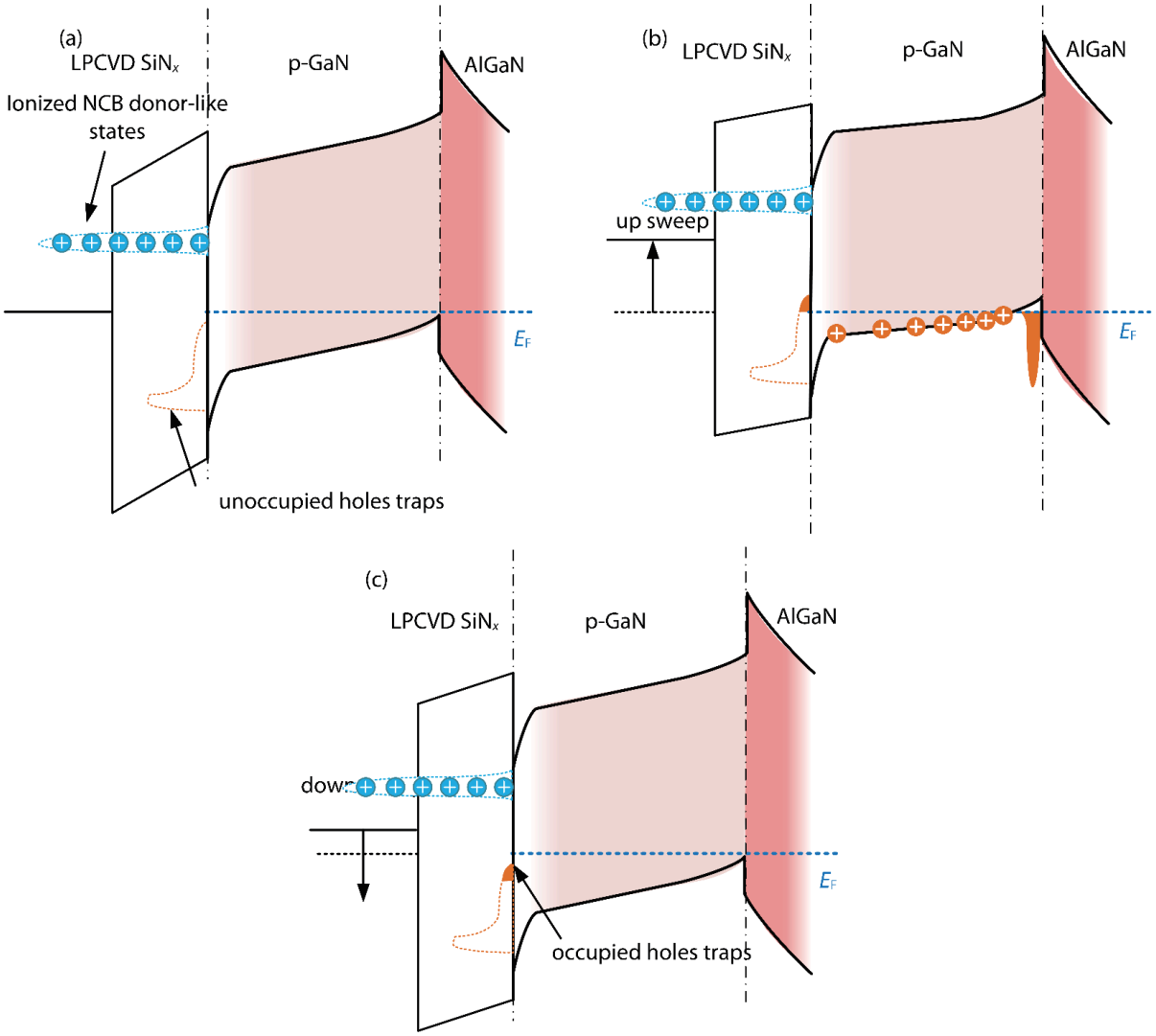

Fig. 8. (Color online) The Band diagram schematics of the MIS gate of Si-rich sample during the (a) initial state, (b) up sweep and (c) down back.

dielectric/p-GaN interface in the GaN p-FETs[23]. Due to the different band bending, during the gate bias negative sweep-up process, less hole traps are occupied in the Si-rich sample (Fig. 8(b)) while more traps are filled in the N-rich sample (Fig. 9(b)). The less un-ionized hole traps lead to the negligible V_{TH} shift, as observed in the Si-rich sample during the down back process in this manner (Fig. 8(c) vs. Fig. 9(c)).

A comparison of the output characteristics shown in Figs. 6(c) and 6(d) shows that the Si-rich LPCVD-SiN_x gate dielectric is effective in improving the current conduction capability of GaN p-MISFET on p-GaN/AlGaN platform. Figs. 10(a) and 10(b) show the μ_{eff} extracted from FAT-FET (L_G/ W_G = 64/100 μm), the maximum channel hole mobility of 19.4 $cm^2/(V{\cdot}s)$ is measured in the Si-rich sample, which is much larger than 8.1 $cm^2/(V{\cdot}s)$ in N-rich sample. Owing to the substantially improved channel mobility, the device with Si-rich gate dielectric delivers a decent high I_D of −1.6 mA/mm at V_{GS} = −10 V, which is double to that in the device with N-rich gate dielectric. It should be noted that the dimension of the fabricated device features large gate length L_G of 1.9 μm and overall source-to-drain distance of 7.4 μm, due to the photolithography limit. It can be inferred from this that the drive current of the device can be further enhanced by shrinking the dimensions of the device.

Table 1 gives the benchmark of the typical device parameters of GaN p-FETs in the recently reported literature. It can be noted that even by adopting stringent criteria of 10 μA/mm to define the V_{TH}, the E-mode p-MISFET that is fabricated in this work features a negative V_{TH} of −2.3 V, which enables the essential E-mode operation of the GaN p-MISFET. The V_{TH} also exhibits superior stability when compared with the reported results[25]. Most importantly, even when compared with the intrinsic hole mobility reported in the access region without Ⅲ-nitride etching[12–15], the channel hole mobility extracted from the E-mode gate region in this work is higher. This superior channel mobility leads to the decent drain current in the E-mode p-MISFET, even when featuring the negative V_{TH} and large device dimension. The improved channel mobility may stem from the additional strain that is induced by the Si-rich LPCVD-SiN_x gate dielectric. It is reported that even a slight increase of 2% for tensile strain can induce a substantial hole mobility increase from 42 to 113 $cm^2/(V{\cdot}s)$ in GaN[25]. By increasing the S/N ratio of the SiN_x passivation dielectric, we can effectively enhance the tensile strain in Ⅲ-nitride material[26].

4. Conclusion

In this work, a technique for improving the hole mobility in gate recessed E-mode GaN p-FETs was first demonstrated. A record high V_{TH} of −2.3 V was achieved in the device with ~58 nm gate trench, which enables decent E-mode

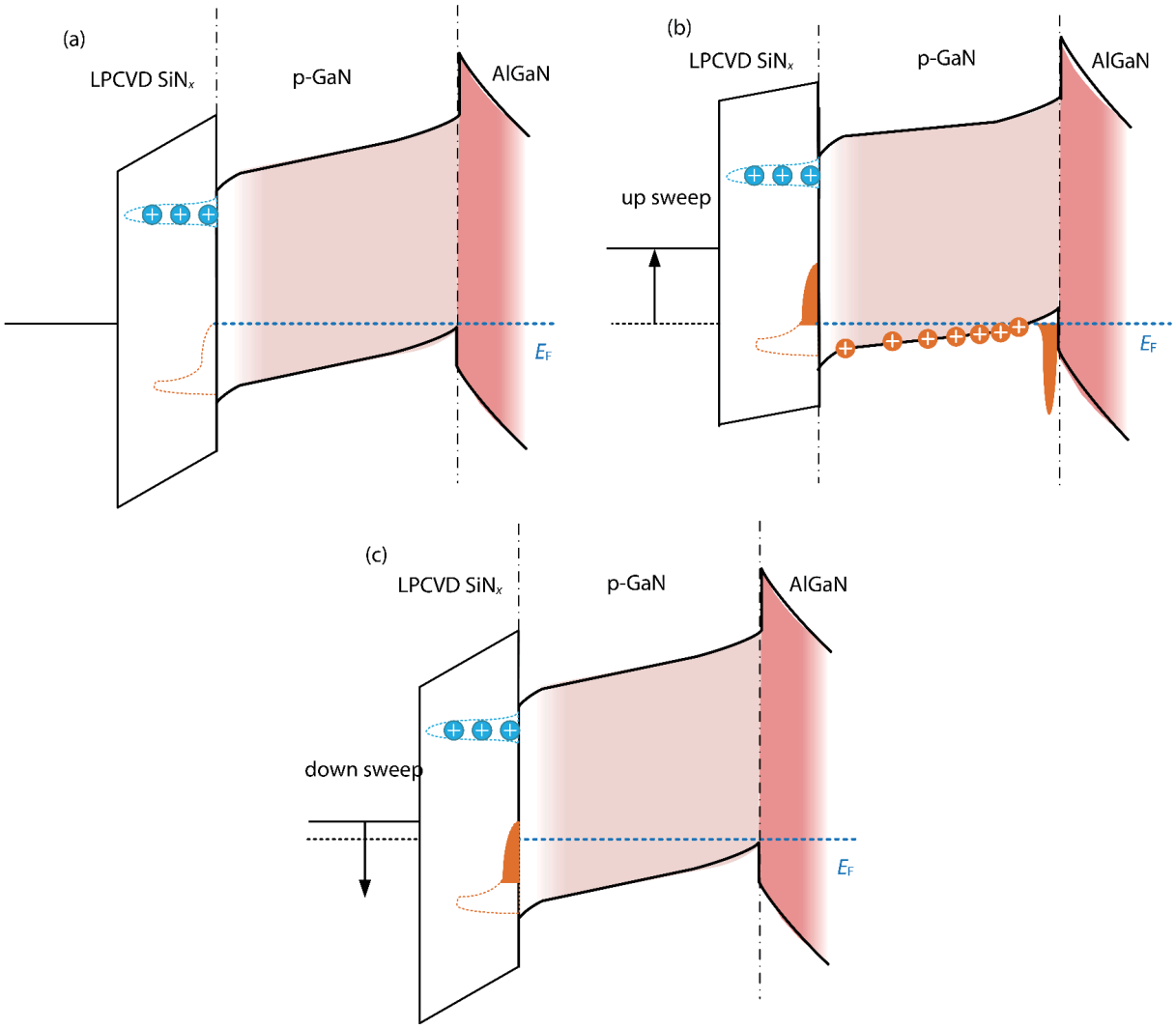

Fig. 9. (Color online) the Band diagram schematics of the MIS gate of N-rich sample during the (a) initial state, (b) up sweep and (c) down back.

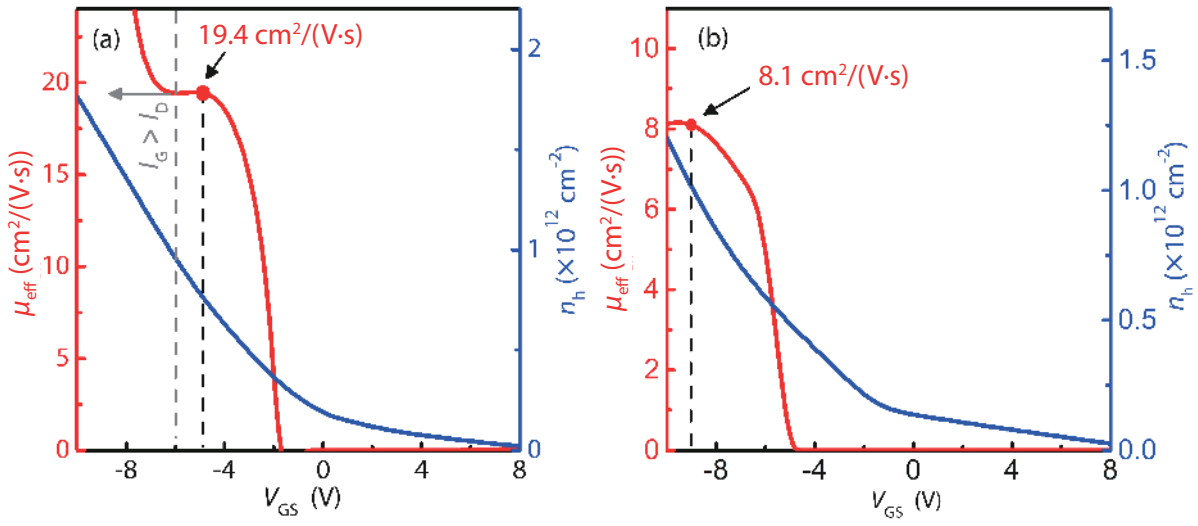

Fig. 10. (Color online) The μ_{eff} and the n_h of (a) Si-rich and (b) N-rich sample with ~58 nm trench.

operation of the device. A maximum hole mobility μ_{eff} of ~19.4 cm^2/(V·s), which is the highest value for the reported gate recessed E-mode GaN p-FETs, was achieved by using the Si-rich LPCVD-SiN$_x$ gate insulator. Additionally, the V_{TH} hysteresis was also well suppressed by the Si-rich gate insulator. These results suggest the Si-rich LPCVD-SiN$_x$ is a promising gate insulator for high performance E-mode GaN p-FETs based on p-GaN/AlGaN/GaN heterostructure.

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Table 1. Benchmark of typical parameters of GaN p-FETs.

Group	Mobility ($cm^2/(V·s)$)	I_{ON}/I_{OFF} [f]	V_{TH} (V)	ΔV_{TH} (V@V_{GS_min})	R_{ON} (kΩ·mm)
This work	**19.4[a]**	5×10^5	**−2.3[c]**	**−0.1 (@-10 V)**	5.7
Xidian[14]	2[b]	~10^2	−2.2[d]	N. A.	0.54
Sheffield[16]	11.8[a]	~10^7	−0.73[c]	−0.12 (@−8 V)	1
HKUST[24]	N. A.[e]	~2×10^7	−1.7[c]	~−0.1 (@−6 V)	0.65
SINANO[22]	11[b]	~10^6	−2.7[c]	−2.4 (@−12 V)	0.061
MIT[12]	15[b]	~10	3.5[d]	N. A.	2.3
MIT[13]	11[b]	~10	−0.3[d]	N. A.	2.3
MIT[18]	10[a]	~10^2	−1	N. A.	2.4
MIT[17]	7.5[a]	~10^6	2	N. A.	
HKUST[15]	10.2[b]	~2×10^7	−1.7[c]	N. A.	

[a] mobility in channel; [b] mobility in access region;
[c] defined at I_D = 0.01 mA/mm; [d] defined by linear-extrapolation;
[e] N. A. is abbreviation for "not available"; [f] I_{OFF} in here was the current when V_{GS} is biased to 0 V.

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