COMMENTS AND OPINIONS

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Vertical β-Ga_2O_3 power electronics

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β-Ga_2O_3 possesses a highly promising critical electric field of 8 MV/cm, allowing devices with improved performance compared with other wide bandgap materials[1, 2]. The 4-inch wafers grown from a melt and over 10 μm of the epitaxial layers grown by Halide vapor phase epitaxy (HVPE) with highly controllable doping concentration, are commercially available, paving the way of vertical power devices. The β-Ga_2O_3 community has consistently elevated the average critical electric field superior to SiC or GaN, which is suitable for medium/high voltage infrastructures demanding over 900 V[1]. Vertical β-Ga_2O_3 power electronics have made a tremendous progress in recent years, such as various surface/interface engineering, diverse edge termination, quasi-inversion vertical transistor, etc.

"The interface is the device" was coined by Nobel laureate Herbert Kroemer. This famous phrase is also applicable to β-Ga_2O_3 diodes. **Several surface/interface engineering methods have been applied including pre-treatment, surface etching, oxidized metal and annealing.**

(1) There are several pre-treatment methods available to ensure a reliable surface before fabricating the Schottky metal. The performance of Schottky barrier diodes (SBDs) can be significantly enhanced by employing pre-treatment methods such as piranha, Hydrochloric acid (HCl), acetone, and UV ozone. These methods can lead to improved characteristics, including near-ideal ideality factors and higher breakdown capabilities in SBDs[3].

(2) During the device preparation process, the surface of gallium oxide probably adsorbs part of the gas molecule from the surrounding environment. The performance and uniformity of devices can be significantly improved by employing dry etching techniques and minimizing the time exposed to ambient air during the preparation process[4]. However, the insight of excellent β-Ga_2O_3 surface needs to be more investigated such as surface energy, surface absorption, dangling bonds, chemical ratios, and so on. On the other hand, it is crucial to establish a universal and simple surface treatment method that can make sure every β-Ga_2O_3 team reaches the first-rate baseline device in the near future.

(3) By inserting oxidized metal layer like PtO_x or $PdCoO_x$ in Schottky contact can lead to a higher barrier height, thereby reducing the leakage current density and improving the breakdown characteristics. However, this approach may not be conducive for the turn-on voltage[5–7]. Combination with low work-function metal may be a preferable route for low power loss diodes[8].

(4) Annealing at oxygen environment is believed to passivate the oxygen vacancies and compensate for the surface charge from 300 °C to 1000 °C. Compensation of the surface charge not only reduces the image forces lowering but also increases the electron tunneling width, resulting in the increased Schottky barrier height and the reduced reverse leakage current[9]. Post metallization annealing at nitrogen environment can significantly reduce the interface states, which can lead to a substantial improvement in the breakdown voltage and a significant reduction in the *I*–*V* hysteresis of the device[10].

The interface quality is the baseline to ensure the performance of device. However, with the transition of planar junction to cylindrical junction at the edge of anode, the edge electric field crowding effect becomes apparent. Thus the implementation of **edge termination techniques** was reached to a high level of difficulty due to the extremely high critical electric field. **These techniques include the use of field plate, high-resistivity, heterojunction termination extension (JTE) and etched mesa termination**, as shown in Fig. 1.

(1) The silicon dioxide is commonly used as dielectric for other semiconductors. However, the permittivity of silicon dioxide is relatively low compared to that of β-Ga_2O_3, making silicon dioxide less prone to experiencing breakdown before β-Ga_2O_3[11]. Researchers have chosen high-k dielectric as the gallium oxide field plate and obtained good performance[12].

(2) The high-resistance zone formed by ion implantation or oxygen annealing promotes the spreading of the potential along the surface and suppresses leakage current[13–15]. Lattice damage and deep acceptor may affect the reliability and switching characteristics of devices.

(3) The JTE technique is a very effective technique commonly used in commercial Si and SiC devices. The p-type NiO can expand the depletion boundary to reduce the peak electric field[16–18]. The effectiveness of NiO has been verified to improve the reverse characteristic. The mechanism behind conductivity modulation in the device, which grants it the ability to withstand surge events, remains somewhat mysterious.

(4) Mesa termination provides a simple and cost-effective method, which the peak electric field can be transfered from contact edge to the mesa corner[19–21]. Further optimizations can be made by refining the etching process to effectively control sidewall damage and interface charge.

Currently, **there have been four kinds of vertical transistors demonstrated in β-Ga_2O_3,** including Fin field-effect tran-

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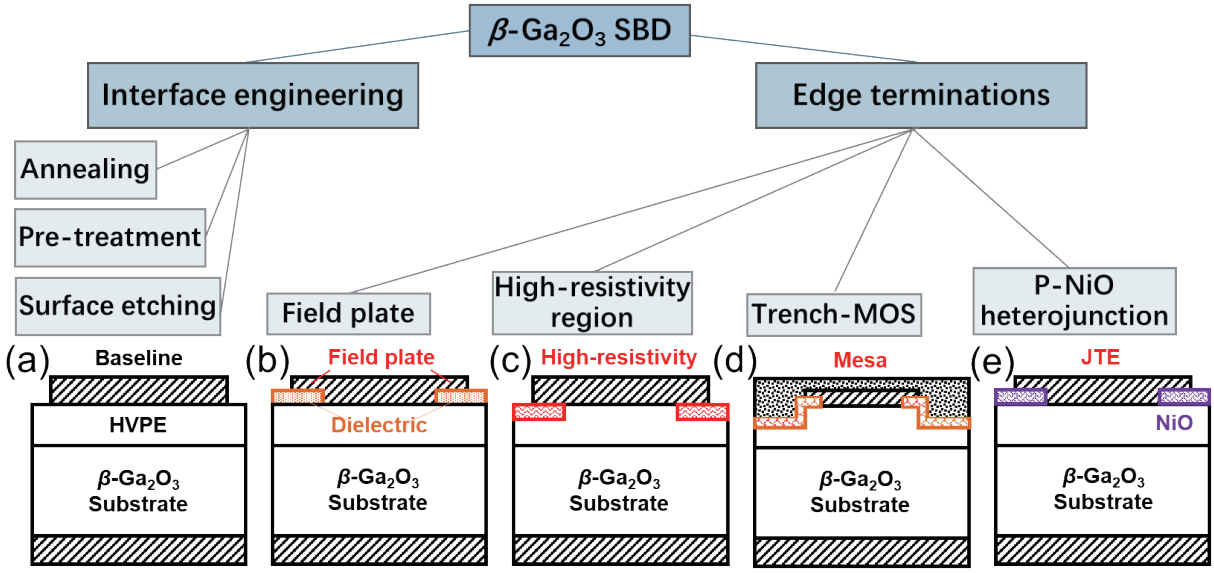

Fig. 1. (Color online) The schematic diagram of the roadmap and structures for SBDs. Surface engineering technique (a), and edge termination techniques (b-e) have emerged in recent years.

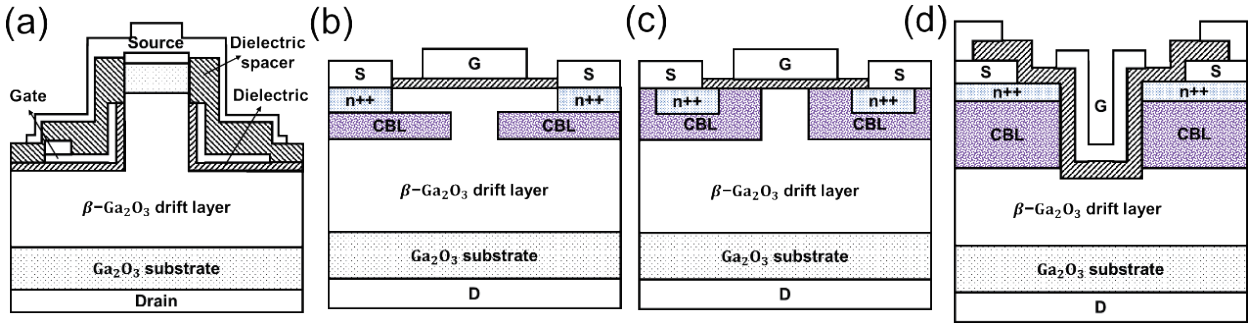

Fig. 2. (Color online) The schematic diagram of four kinds of vertical transistors, (a) fin field-effect transistor (FinFET), (b) current aperture vertical electron transistor (CAVET), (c) vertical diffused barrier field-effect transistor (VDBFET), and (d) U-shaped gate trench MOSFET (U-MOSFET).

sistor (FinFET), Current aperture vertical electron transistor (CAVET), Vertical diffused barrier field-effect transistor (VDBFET) and U-shaped gate trench MOSFET (U-MOSFET), as shown in Fig. 2.

(1) The FinFET shows strong gate control of the channel and reaches a very high breakdown voltage. Drain-induced barrier lowering (DIBL) has been observed in β-Ga_2O_3 FinFETs, and was found to be the dominant breakdown mechanism in these devices[22]. Fabrication complexity is one of the challenges for FinFETs, as FinFETs have to be realized by fine line lithography and are dependent on sidewall channels formed by dry etching.

(2) The CAVET consists of the highly resistive current blocking layers (CBLs) around the conductive aperture to confine the current path. A robust CBL and a clean dielectric/semiconductor interface are needed for sustaining high reverse voltage and promoting effective/stable channel modulation respectively. Proper designs of doping schemes and aperture conductivity are also vital[23].

(3) In VDBFETs or UMOSFETs, a quasi-inversion conductive channel can be formed at the surface of the CBL under a proper gate voltage[24, 25]. These structures were intrinsically E-mode as the channel naturally remains non-conductive at zero gate bias because of the blocking capability of the highly resistive CBLs. CBLs realized by selective diffusion by Mg doping spin-on-glass, oxygen annealing, N implantation and N impurities during epitaxy have great impact on conduction and voltage blocking characteristics of the transistors[26]. Oxygen annealing offers the advantage of avoiding lattice damage, unlike nitrogen implantation, and the CBL formed by oxygen annealing generating the gallium vacancies at more than 1000 °C is more stable. Additionally, oxygen annealing can form a thicker CBL depth, which is important for minimizing punch-through current and improving breakdown voltage. On the contrary, nitrogen implantation-based UMOSFET devices have more advanced performance and better controllability of CBL profile, but they come with the drawbacks of higher cost, lattice damage, and larger device leakage current. Generally speaking, UMOSFET has shown promising performance, with N implantation-based UMOSFET surpassing the unipolar theoretical limit of Si-based devices[27]. Nevertheless, its breakdown voltage remains inferior to that of FinFET, which requires further optimization. The mechanism and controllability of the oxygen annealing process need further exploration. In addition, the device shows a nonlinear turn-on of the output current, necessitating additional investigation to understand and improve this characteristic.

After a decade of development, β-Ga_2O_3 power devices have made great progress so far. However, **several challenges and issues still persist**.

(1) The breakdown voltage and PFOM of large area devices are far inferior to the small-size devices. The high defect density and severe interface damage greatly affect device performance. To address these issues, techniques such as high aspect ratio ICP etching and BOE surface damage repair can be employed.

(2) The absence of p-type doping in β-Ga_2O_3 poses a challenge in the development of power devices. On the one hand, we can use mesa structure or high resistivity region or PtO_x/p-NiO-based junction engineering to reduce off-state leakage. On the other hand, optimizing the thermal oxygen process/nitrogen implantation process/*in situ* epitaxy, studying the leakage mechanism and the formation mechanism of compensating defects will also help.

(3) The low thermal conductivity is also a big problem. Thinning the substrate combined with double-side packaging or flip-chip packaging may abate this inherent vice. Of course, these problems in the development of gallium oxide power devices still require the efforts of international community to promote the early industrialization of gallium oxide power devices.

In summary, the current maximum commercial wafer size is 100 mm, containing an n^+ monocrystalline substrate and an n^- HVPE epitaxial layer. Increasing the wafer size further would lead to a reduction in the fabrication cost of gallium oxide devices. The development of interface engineering and various edge termination techniques has continually pushed the boundaries of β-Ga_2O_3 high-performance devices. U-MOSFET shows promise as potential solutions for β-Ga_2O_3 power transistors, but this structure has many uncertainties such as breakdown voltage and reverse recovery characteristics. In-depth exploration of device physics mechanisms related to interface defects and intrinsic defects is necessary. Reliable soft breakdown and ideal reverse leakage have not been achieved. Additionally, attention should be given to the development of ampere-level diodes/transistors and improving device reliability.

References

[1] Green A J, Speck J, Xing G, et al. β-Gallium oxide power electronics. APL Mater, 2022, 10, 029201

[2] Yuan Y, Hao W B, Mu W X, et al. Toward emerging gallium oxide semiconductors: A roadmap. Fundam Res, 2021, 1, 697

[3] Chen H, Wang H Y, Wang C, et al. Low specific on-resistance and low leakage current β-Ga_2O_3 (001) Schottky barrier diode through contact pre-treatment. 2022 IEEE 34th International Symposium on Power Semiconductor Devices and ICs (ISPSD), 2022, 145

[4] He Q M, Hao W B, Zhou X Z, et al. Over 1 GW/cm^2 vertical Ga_2O_3 Schottky barrier diodes without edge termination. IEEE Electron Device Lett, 2022, 43, 264

[5] Hou C X, Gazoni R M, Reeves R J, et al. Oxidized metal Schottky contacts on (010) β-Ga_2O_3. IEEE Electron Device Lett, 2019, 40, 337

[6] Jian G Z, Hao W B, Shi Z Y, et al. Elevated barrier height originated from electric dipole effect and improved breakdown characteristics in PtO_x/β-Ga_2O_3 Schottky barrier diodes. J Phys D: Appl Phys, 2022, 55, 304003

[7] Harada T, Ito S, Tsukazaki A. Electric dipole effect in $PdCoO_2$/β-Ga_2O_3 Schottky diodes for high-temperature operation. Sci Adv, 2019, 5, eaax5733

[8] Xiong W H, Zhou X Z, Xu G W, et al. Double-barrier β-Ga_2O_3 Schottky barrier diode with low turn-on voltage and leakage current. IEEE Electron Device Lett, 2021, 42, 430

[9] Lingaparthi R, Sasaki K, Thieu Q T, et al. Surface related tunneling leakage in β-Ga_2O_3 (001) vertical Schottky barrier diodes. Appl Phys Express, 2019, 12, 074008

[10] Hao W B, He Q M, Zhou K, et al. Low defect density and small I–V curve hysteresis in NiO/β-Ga_2O_3 pn diode with a high PFOM of 0.65 GW/cm^2. Appl Phys Lett, 2021, 118, 043501

[11] Konishi K, Goto K, Murakami H, et al. 1-kV vertical Ga_2O_3 field-plated Schottky barrier diodes. Appl Phys Lett, 2017, 110, 103506

[12] Roy S, Bhattacharyya A, Peterson C, et al. 2.1 kV (001)-β-Ga_2O_3 vertical Schottky barrier diode with high-k oxide field plate. Appl Phys Lett, 2023, 122, 152101

[13] He Q M, Zhou X Z, Li Q Y, et al. Selective high-resistance zones formed by oxygen annealing for-GaO Schottky diode applications. IEEE Electron Device Lett, 2022, 43, 1933

[14] Lin C H, Yuda Y, Wong M H, et al. Vertical Ga_2O_3 Schottky barrier diodes with guard ring formed by nitrogen-ion implantation. IEEE Electron Device Lett, 2019, 40, 1487

[15] Lu X, Zhang X, Jiang H X, et al. Vertical β-Ga_2O_3 Schottky barrier diodes with enhanced breakdown voltage and high switching performance. Phys Status Solidi A, 2020, 217, 1900497

[16] Hao W B, He Q M, Zhou X Z, et al. 2.6 kV NiO/Ga_2O_3 heterojunction diode with superior high-temperature voltage blocking capability. 2022 IEEE 34th International Symposium on Power Semiconductor Devices and ICs (ISPSD), 2022, 105

[17] Hao W B, Wu F H, Li W S, et al. High-performance vertical β-Ga_2O_3 Schottky barrier diodes featuring P-NiO JTE with adjustable conductivity. 2022 International Electron Devices Meeting (IEDM), 2023, 9.5.1

[18] Hao W B, Wu F H, Li W S, et al. Improved vertical β-Ga_2O_3 Schottky barrier diodes with conductivity-modulated p-NiO junction termination extension. IEEE Trans Electron Devices, 2023, 70, 2129

[19] Sasaki K, Wakimoto D, Thieu Q T, et al. First demonstration of Ga_2O_3 trench MOS-type Schottky barrier diodes. IEEE Electron Device Lett, 2017, 38, 783

[20] Li W S, Nomoto K, Hu Z Y, et al. Field-plated Ga_2O_3 trench Schottky barrier diodes with a BV^2/R_{on}, R_{sp} of up to 0.95 GW//cm^2. IEEE Electron Device Lett, 2020, 41, 107

[21] Li W S, Nomoto K, Hu Z Y, et al. Fin-channel orientation dependence of forward conduction in kV-class Ga_2O_3 trench Schottky barrier diodes. Appl Phys Express, 2019, 12, 061007

[22] Li W, Nomoto K, Hu Z, et al. Single and multi-fin normally-off Ga_2O_3 vertical transistors with a breakdown voltage over 2.6 kV. 2019 IEEE International Electron Devices Meeting (IEDM), 2020, 12.4.1

[23] Wong M H, Murakami H, Kumagai Y, et al. Enhancement-mode β-Ga_2O_3 current aperture vertical MOSFETs with N-ion-implanted blocker. IEEE Electron Device Lett, 2020, 41, 296

[24] Zeng K, Soman R, Bian Z L, et al. Vertical Ga_2O_3 MOSFET with magnesium diffused current blocking layer. IEEE Electron Device Lett, 2022, 43, 1527

[25] Zhou X Z, Ma Y J, Xu G W, et al. Enhancement-mode β-Ga_2O_3 U-shaped gate trench vertical MOSFET realized by oxygen annealing. Appl Phys Lett, 2022, 121, 223501

[26] Wakimoto D, Lin C H, Thieu Q T, et al. Nitrogen-doped β-Ga_2O_3 vertical transistors with a threshold voltage of ⩾1.3 V and a channel mobility of 100 $cm^2V^{-1}s^{-1}$. Appl Phys Express, 2023, 16, 036503

[27] Ma Y J, Zhou X Z, Tang W B, et al. 702.3 A·cm^{-2}/10.4 mΩ·cm^2 β-Ga_2O_3 U-shape trench gate MOSFET with N-ion implantation. IEEE Electron Device Lett, 2023, 44, 384

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