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REVIEWS

A comprehensive review of recent progress on enhancement-mode β-Ga_2O_3 FETs: Growth, devices and properties

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Abstract: Power electronic devices are of great importance in modern society. After decades of development, Si power devices have approached their material limits with only incremental improvements and large conversion losses. As the demand for electronic components with high efficiency dramatically increasing, new materials are needed for power device fabrication. Beta-phase gallium oxide, an ultra-wide bandgap semiconductor, has been considered as a promising candidate, and various β-Ga_2O_3 power devices with high breakdown voltages have been demonstrated. However, the realization of enhancement-mode (E-mode) β-Ga_2O_3 field-effect transistors (FETs) is still challenging, which is a critical problem for a myriad of power electronic applications. Recently, researchers have made some progress on E-mode β-Ga_2O_3 FETs via various methods, and several novel structures have been fabricated. This article gives a review of the material growth, devices and properties of these E-mode β-Ga_2O_3 FETs. The key challenges and future directions in E-mode β-Ga_2O_3 FETs are also discussed.

Key words: enhancement mode; FETs; β-Ga_2O_3

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1. Introduction

Modern society heavily relies on various electronics, such as consumer electronics, vehicles, solid-state lighting, etc. And power electronic devices are at the core of power and energy systems. Since the invention of silicon based modern electronic devices in the 1950s[1], silicon has gradually become the choice of fundamental semiconductor material in power devices. However, with the skyrocketing demand for power consumption and conversion, silicon-based power devices have already reached their material limit[2]. Novel semiconductor materials are needed to support high-efficiency, high-power, high-voltage applications.

To solve this problem, third-generation wide/ultrawide bandgap semiconductors, such as SiC, GaN and Ga_2O_3, have been extensively explored for fabricating future power electronics. To date, some SiC and GaN power devices have already achieved commercialization. For example, the fast chargers based on SiC power devices have already been applied in the charging pile for some new energy automobiles[3, 4]. However, the high cost of homogeneous bulk substrates has hindered the wide adoption of these devices, since the heteroepitaxy of semiconductors is unstable in epitaxy quality. Recently, beta-phase gallium oxide has drawn much interest due to its excellent properties. The ultra-wide bandgap of 4.9 eV and costless melt-grown substrates make β-phase Ga_2O_3 ideal for large-scale and high-power devices[5].

Figs. 1(a) and 1(b) show the bandgap dependences of the breakdown field and theoretical limits of on-resistances (R_{on}) as a function of breakdown voltage (BV) among various kinds of semiconductor material, respectively[6]. Here β-Ga_2O_3 exhibits excellent breakdown voltage and on-resistance compared with GaN and SiC. Such property ranks only second to the diamond material, while the diamond semiconductor is not affordable for most of the power device production. In fact, the relationship between breakdown voltage and the on-resistances follows an exponential relationship[1]:

$$R_{on} = \frac{4BV^2}{\varepsilon_S \mu_n E_C^3},$$

where ε_S, μ_n, and E_C are the relative dielectric constant, electron mobility and breakdown electric field, respectively. The $\varepsilon_S \mu_n E_C^3$ is defined as Baliga's figure of merit (BFOM), which is usually used for comparing power electronic performance of different semiconductors. The comparison of BFOM along with other physical properties can be seen in Table 1. β-Ga_2O_3 here shows much higher BFOM than GaN and SiC for power electronics[6].

Recently, various studies on the design and fabrication of lateral β-Ga_2O_3 field-effect transistors (FETs) have been established. The growth of β-Ga_2O_3 epitaxial layers have been achieved via various methods, including metalorganic chemical vapor deposition (MOCVD)[7–9], molecular beam epitaxy (MBE)[10, 11], halide vapor phase epitaxy (HVPE)[12–14], etc. The n-type β-Ga_2O_3 FET channel can be easily achieved and controlled by doping with shallow donor elements like Sn[15–17], Si[18, 19], Ge[17, 20], Zr[21], and Hf[22]. Ohmic contacts in the

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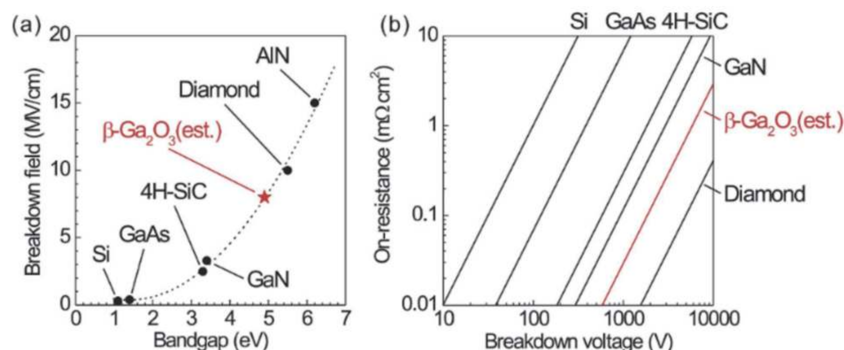

Fig. 1. (Color online) (a) The dependences between the breakdown field and bandgap. (b) Theoretical limits of the relation between on-resistances and breakdown voltage for major semiconductors and β-Ga_2O_3. © 2012 American Institute of Physics. Reprinted with permission from Ref. [6].

Table 1. Comparison of the physical properties of Si, GaN, SiC, and β-Ga_2O_3.

Semiconductor material	Si	GaN	4H-SiC	β-Ga_2O_3
E_g (eV)	1.1	3.4	3.3	4.7-4.9
μ (cm^2/(V·s))	1400	1200	1000	300
E_{br} (MV/cm)	0.3	3.3	2.5	8
BFOM	1	870	340	3444
λ (W/(cm·K))	1.5	2.1	2.7	0.11

source and drain region are usually defined using Si^+ ion implantation. With all this preparation, the first β-Ga_2O_3 MOSFETs with gate-connected field plate (GFP) was developed by Wong *et al*. in 2016[23], and the source-connected field plate (SFP) MOSFETs were also demonstrated by Lv *et al*.[24]. The device fabricated by Sharma *et al*.[25] in 2020 showed extremely high BV of 8.03 kV using composite GFP and polymer passivation, which is the highest breakdown voltage in β-Ga_2O_3 MOSFETs as recorded. Besides, vertical β-Ga_2O_3 FETs have been accomplished in recent years based on the former design of GaN[26] and SiC[27]. Even though these vertical devices are still facing some difficulties such as the lack of stability and the mismatch of the present electrical system, the potential of breakdown voltage and possibity of higher forward current make it another candidate for future applicable β-Ga_2O_3 FETs.

However, fabricating enhancement-mode β-Ga_2O_3 FET is still challenging due to some issues from the material properties of β-Ga_2O_3. The main problem is the lack of p-type doping. The high effective hole mass causing by the flat valence band of β-Ga_2O_3 severely restricts the hole mobility, and self-trapping of holes also prevents the formation of p-type doping β-Ga_2O_3[28]. It is worth noting that the lack of p-type doping is also the reason for designing unipolar β-Ga_2O_3 MOSFETs. Hence, several novel structures of E-mode FETs have now been developed, such as trench MOSFETs[29], ferroelectric gate dielectric[30], optimized doping channel[31], etc. Besides, the NiO/β-Ga_2O_3 p–n diode has already been fabricated[32], which has been expected to solve the p-type doping problem of β-Ga_2O_3 devices.

This article focuses on reviewing the current advances of E-mode β-Ga_2O_3 FETs. This review will first talk about the lateral E-mode β-Ga_2O_3 FETs, including a brief introduction of the β-Ga_2O_3 MOCVD growth at the beginning. The novel design and key parameters of recently reported E-mode lateral β-Ga_2O_3 FET will be intensively discussed afterward as a main section. Next, the recent prograss of vertical E-mode β-Ga_2O_3 FETs will also be reviewed. Other optimizations of breakdown voltage and on-resistance are also presented at the end in order to completely describe the development of β-Ga_2O_3 power devices.

2. Lateral β-Ga_2O_3 FET

At present, achieving E-mode lateral β-Ga_2O_3 MOSFETs is still challenging. The main problem is that the gate control of lateral β-Ga_2O_3 MOSFETs is not strong enough to fully deplete the channel under the gate at zero gate voltage bias. In this section, the research to overcome such difficulty was classified into three main directions. Firstly, reducing the width of the channel can make it more easily to be depleted, hence realizing the E-mode. Secondly, an easily depleted channel can also be achieved by adjusting the doping distribution in the MOSFETs channel layer. Finally, several kinds of material that present strong gate control ability can also be chosen to replace the traditional gate material.

2.1. Metalorganic chemical vapor deposition of Ga_2O_3

The drift layer in lateral β-Ga_2O_3 FETs is rather critical for device performance. Thanks to the relatively costless native substrates, the good quality drift layer can be grown via homoepitaxial methods such as MOCVD, MBE, HVPE, LPCVD, etc. Among all these technologies, MOCVD is considered as the suitable method for the industrial production of β-Ga_2O_3 devices because of its superiority in epitaxial growth, while there are still some unsolved problems in other methods. For example, the MBE method cannot control the n-type doping concentration at a low value, and the precise control of epitaxial thickness in the nanometer range is still difficult for HVPE and LPCVD[33]. In this section, we will introduce some details about the MOCVD epitaxial method and briefly review the research and development of homoepitaxial growing β-Ga_2O_3.

MOCVD is a vapor phase growing method with Ar or N_2 as the carrier gas transporting the precursors such as metalorganics and oxygen in the reaction chamber. In the epitaxy of β-Ga_2O_3, TMGa[34] (or TEGa[35]), and oxygen are usually selected as the metalorganic precursor and oxide precursor, respectively. After entering the chamber, the metalorganic and oxide precursors are absorbed on the substrate and start to react with each other. The epitaxial layer is formed in this

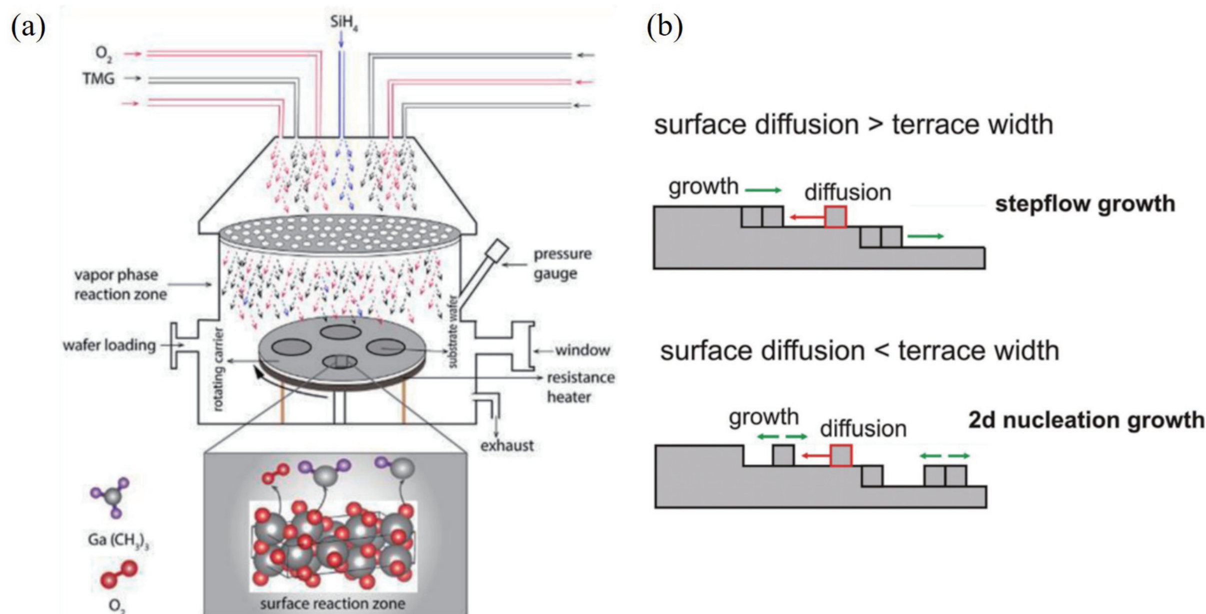

Fig. 2. (Color online) (a) The schematic of the showerhead MOCVD reaction chamber. © 2021 Elsevier B.V. Reprinted with permission from Ref. [34]. (b) The schematic diagram showing the mechanism of step-flow growth and two-dimensional nucleation growth. © 2019 American Institute of Physics. Reprinted with permission from Ref. [37].

process, as well as the by-products. The by-products are swept by the carrier gas and carried to the exhaust. The schematic diagram of the β-Ga_2O_3 epitaxy via the close coupled showerhead MOCVD technique is shown in Fig. 2(a)[36]. Such a technique is more suitable for industrial production, and the horizontal type is more commonly used in scientific research.

The epitaxial rate and quality are affected by several parameters. Firstly, the selection of gallium sources should be considered carefully. Fikadu *et al*. studied the effects of different gallium precursors on epitaxial rate, including $Ga(DPM)_3$, TMGa, and TEGa[37]. It is found that TMGa has the highest growth rate due to its high decomposition temperature. But the TMGa can introduce carbon that is considered as the donor-type impurities, possibly degrading device electronic performance. Hence, the high-quality β-Ga_2O_3 layers now are mainly fabricated via TEGa[9]. But Seryogin *et al*. later proved that high-quality β-Ga_2O_3 layers could also be obtained using TMGa[34]. In their study, a record low-temperature electron mobility exceeding 23 000 $cm^2/(V\cdot s)$ at 32 K has been achieved. Seryogin *et al*. also mentioned that unexpected impurities can be diminished via growth condition modulation. By changing the O_2/TMGa ratio from 230 to 530, the value of carbon concentration dropped below the instrument detection limit, and the RT Hall mobility of 113 $cm^2/(V\cdot s)$ at $n = 1 \times 10^{17}$ cm^{-3} was recoveried from the resistive condition.

Secondly, for better epitaxial growth of β-Ga_2O_3, the native substrates usually have a small miscut angle for step flow growth mode. But to be honest, the step flow growth won't be achieved without the careful optimization of growth parameters. Anooz *et al*. studied the transition between different growth modes and gave guidance about how to adjust the growth condition[38]. Fig. 2(b) shows a schematic diagram of two growth modes[39]. The relation between the source diffusion length and terrace width determines the morphology of the layer. The step flow growth only occurs when the diffusion length is comparable to the terrace length, and a step-bunching growth will appear when the diffusion length is much larger than the terrace length. It is obvious that the terrace length is getting longer as the miscut angle increasing, and the diffusion length can be changed as the change of chamber pressure and gallium flux. By adjusting the growth condition, the balance between terrace length and diffusion length will finally be found, and then the growth of β-Ga_2O_3 will follow the step flow mode.

Thirdly, the n-type conductivity of β-Ga_2O_3 can be realized via Si^+ doping. However, the tradeoff between doping concentration and carrier mobility still needs further study. The discrepancy between the carrier density and doping concentration indicates the existence of compensating defects and impurities. For precisely measuring the β-Ga_2O_3 crystal quality, the low-temperature hall mobility can be applied, and the measurement result is shown in Fig. 3(a)[33]. A peak mobility of 4984 $cm^2/(V\cdot s)$ was achieved at a temperature of 45 K, indicating the low concentration of scattering centers. Meanwhile, three different donor energy levels can also be studied via the dependence of Hall charge density on the reciprocal of temperature (1000/T) obtained from this Hall measurement. The one with the lowest energy belongs to Si, while the origin of other donor levels has not been fully understood yet. Fig. 3(b) is a SIMS depth profile of impurities in MOCVD grown (010) β-Ga_2O_3 homoepitaxial thin film[33]. The carbon impurity comes from the TMGa, and the origin of Fe is the diffusion of Fe-doped substrate. The impurity concentration in the bulk area is below the detecting limit, proving the good quality of MOCVD growth layer even with Si^+ doping.

2.2. E-mode via channel reshaping

E-mode lateral Ga_2O_3 MOSFETs via channel reshaping was first achieved by Chabak *et al*.[40]. They fabricated a wrap-gate fin field-effect transistors on native (100) β-Ga_2O_3 substrate. Fig. 4(a) shows the fabrication process of the wrap-gate FinFETs. Firstly, a double layer Cr hard mask was deposited by electron beam lithography. The inductively coupled plasma (ICP) etching process was employed afte-

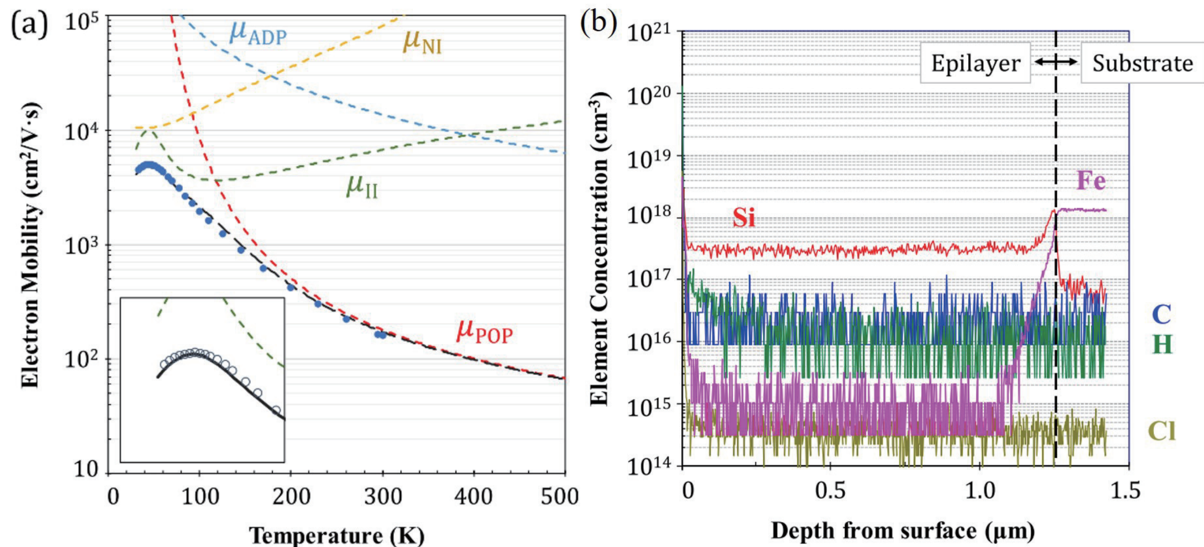

Fig. 3. (Color online) (a) Temperature dependence of carrier mobility tested in low-temperature hall measurement. (b) SIMS depth distribution of impurities in MOCVD grown β-Ga_2O_3 epitaxial layer on (010) substrate. © 2019 American Institute of Physics. Reprinted with permission from Ref. [31].

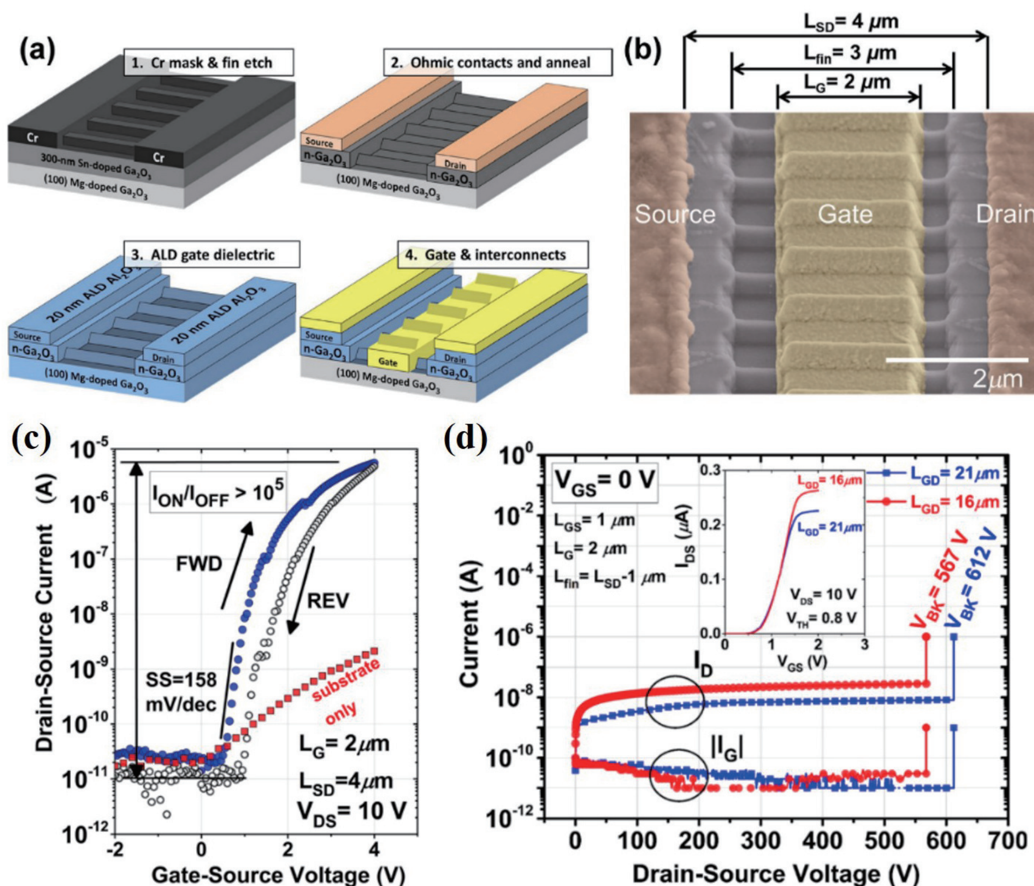

Fig. 4. (Color online) (a) Fabrication process and (b) the geometry structure false-colored SEM image of FinFET with an L_{SD} = 4. (c) The transfer characteristics in the form of log(I_D)–V_G with the forward and reverse sweeps. (d) The breakdown characteristics of β-Ga_2O_3 FinFETs with L_{GD} of 16 and 21 μm measured at V_{GS} = 0 V. © 2016 Chabak *et al*. Reprinted with permission from Ref. [40].

rward[41]. In this process, the Cr hard mask and the β-Ga_2O_3 layer were etched simultaneously in the ratio of 1 : 2, forming the fin gate structure and the bulk mesa contacts for source and drain electrodes. The triangle shape of the fin structure with a width of 300 nm at the bottom and a height of 200 nm was formed by over-etching, through which the Cr hard mask between fins was totally removed. Ohmic contacts were achieved by depositing Ti/Al/Ni/Au (20/100/50/50 nm) followed by rapid annealing process for 1 min at 470 °C in nitrogen. The 20 nm Al_2O_3 and the Ni/Au (20/480 nm) were used as the gate dielectric and gate metal, respectively. Fig. 4(c) shows the transfer characteristic of this device at

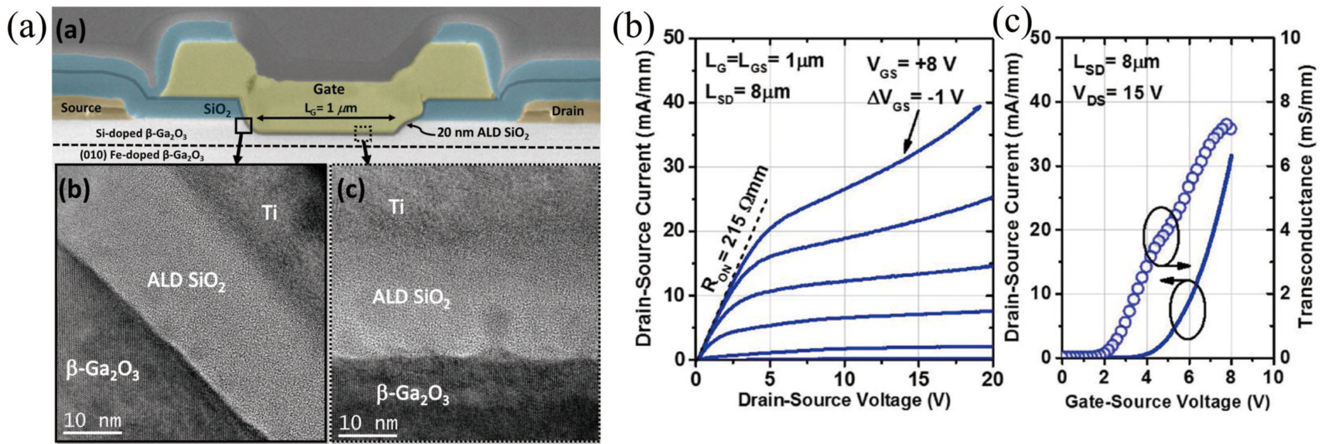

Fig. 5. (Color online) (a) The false-colored SEM view of a recessed gate device with the L_{SD} = 3 μm device. The HR-TEM picture below shows the facet morphology of sidewall and bottom in the gate-recess contact and gate metal interfaces. (b) The output characteristics for an L_{SD} = 8 μm device at the gate bias of 8 V. (c) Linear transfer characteristics at V_{DS} = 15 V. © 2017 IEEE. Reprinted with permission from Ref. [29].

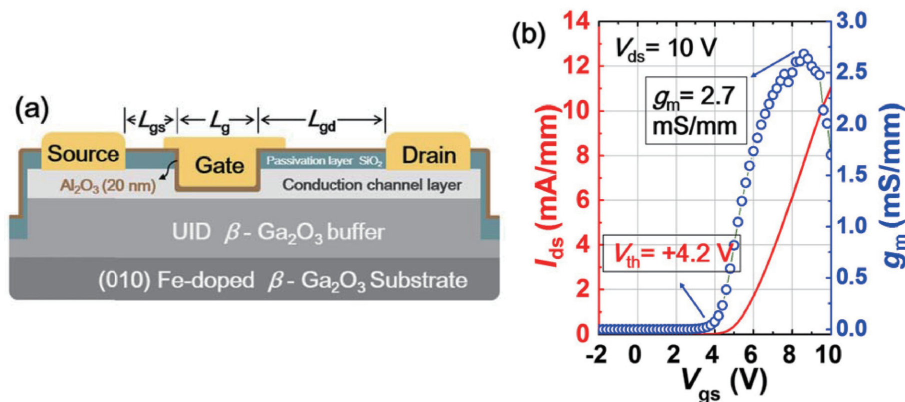

Fig. 6. (Color online) (a) Schematic diagram of the enhancement-mode MOSFET. (b) Linear transfer characteristics (I_{DS}–V_{GS}) of the fabricated trench gate MOSFET measured at V_{DS} = 10 V. © 2019 IEEE. Reprinted with permission from Ref. [42].

V_{DS} = 10 V. An obvious enhancement mode with a threshold voltage of 1 V can be extracted in this curve, proving that the thin fin-shaped channels are easily depleted. Besides the E-mode, the relatively high breakdown voltage of 600 V is also realized, as shown in Fig. 4(d).

However, such wrap-gate FinFET is too complicated, which causes difficulties in repeatability and stability in the fabrication process. The absence of further study also verifies the lack of research value. Chabak *et al*. fabricated the first recessed-gate E-mode β-Ga_2O_3 MOSFETs, which is much more simple in structure than the wrap-gate design[29]. Fig. 5(a) shows the SEM false-colored cross-sectional view of this recessed-gate device. The initial channel with width of 200 nm was ICP etched to 60 nm at the gate region while the rest remained at 200 nm, minimizing the on-resistance. An evaporated Ti/Al/Ni/Au metal and Ti/Au metal were used as the ohmic contact and the gate metal, respectively. Obviously, the simplified etching process will lead to fewer defects and interface states, therefore reducing the threshold voltage offset and the sub-threshold swing. Figs. 5(b) and 5(c) present the output and transfer characteristics of recessed-gate MOSFETs. The transfer characteristics measured at V_{DS} = 15 V clearly shows the positive threshold voltage of around 4 V. From the curve of output characteristics, the R_{ON} = 215 Ω·mm can be extracted. Such relatively high on-resistance point out the shortcoming of decreased channel width. Dong *et al*. also fabricated a similar E-mode recessed-gate MOSFETs, and the cross-section view is shown in Fig. 6(a)[42]. The even higher on-resistance of 364 Ω·mm measured in this study increases the concern about the application prospect of recessed-gate structure. It has to be mentioned that the recessed-gate structure without E-mode was first reported by Green *et al*.[43], and the power gain measurement of RF operation is the initial purpose of this device. With the thinner channel width, recessed-gate β-Ga_2O_3 MOSFET can perform a high switching speed, which is suitable for RF operation. The on-resistance, as one of the crucial parameters of power devices, was not considered the key point at the beginning of the design. Recently, Huy-Binh Do *et al*. have offered a solution to this resistance problem in recessed-gate structure via TCAD simulation study[44]. The HfO_2 gate dielectric and gate-connected field plate were used to optimize the device performance. A relatively low on-resistance of 92.1 Ω·mm was observed through the simulation process, while the device is still working in the E-mode. Such results benefited from the high permittivity of HfO_2[45], resulting in more flexible control of the semiconductor Fermi-level. Besides, the breakdown voltage was increased to 1573 V after the fabrication of the field plate. However, this design is still in the simulation state yet. Further experiments of fabrication and testing are needed to prove the feasibility of the recessed-gate β-Ga_2O_3 MOSFET.

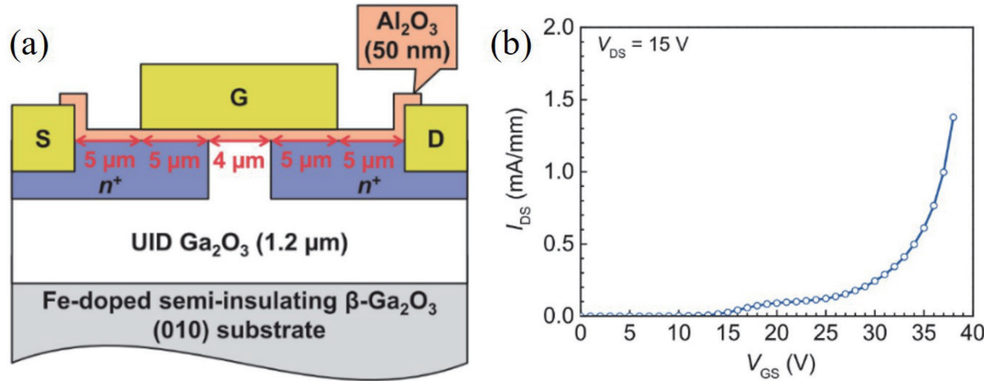

Fig. 7. (Color online) (a) Cross section view of the E-mode MOSFETs with the UID channel layer and Si+-implanted source (drain) contacts. (b) Linear transfer characteristics at V_{DS} = 15 V. © 2017 The Japan Society of Applied Physics. Reprinted with permission from Ref. [47].

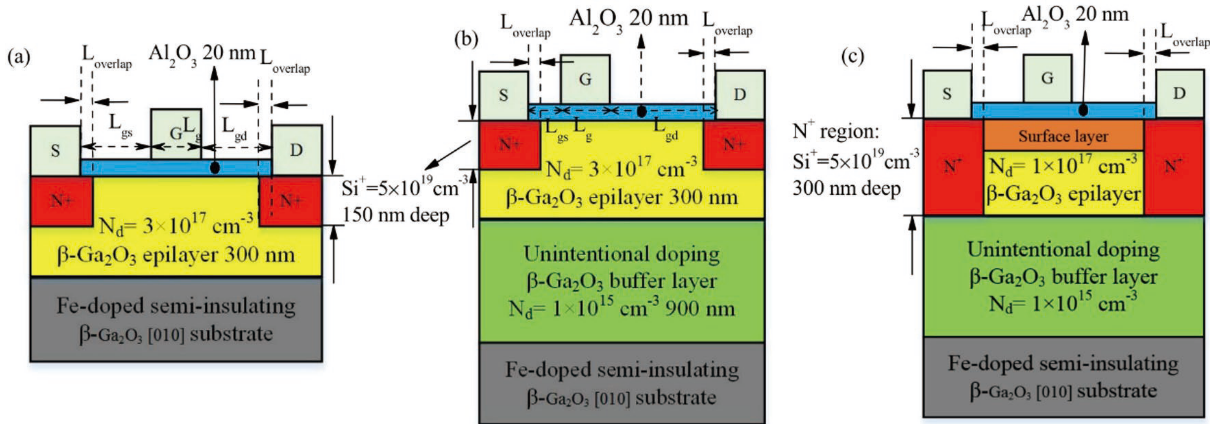

Fig. 8. (Color online) Schematic diagram of lateral Ga_2O_3 MOSFET structures (a) without and (b) with UID buffer layer. (c) The novel triple layer design of lateral MOSFET structure. © 2021 IEEE. Reprinted with permission from Ref. [47].

2.3. E-mode via channel doping modulation

The doping process during epitaxial techniques is the critical step toward fabricating a conducting channel layer. By significantly increasing the carrier concentration, the on-state currents can be maintained at a proper value. However, high carrier concentration makes the gate control difficult to deplete the channel, which hinders the realization of E-mode lateral β-Ga_2O_3 FETs. Hence, simply decreasing the carrier concentration in the channel might be helpful in achieving E-mode. Wong *et al*. fabricated unintentionally doped (UID) channel MOSFETs[46]. Fig. 7(a) shows the cross-section view of this UID channel MOSFETs, and the device transfer characteristic is shown in Fig. 7(b). Due to the low carrier concentration in the UID channel layer, the channel layer was easily depleted even with the relatively high thickness of 1.2 μm. Another advantage of this design is the reduced process complexity compared to other E-mode structure. Kamimura *et al*. also fabricated similar UID channel MOSFETs via MBE[31]. The channel layer that was unintentionally doped by N and Si impurities in the epitaxial process can act as a p-type material to form the E-mode MOSFETs, even if the source of these impurities remained unclear. However, the UID carrier concentration in these devices is far below the level that could provide acceptable threshold voltages and on-resistance. Therefore, the design of the channel doping needs to be further optimized to realize better performance.

Recently, Guo *et al*. studied the muti-layer doping distribution in the MOSFETs channel via the TCAD simulation[47]. As shown in Fig. 8, a surface layer was formed at the top of the Si-doped channel layer. On the one hand, the total carrier quantity has been reduced compared to the traditional channel layer, making it easier to be depleted. On the other hand, the carrier concentration in the channel beneath the surface layer remained at a high doping level. By adjusting the surface layer thickness, a trade-off between threshold voltage and device performance can be achieved. Besides, the electric field crowding at the corner of the gate could also be relaxed due to the introduction of the surface layer.

Another doping optimization design was carried out by Zhou *et al*.[48]. The variation of lateral doping (VLD) technique was studied via TCAD simulation method. As shown in Fig. 9(b), the doping concentration varies with four regions in the order of magnitudes from the gate to the drain. Such doping distribution meets both requirements of device reliability and performance. The low channel doping concentration of 10^{16} cm^{-3} near the gate not only formed an easily depleted region at zero gate voltage bias but also protected the device from early breakdown caused by the electric field crowding. As the distance to the gate region increased, the demand for device protection became less important, while the on-resistance needed to be limited in these regions. Therefore, the doping concentration becomes higher and higher to boost the carrier quantity. The result of the simulation is shown in Figs. 9(c) and 9(d). The VLD lateral device and the one with a doping concentration of 10^{16} cm^{-3} were the only

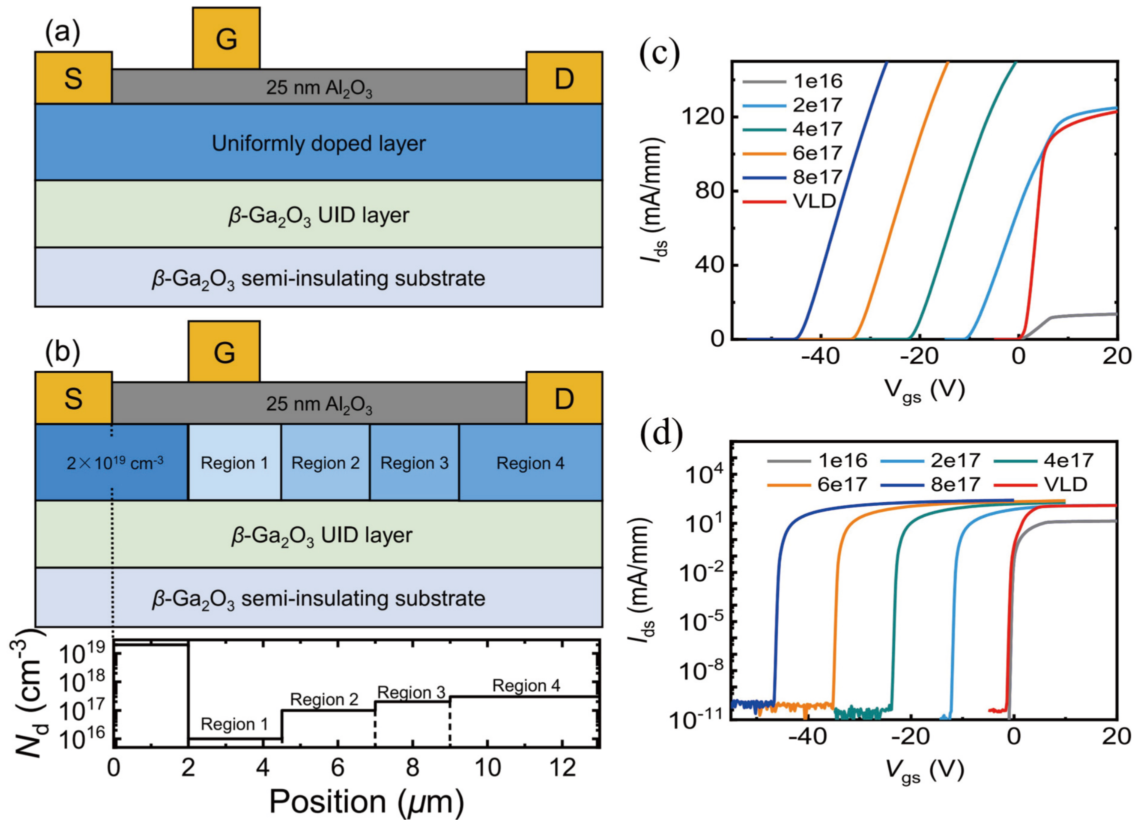

Fig. 9. (Color online) Cross section view of the FET with (a) UD layer and (b) VLD layer. The (c) linear and (d) semi-logarithmic scale of transfer characteristics extracted from the simulation. © 2021 IEEE. Reprinted with permission from Ref. [48].

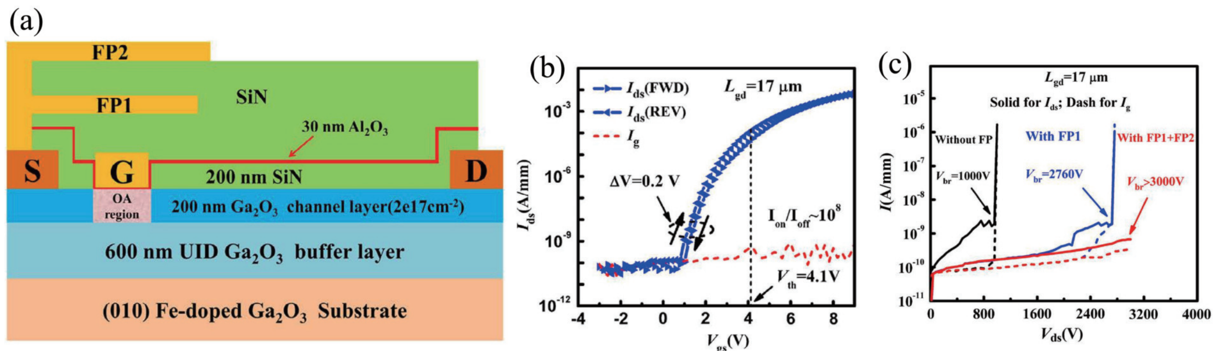

Fig. 10. (Color online) (a) Schematic diagram of the OA β-Ga_2O_3 MOSFET with L_{gd} = 17 μm. (b) Log-scale transfer characteristics of the device. (c) The breakdown characteristics of the OA Ga_2O_3 MOSFET without source field plate, with single SFP and with double SFP. © 2019 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim. Reprinted with permission from Ref. [50].

two that performed the E-mode among all these references. Considering the output characteristic, the device with the lowest doping concentration showed an extremely high R_{on}, while the VLD lateral device had a moderate R_{on} of 104.1 Ω·mm, which is close to the value of the uniform doping (UD) transistor with doping of 10^{17} cm^{-3}. The breakdown voltage of UD and VLD transistors was simulated to be 1161 and 1832 V, respectively. Although all these excellent parameters above proved the success of the VLD design, such a complicated structure certainly will cause lots of problems in the fabrication process. Stengl *et al*. achieved this VLD via the implantation method in the silicon material[49]. A series of small holes with laterally decreasing diameter were used to realize the variation of carrier concentration. It is also pointed out that a VLD structure can also be realized via the diffusion of gas or liquid dopant source.

Except for modulating the doping concentration, Lv *et al*. found another way to adjust the carrier concentration in β-Ga_2O_3. The schematic cross section of the E-mode transistor fabricated by Lv *et al*. is presented in Fig. 10(a)[50]. The channel region under the gate was treated via oxygen annealing (OA) process after the epitaxial growth. Before depositing the gate metal, the structure with only the source and drain contacts was tested to confirm the electrical mechanism of OA. The extremely high on-resistance of 739 Ω·mm was extracted at low drain bias with the L_{gd} of 17 μm. This phenomenon could be explained that the oxygen vacancies were filled or the donor impurities were oxidized in the OA process. After the test, the gate metal was deposited to form the MOSFET structure, and the SiN passivation layer was formed afterward to support two source-connected field plates. The transform characteristic presented in Fig. 10(b) proves the E-

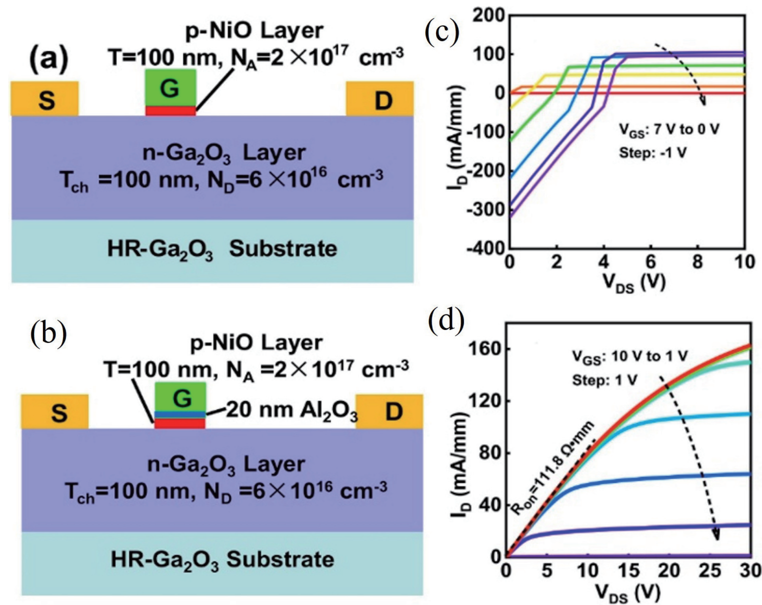

Fig. 11. (Color online) Cross-sectional view of the E-mode HJ-FET (a) without the Al_2O_3 layer and (b) with the Al_2O_3 layer. The linear-scale transfer characteristics for the E-mode HJ-FET (c) without the Al_2O_3 layer and (d) with the Al_2O_3 layer. © 2022 IEEE. Reprinted with permission from Ref. [55].

mode of this OA lateral MOSFET, but also points out that the saturation current of this device is not high enough. Besides, excellent breakdown characteristics of this device were also realized on account of the field plate structure, as shown in Fig. 10(c). On the whole, even though the OA treated MOSFET didn't reach the ideal performance, finding the proper treatment method is still worth trying in the fabrication of lateral E-mode β-Ga_2O_3 FETs.

2.4. E-mode via novel gate material

Due to the lack of p-type doping in β-Ga_2O_3, using alternative p-type materials to form heterojunctions might be a possible solution to form E-mode. Recently, the heterojunction of p-type NiO_x and β-Ga_2O_3 has drawn lots of interest due to its successful realization of p–n junction. The NiO_x forming by sputtering and thermal oxidation of Ni owns intrinsic p-type conductivity due to the nickel defects and impurities naturally forming in the amorphous structure[51]. Lu *et al*. fabricated the first kilovolt-class NiO/β-Ga_2O_3 heterojunction diodes (HJD)[52], and several remarkable achievements were achieved later[53]. The first β-Ga_2O_3 HJ-FET using NiO as the gate dielectric was fabricated by Wang *et al*.[54]. The structure in this study was designed to meet the requirement of testing the MOSFET and diode performance at a single device. In this research, two different channel widths of 200 and 600 nm were applied in the fabrication of HJ-FETs structure, but neither of them performed the E-mode as expected. Obviously, the gate control is not strong enough at this channel width even with HJ structure. Later, Lei *et al*. also studied the E-mode β-Ga_2O_3 FETs on the combination of NiO/β-Ga_2O_3 heterojunction via TCAD simulation[55]. The device with a channel width of 600 nm was first tested to be depletion mode (D-mode) as expected. The channel width of 100 nm was then simulated, and the E-mode was almost achieved. However, a severe leakage current at low drain voltage bias was shown in the output characteristic (Fig. 11 (b)). The condition comes from the parasitic HJD between the gate and drain. When the gate voltage exceeds the drain voltage, the HJD will be turned on and will cause the severe leakage current. Hence, a Al_2O_3 layer with the thickness of 20 nm was then added between the gate metal and dielectric for blocking the leakage current, as shown in Fig. 11(c). The absence of reverse leakage current in the output characteristic (Fig. 11(d)) demonstrates the successful control of parasitic HJD. Moreover, a more significant E-mode was achieved in this structure compared to the previous one without the blocking layer. This parasitic HJD was not considered in the previous study of heterojunction FETs, and it has to be taken into account in the future design. Recently, the real fabrication of E-mode β-Ga_2O_3 HJ-FETs was achieved by Zhou *et al*.[32]. As shown in Fig. 12(a), this E-mode was realized via the combination of p-type NiO and recessed-gate structure. It seems that the E-mode lateral Ga_2O_3 FETs can't be realized only by the NiO gate dielectric without sacrificing the on-resistance of the device. After the epitaxially growing 200 nm thick β-Ga_2O_3 channel layer, the low RF power ICP etching method was used to form the 120 nm gate trench. Therefore, the channel width under the gate was only 80 nm. The heavily doped source and drain regions were formed by MOCVD selectively regrown using SiO_2 as a hard mask. The positive threshold voltage of 0.9 V can be extracted from the transfer characteristic shown in Fig. 12(b). An on-resistance of 151.5 Ω·mm and a saturation current of 10.8 mA/mm can be extracted from the linear region and saturation region of output characteristic, respectively. Even though the ideal device performance was not achieved, further study of the combination among various design of E-mode β-Ga_2O_3 FETs is worthwhile.

Except for the p-type NiO, Feng *et al*. fabricated the E-mode β-Ga_2O_3 via the laminated-ferroelectric (L-FeG) charge storage gate[30]. Fig. 13(a) depicts the schematic diagram of the L-FeG E-mode FETs. The 200 nm Sn-doped β-Ga_2O_3 channel layer was deposited on the Fe-doped (010) homogeneous substrate. The source and drain region were etched for about 20 nm via the ICP method to achieve a lower Ohmic contact resistance. The laminated-ferroelectric was then formed

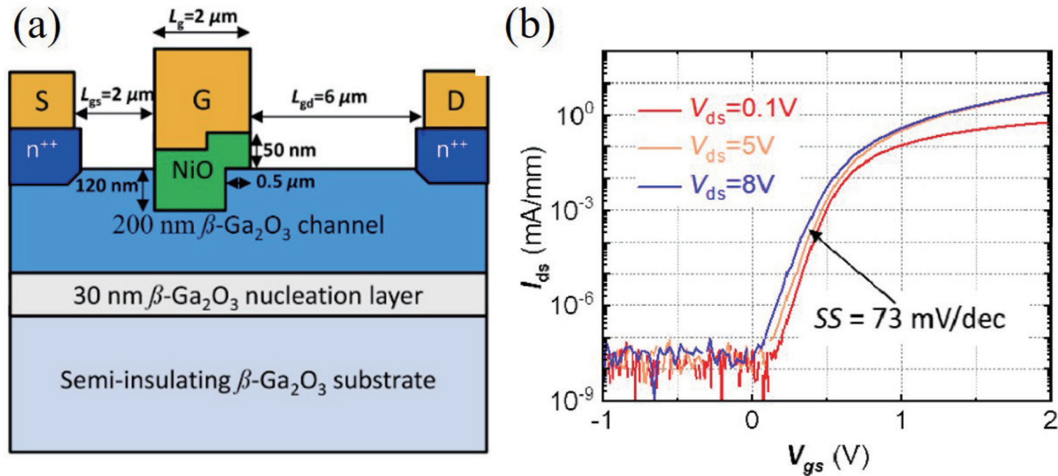

Fig. 12. (Color online) (a) Cross-section view of the gate-recessed HJ-FET. (b) Log-scale I_{DS}–V_{GS} curves of the gate-recessed HJ-FET at V_{DS} of 0.1, 5, and 8 V. © 2022 IEEE. Reprinted with permission from Ref. [30].

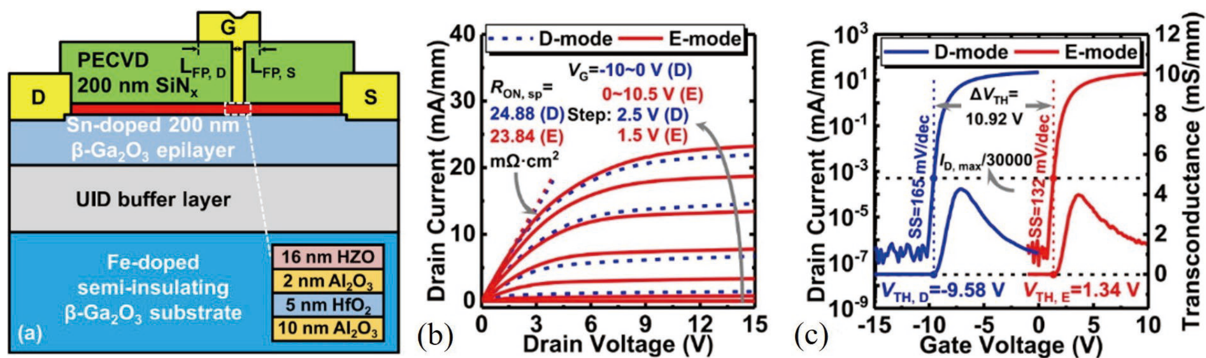

Fig. 13. (Color online) (a) Schematic diagram of L-FeG Ga_2O_3 MOSFET. (b) Linear-scale I_{DS}–V_{DS} and (c) I_{DS}–V_{GS} curves of the D- and E-mode L-FeG Ga_2O_3 MOSFET with an L_{SD} = 11.4 μm © 2020 Feng *et al*. Reprinted with permission from Ref. [30].

by plasma-enhanced atomic layer deposition (PEALD), which specific layered structure can be seen in the inset of Fig. 13(a). The Al_2O_3 here served as a charge tunneling layer and interlayer, covering the HfO_2 as the charge storage layer. The key unit of this muti-layer structure was the ferroelectric HZO. This L-FeG actually acted as the D-mode when it was first fabricated. Then, a 1 ms pulse bias of 18 V was given to the gate electrode. This gate pulse forced the HZO to build a strong polarization, hence drawing electrons through the charge tunneling layer and trapping them in the charge storage layer. These trapping electrons together with the gate electrode could offer the gate control ability strong enough to fully deplete the channel layer below. Fig. 13(c) shows the comparison of transfer characteristics between E-mode and D-mode. The threshold voltage changed from −9.85 to 1.34 V, proving the transformation from D-mode to E-mode. The low on-resistance of 23.84 Ω·mm can be extracted from Fig. 13(b), further affirming the superiority of the device. The only problem might be the complicated fabrication process and the instability of device performance. Even though Feng *et al.* have proved that the threshold voltage shifting was negligible, the structure complexity still calls out the concern about the real application.

3. Vertical β-Ga_2O_3 FET

3.1. Hydride vapor phase epitaxy of β-Ga_2O_3

Before the review of vertical β-Ga_2O_3 devices, it is also necessary to give a brief introduction about the epitaxial method. Being different from the lateral devices, vertical FETs were usually fabricated via the HVPE technique because of their less requirement for the thickness control[2]. The pure metal Ga was first reacted with HCl at the temperature of 850 °C to form GaCl in the upstream region. In the epitaxial growth of β-Ga_2O_3, the GaCl was then transported to the downstream region along with O_2 by the carrier gas. These Ga source and oxygen were finally started to react with each other on the β-Ga_2O_3 native substrate which has been heated to a temperature between 800 and 1050 °C[56]. The main advantage of the HVPE method is its high growth rate over 10 μm/h in the β-Ga_2O_3 epitaxial growth, which makes it the common choice for the commercial production of β-Ga_2O_3 material. However, defects such as surface pits are formed in this fast growth process. Hence, extra procedures like chemical mechanical polishing (CMP) are particularly important for the HVPE technique to form a pristine surface. Besides, compared to other method, using the HVPE method can significantly decrease the background electron density in the β-Ga_2O_3 epitaxial layer to the level below 10^{13} cm^{-3}, further guaranteeing the subsequent device performance.

3.2. CAVETs and CBL structure

To be honest, the inspiration of vertical β-Ga_2O_3 FETs is another imitation of previous successful design realized by other semi-conductor material. Wong *et al*. built the first vertical β-Ga_2O_3 FETs using a current blocking layer (CBL) struc-

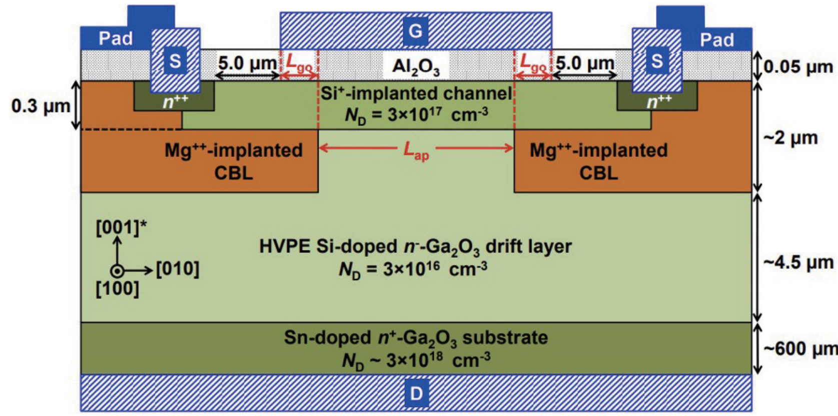

Fig. 14. (Color online) Cross-sectional view of the current aperture vertical Ga_2O_3. © 2018 IEEE. Reprinted with permission from Ref. [57].

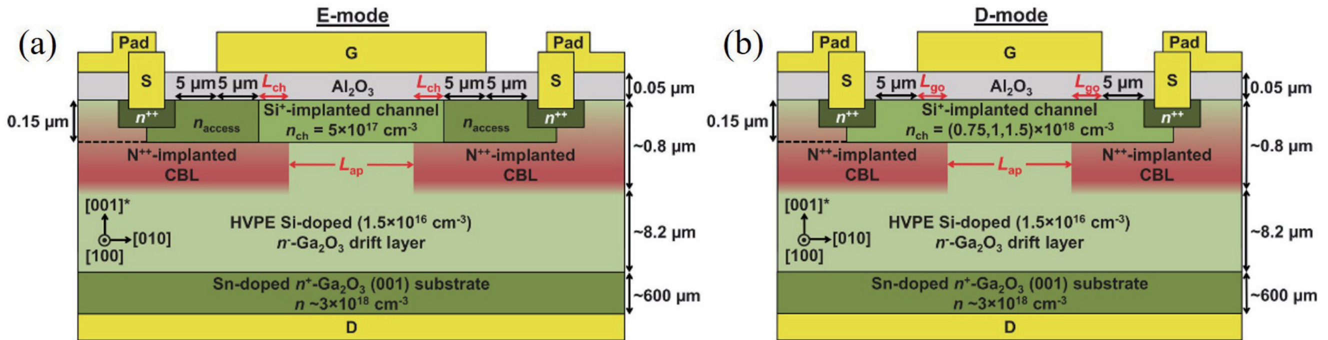

Fig. 15. (Color online) Schematics of (a) E-mode and (b) D-mode current aperture vertical Ga_2O_3 MOSFETs. © 2019 IEEE. Reprinted with permission from Ref. [58].

ture[57] which directly followed the similar design of GaN current aperture vertical electron transistors (CAVETs)[26] and SiC double-implanted MOSFETs[27]. Fig. 14 shows the cross-sectional schematic of the β-Ga_2O_3 CAVETs. The fabrication process began with the HVPE growth of the 10 μm thick Si-doped β-Ga_2O_3 drift layer on the (001) native Sn-doped substrate. Both sides of this chip were then planarized by CMP to further improve the subsequent contact quality. After that, the Mg^{++} was implanted to the layer at the energy around 560 keV to form the CBL with an aperture at the central of it, and the defects caused by this process was partially recovered through 30 min N_2 thermal annealing at 1000 °C. Subsequently, the channel region of 150 nm thick was defined by Si ion implantation. The gate dielectric and several electrodes were finally deposited after activating the dopants. Even the peak transconductance of 1.25 mS/mm and the minus threshold voltage of −34 V measured at a drain bias of 8 V showed the immaturity of this design, it was still a good start for the vertical β-Ga_2O_3 FETs. The further optimization of this design was also achieved by Wong *et al*. in 2018. They used N^{++} instead of Mg^{++} to form the CBL because the better blocking ability of N^{++} was proved by the experiment, and the peak transconductance was successfully increased to 4.7 mS/mm.

The first attempt of E-mode CAVET was still studied by Wong *et al*.[58]. Figs. 15(a) and 15(b) here show a comparison between the E-mode and D-mode CAVET. It is obvious that the key point of this E-mode design is the decrease of channel doping concentration (n_{ch}). But even the highly doped access region was enlarged in this E-mode CAVET to improve the conducting characteristic, the I_D of this E-mode CAVET could only reach the 1/10 of the D-mode one (n_{ch} = 1 × 10^{18} cm^{-3}). Considering the complexity of this structure, it is pretty doubtful for this design to become applicable.

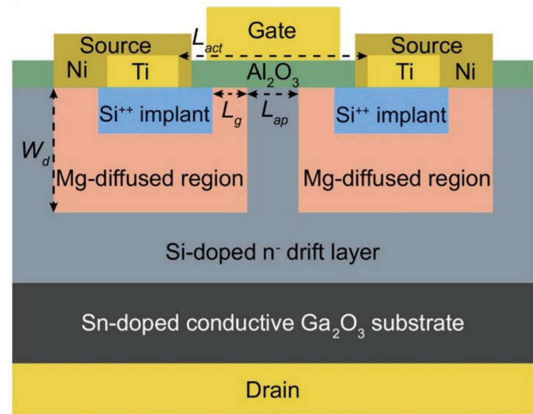

Fig. 16. (Color online) Cross-section schematic of the fabricated VDBFET. © 2022 IEEE. Reprinted with permission from Ref. [59].

However, researchers have already come up with kinds of ideas using CBL to realize E-mode β-Ga_2O_3 FET. In 2022, Zeng *et al*. developed the diffusion doping process to form the CBL[59]. The Mg was deposited on the surface by the spin-on-glass technique, followed by furnace thermal to accomplish the diffusion. Such a doping method won't produce much crystal damage like ion implantation, which means the needlessness of the annealing process. Based on this technique, Zeng *et al*. fabricated the first β-Ga_2O_3 vertical diffused barrier field-effect-transistor (VDBFET), and its schematic is shown in Fig. 16. Since the source regions were

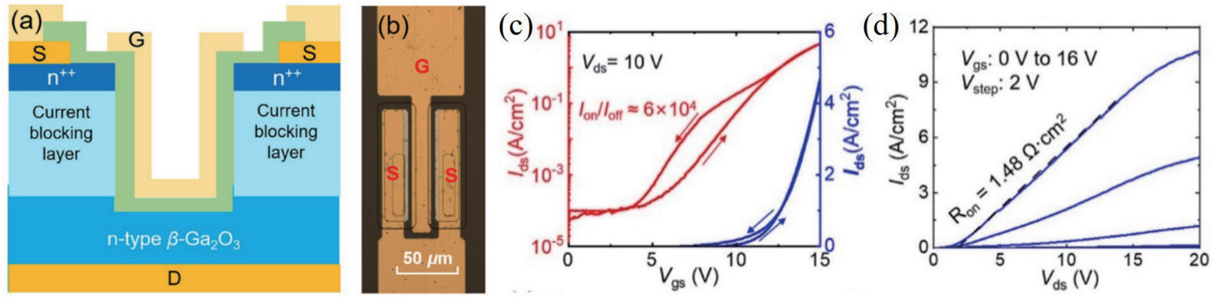

Fig. 17. (Color online) (a) Cross sections view and (b) optical micrograph of a Ga_2O_3 UMOSFET with CBL realized by oxygen annealing. (c) Transfer and (d) output characteristics of Ga_2O_3 UMOSFET © 2022 Zhou et al. Reprinted with permission from Ref. [60].

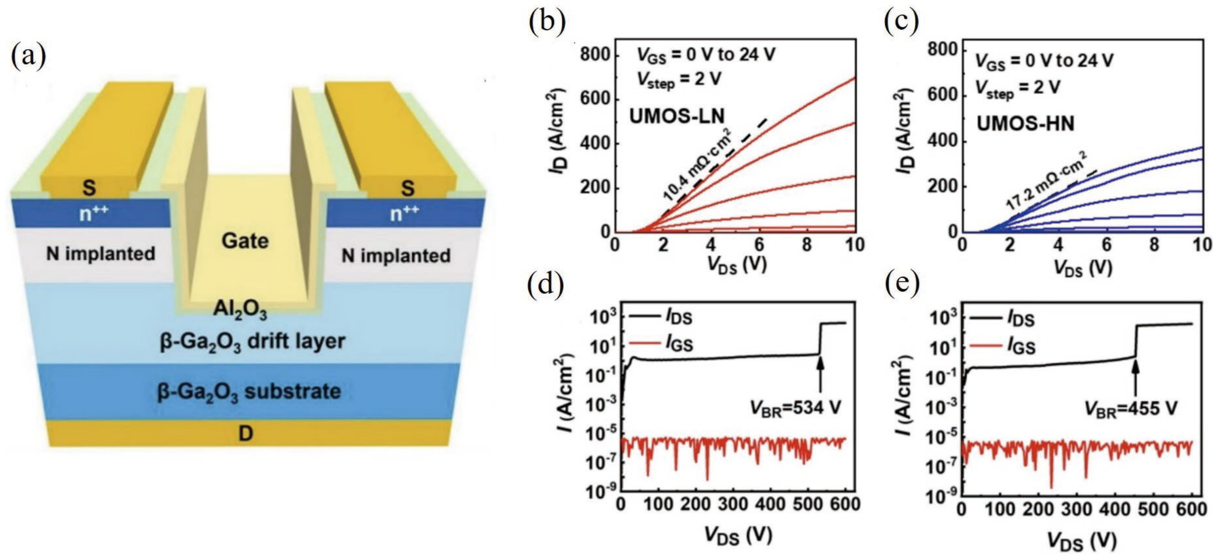

Fig. 18. (Color online) (a) Schematic view of Ga_2O_3 UMOSFET with CBL realized by N^+ implantation. Output characteristics of (b) UMOS-LN and (c) UMOS-HN. Three terminal breakdown characteristics of (d) UMOS-LN and (e) UMOS-HN. © 2023 IEEE. Reprinted with permission from Ref. [61].

totally covered by the Mg-diffused region, the VDBFET would stay at off-state without voltage bias. When applying the positive gate voltage bias, a near-box profile will be accumulated at the interface between Mg-diffused region and Al_2O_3, forcing the device to turn on. Thus, a natural normally-off FET was achieved with the help of CBL.

Following similar principles as Zeng *et al*., Ma *et al*. and Zhou *et al*. constructed the E-mode β-Ga_2O_3 U-Shape trench gate MOSFET (U-MOSFET). The schematic view of the UMOSFET fabricated by Zhou *et al*. is shown in Fig. 17(a)[60]. The CBL here was realized via oxygen annealing at 1200 °C for 6 h. The top access region with the thickness of 100 nm was then defined by the Si ion implantation. After activating the dopants, they used the ICP etching process to accomplish the trench shape along with the mesa isolation. The gate dielectric and electrode were finally deposited and patterned in the trench region. The charge accumulation layer would form at the side interface between CBL and gate dielectric when the positive gate voltage was applied. The E-mode was proved through measurement with the threshold voltage of 11.5 V, and the $R_{on,sp}$ of 1.48 Ω·cm^2 was also extracted, as shown in Figs. 17(c) and 17(d). However, the breakdown characteristic was dissatisfactory, which might come from the immaturity of the oxygen annealing technique. In the study by Ma *et al*., the similar device was fabricated but via a different method[61]. The layers here were formed by high dose of N^+ implantation at the energy of 380 keV. Two types of devices with different N^+ concentration level of 5 × 10^{18} and 1 × 10^{19} cm^{-3} were tested in this experiment, denoted as UMOS-LN and UMOS-HN, respectively. The testing results showed in Figs. 18(c) and 18(d) present a higher $R_{on,sp}$, but the obvious promotion of high voltage tolerance still proves the feasibility of this design. In short, further study on the fabrication of CBL is needed to find the proper method.

3.3. FinFETs

Even though the CAVETs were the first fabricated vertical β-Ga_2O_3 FET, the first achievement of vertical E-mode Ga_2O_3 FET was the FinFET structure fabricated by Hu *et al.*[62]. This study was just next to their first success of fabricating β-Ga_2O_3 FinFET. Fig. 19(a) here presents the schematic structure of this device. The top 50 nm of β-Ga_2O_3 FinFET was doped with Si for the convenience of Ohmic contact. In the procedure of forming the fin shaped structure, Pt metal was patterned serving as the hard etching mask, and the chips was then etched to fin-channels with the height/width of 1.0/0.3 μm. The Al_2O_3 and Cr was deposited as the gate dielectric and electrode in the trench, respectively, while the part on the top of the fin was etched away. A 200 nm SiO_2 was deposited and patterned before the final depositing of source electrode in order to isolate the gate metal and source metal. The clear E-mode with the threshold voltage of 2.2 V can be seen in the testing results shown in Fig. 19(b). The $R_{on,sp}$ of 18 mΩ·cm^2 and the breakdown voltage of 1057 V

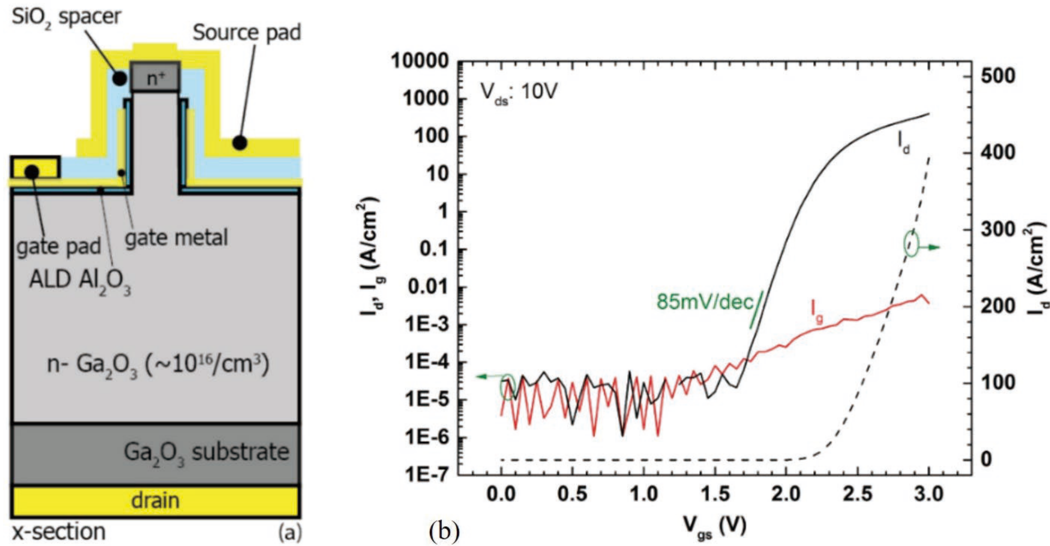

Fig. 19. (Color online) (a) Cross sections view and (b) output characteristics of a Ga_2O_3 FinFET. © 2018 IEEE. Reprinted with permission from Ref. [62].

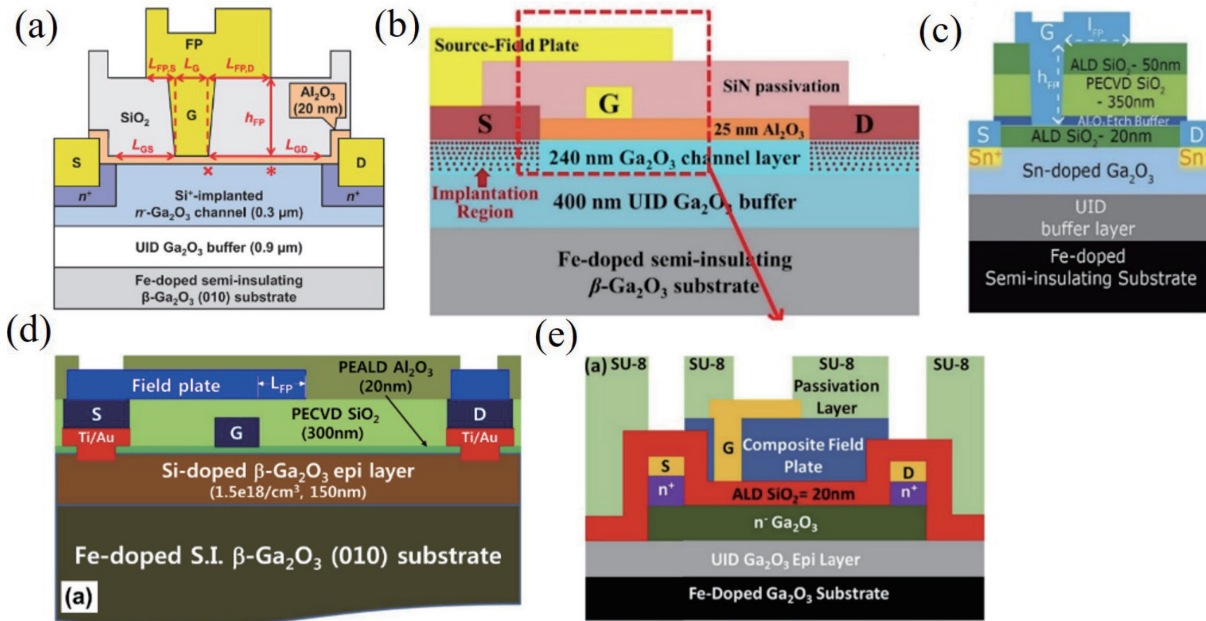

Fig. 20. (Color online) Cross section view of (a) gate-connected Ga_2O_3 FP-MOSFET. © 2015 IEEE. (b) SFP-MOSFET © 2018 IEEE. (c) Composite gate-connected Ga_2O_3 FP-MOSFET © 2018 IEEE. (d) Ga_2O_3 composite field plate MOSFET © Mun *et al*. 2019. (e) Composite gate-connected Ga_2O_3 FP-MOSFET with polymer passivation. © 2020 IEEE.

also exhibit some advantages of this design. In 2019, Hu *et al.* optimized this design via adding the source connected field plate[63]. The breakdown voltage was further increased to over 1.6 kV, and the lower $R_{on,sp}$ of 5.5 mΩ·cm^2 can be extracted with the help of a wider fin shape. Right in the same year, Li *et al.* developed a post-deposition annealing technique that could boost the channel mobility in the β-Ga_2O_3 FinFET[64]. The multi-fin β-Ga_2O_3 FET fabricated by them performed the record high breakdown voltage of 2.6 kV and relatively low $R_{on,sp}$ of 23.2 mΩ·cm^2, further showing the potential of β-Ga_2O_3 FinFET and vertical devices.

4. Other optimizations of β-Ga_2O_3 FETs

Besides realizing the E-mode, there are still some other parameters needed to be optimized in the fabrication of lateral β-Ga_2O_3 FETs. As the direct indicator of device reliability, breakdown voltage has already been considered as the key point for a long time. Recently, the field plate structure has been commonly used to increase the device breakdown voltage. Fig. 20 here shows some representative field plate structure. The employment of the field plate started from the first successful fabrication of β-Ga_2O_3 MOSFETs. Wong *et al.* achieved the first stable β-Ga_2O_3 MOSFET via the gate-connected field plate (GFP) structure[23]. The on/off ratio over 109 and V_{br} of 755 V was obtained through this GFP structure. Later then, Lv *et al.* fabricated the source-connected field plate (SFP) with the V_{br} of 480/680 V, $R_{on,sp}$ of 4.57/11.7 mΩ·cm^2, the $I_{DS,sat}$ of 267/222 mA/mm and the BFOM of 50.4 MW/cm^2 [24]. In 2018, Zeng *et al.* achieved excellent performance β-Ga_2O_3

MOSFET measured a V_{br} of 1850 V for a L_{gd} = 20 μm[65]. The gate-connected field plate was supported by composite atomic layer deposited (ALD) and plasma-enhanced CVD

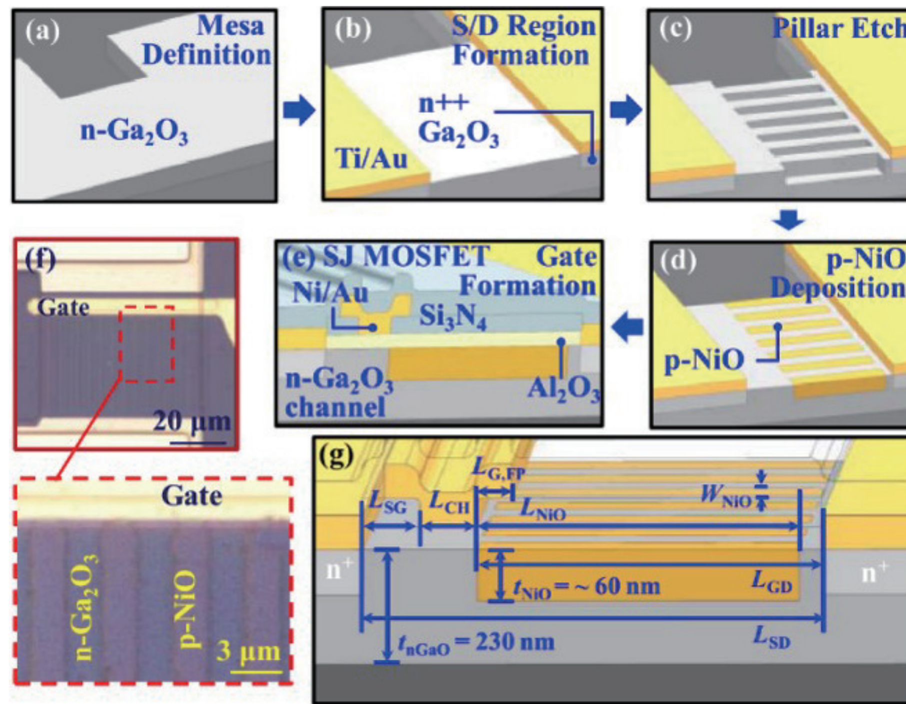

Fig. 21. (Color online) (a–e) Schematic of the fabricating steps for β-Ga_2O_3 SJ-equivalent MOSFETs. (f) The Photographs of SJ formed by parallel arranged p-NiO/n-Ga_2O_3 strips in the region between gate and drain. (g) 3-D schematic diagram of the β-Ga_2O_3 SJ-equivalent MOSFETs. © 2022 IEEE. Reprinted with permission from Ref. [67].

(PECVD) SiO_2 layer, as shown in Fig. 20(c). A similar improvement was also achieved in the SFP β-Ga_2O_3 MOSFETs by Mun *et al.*[66]. Via fabricating SFP β-Ga_2O_3 MOSFETs with L_{gd} of 25 μm and composite PECVD SiO_2 and Si_3N_4 layers, the V_{br} = 2.32 kV was got, and the increase of breakdown voltages followed a linear trend with the L_{gd}. The highest breakdown voltage of lateral β-Ga_2O_3 MOSFETs was observed by Sharma *et al.* in their GFP β-Ga_2O_3 MOSFETs[25]. The self-aligned RIE method was used on the high-doping β-Ga_2O_3 layer to form the source and drain contacts. After the formation of composite oxide layer and the gate-connected field plate, the SU-8 passivation was spin coated on the surface and patterned to open the area of metal pads. The extremely high breakdown voltage of 6.72, 8.03 kV was achieved in the L_{gd} of 40, 70 μm, respectively. Besides, some novel composite FP structures have also been proven to own some excellent properties. For example, the OA treated β-Ga_2O_3 MOSFETs fabricated by Lv *et al.* as mentioned above achieved both the high breakdown voltage and E-mode[50].

Fig. 21 shows another lateral β-Ga_2O_3 MOSFETs structure designed by Wang *et al.* to enhance the device reliability[67]. A super junction (SJ) structure was fabricated in the channel region between the gate and drain. With the help of these p–n junctions, the channel can be easily depleted even with relatively high carrier concentration, resulting in a uniform distribution of the electric field. The breakdown voltage of the device can be increased without the electric field crowding, and the serious sacrifice of on-resistance through decreasing carrier concentration can be avoided. The super junction design has been commonly used in commercialized silicon power devices in order to break the theoretical limit[68]. Some devices based on ultra-wide bandgap materials like SiC[69] and GaN[70], have also adopted the super junction structure to improve their performance. Such a design was not considered in the β-Ga_2O_3 device fabrication at the beginning because of the lack of p-type doping. But the development of p-type NiO offers the possibility to demonstrate β-Ga_2O_3 SJs. Fig. 21 shows the fabrication process of the SJ lateral β-Ga_2O_3 MOSFETs. After the deposition of source and drain metal, the trenches in the drift region were etched in the BCl_3/Cl_2 mixed ambient, followed by a wet treatment to smooth the etched surface. The p-NiO was then epitaxially grown in the trench by radio frequency (RF) reactive magnetron sputtering and lift-off processes. The breakdown voltage of 1326 V can be observed in the trench width of 2 μm. However, the charge balance in the p–n junction is of great importance for the performance of SJ, but the control of hole carrier concentration in p-NiO is not mature enough to stably reach that balance. A big deviation of breakdown voltage among SJ devices could be observed in the study, calling for further development on the p-NiO epitaxial technique.

The poor thermal conductivity is another main drawback of β-Ga_2O_3. Lots of research has been established to overcome this obstacle. Kim *et al.* systematically studied the thermal conducting mechanism on the dependence of two main parameters: the orientation of the channel width and the geometrical design of the metallization structures[71]. The impact of channel orientation on the thermal conducting was first studied through the real structure shown in Fig. 22(b) and the simulation method. Four orientations of 0°/30°/60°/90° were compared in the real device measurement. The 30° device with the channel direction perpendicular to (–201) exhibits the lowest channel temperature rise in the measurement. Besides, the impact of metallization structures on thermal conductivity was tested to exclude the possible influence. Results showed that the metallization structures had little effect on the device thermal conductivity. However, only

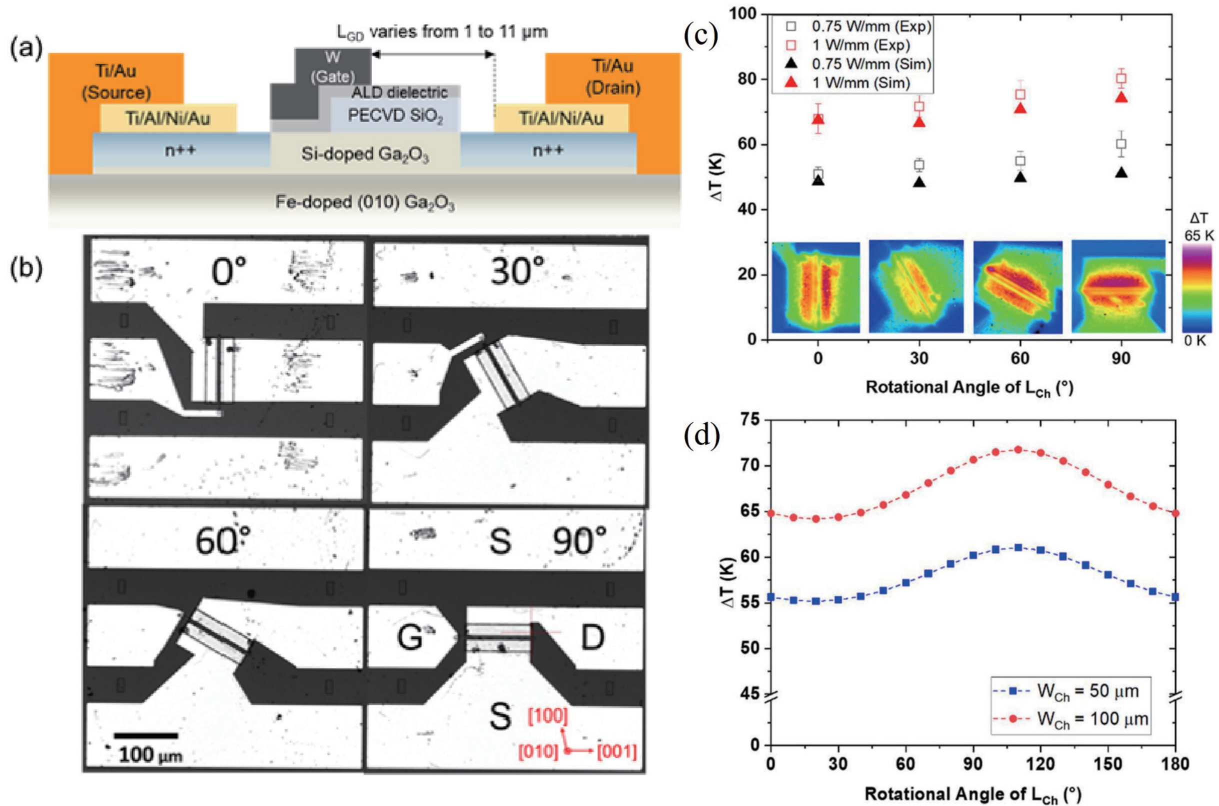

Fig. 22. (Color online) (a) Schematic diagram of the β-Ga_2O_3 MOSFET. (b) CCD images of β-Ga_2O_3 MOSFETs with four different channel orientations. (c) Simulation and experimental results of Gate temperatures and IR images for MOSFETs with different orientations. (d) Simulated results of relation between MOSFET channel temperatures and channel orientation at V_{GS} = 4 V. Two devices with different channel widths of 50 and 100 μm were used in this simulation. © 2022 IEEE. Reprinted with permission from Ref. [71].

rotating the channel direction cannot afford enough heat dissipation that exceeds the limit of β-Ga_2O_3. The specific design to systematically improve the device thermal conductivity is needed in the fabrication of β-Ga_2O_3 MOSFETs. Recently, Song *et al*. have achieved the lateral β-Ga_2O_3 MOSFETs on the β-Ga_2O_3/4H-SiC composite wafer. By bonding the Ga_2O_3 substrate with other material with relatively high thermal conductivity, the self-heating problem of the Ga_2O_3 device can be somehow relieved to a certain extent. It is believed that diamond might be another material that can assist the device heat dissipation. The study of device-level transient cooling via diamond was also established by Kim *et al*.[72]. As shown in Fig. 23, three structures were fabricated to compare the heat dissipation performance under steady-state and high frequency power switching conditions. The result shows that the steady-state channel temperature can be reduced by 65% through the backside bonding on the substrate. However, the second option didn't exhibit the expectative heat dissipation ability during the high frequency power switching condition, proving that the composite substrate did not improve the transient thermal response of the device. The third option with the diamond heat spreader on both sides of the device exhibited the best performance during the high frequency power switching condition, indicating that the double-side cooling schemes might be a common choice for device-level transient cooling in the near future.

5. Conclusion and outlook

In conclusion, there have been considerable improvements in the design of E-mode β-Ga_2O_3 FETs. Three main fabrication schemes proposed for lateral E-mode design in recent years are channel reshaping, channel doping modulation, and the selection of proper gate material. Starting from the wrap-gate design, the E-mode lateral β-Ga_2O_3 FETs has been proven feasible through the channel reshaping scheme, and the invention of recessed-gate structure paved a simple way to fabricate E-mode Ga_2O_3 FETs. The UID channel MOSFETs is another feasible attempt, but the high on-resistance and threshold voltage call for the proper modulation of channel doping. Some E-mode devices with novel channel doping distribution have been achieved in simulation, and other methods like OA treatment can also effectively change the device's doping concentration. As for the choice of gate material, the β-Ga_2O_3 HJ-FETs using p-NiO to form the HJ gate structure has been considered as a possible solution for achieving the E-mode. Besides, there are still some novel materials like L-FeG that deserve to be carefully studied to enhance the gate control ability. Besides, there are still some novel materials like L-FeG that deserve to be carefully studied to enhance the gate control ability. Besides, the E-mode vertical Ga_2O_3 FET has been accomplished via the CBL structure, FinFETs and so on. Even though these attempts are still at a preliminary stage, the potential of these vertical devices is still worth exploring.

However, few of these E-mode fabrication schemes have reached the application standard due to their intrinsic drawbacks and the immaturity of β-Ga_2O_3 device fabrication technology. The high subthreshold swing of recessed-gate structure and FinFETs indicates the existence of interface states caused by the etching process. These harmful defects can be

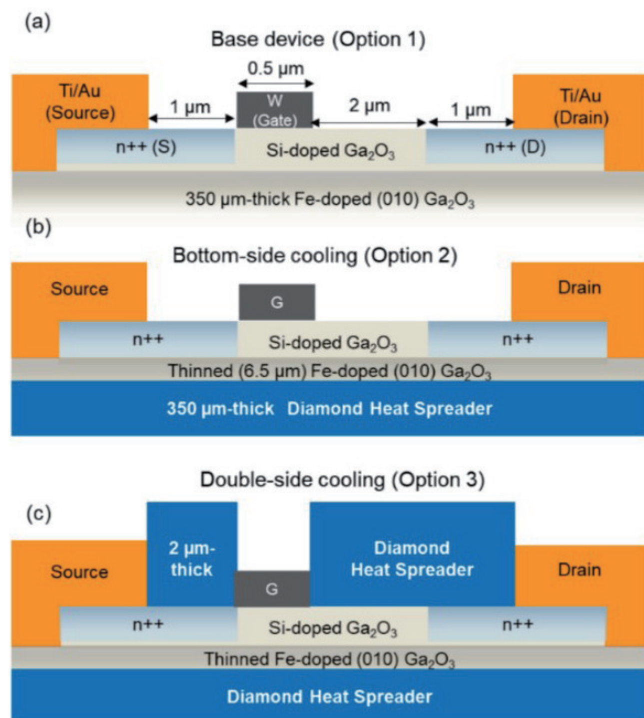

Fig. 23. (Color online) (a) Option 1: Cross section view of a lateral β-Ga_2O_3 MOSFETs. (b) Option 2: A simulated structure with the β-Ga_2O_3 substrate bonded by the diamond at the bottom. (c) Option 3: A simulated structure based on the option 2 in (b) optimized by depositing the polycrystalline diamond over the exposed part of β-Ga_2O_3 channel layer. © 2022 IEEE. Reprinted with permission from Ref. [72].

removed via some wet-etching processes like hot concentrated phosphoric acid (H_3PO_4) treatment. But even if the defects can be effectively eliminated , the inevitable sacrificing of on-resistance is still a big problem for recessed-gate lateral MOSFET, while the stability is still a big problem for the FinFET structures. As for the channel doping modulation, the experimental realization of these doping distribution was still absent except for the OA treatment due to some technical difficulties. A similar problem also occured in the study of β-Ga_2O_3 HJ-FETs. The E-mode can be observed in the simulation process, but this E-mode can be achieved without the help of recessed-gate in the real fabrication. Except for realizing the E-mode, the β-Ga_2O_3 devices are still facing some basic problems. The device reliability needs to be further optimized through structures like field plates to approach the material limit of β-Ga_2O_3, and the bonding of high thermal conductivity material can probably solve the thermal conductivity problem. Fortunately, these difficulties mentioned above have their own solutions, which require further understanding of the material property.

In summary, considerable improvement has been achieved in the realization of E-mode β-Ga_2O_3 FETs. The gap between experiments and applications will exist for a long time since the β-Ga_2O_3 device fabrication is not mature enough now. Still, breakthroughs in the p-type doping of β-Ga_2O_3 or the further optimization of p–n HJ are needed to achieve the applicable β-Ga_2O_3 FETs.

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