REVIEWS

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Volatile threshold switching memristor: An emerging enabler in the AIoT era

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Abstract: With rapid advancement and deep integration of artificial intelligence and the internet-of-things, artificial intelligence of things has emerged as a promising technology changing people's daily life. Massive growth of data generated from the devices challenges the AIoT systems from information collection, storage, processing and communication. In the review, we introduce volatile threshold switching memristors, which can be roughly classified into three types: metallic conductive filament-based TS devices, amorphous chalcogenide-based ovonic threshold switching devices, and metal-insulator transition based TS devices. They play important roles in high-density storage, energy efficient computing and hardware security for AIoT systems. Firstly, a brief introduction is exhibited to describe the categories (materials and characteristics) of volatile TS devices. And then, switching mechanisms of the three types of TS devices are discussed and systematically summarized. After that, attention is focused on the applications in 3D cross-point memory technology with high storage-density, efficient neuromorphic computing, hardware security (true random number generators and physical unclonable functions), and others (steep subthreshold slope transistor, logic devices, *etc.*). Finally, the major challenges and future outlook of volatile threshold switching memristors are presented.

Key words: AIoT; threshold switching; memristor; selector; neuromorphic computing; hardware security

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1. Introduction

From smart home[1], smart city[2] to smart planet[3], artificial intelligence (AI) plays an important role that will greatly change people's daily lives and human civilization. With numerous flows of data streamed from internet-of-things (IoT) devices that are increasing by a billion per year, the ability to process data in an effective manner is urgently demanded. Consequently, the artificial intelligence of things (AIoT) has emerged as a promising technology attracting much attention from industry and academia[4]. Deep integration of AI and IoT allows the connected physical objects (intelligent devices) not only exchange information with each other, but also process data and make decisions at the edge. In AIoT systems, IoT devices act as the "body" that can interact with real environments (light, sound, gas molecules, *etc.*), collecting data and creating a network for transmitting critical information to the processing center, while AI is the "brain" that can store information and process data by machine learning. Nowadays, AIoT has been integrated into our surroundings and own wide applications in various fields[5–10] like social networks, industry, agriculture, architecture, health care, *etc.* It is of great significance to push the development of AIoT technology.

However, the AIoT system is facing several challenges to be solved. (1) High storage-density of memory chip is increasingly demanded. Thanks to the development of 3D integration technology[11], more memory units with smaller space and lower cost become possible. (2) Advanced computing technology with high energy efficiency is desired for timely and effective data-processing. Neuromorphic computing technology such as deep neural network (DNN) and spiking neural network (SNN) appears in recent years[12]. The employment of DNN and SNN can contribute to the realization of in-memory computing and in-sensor computing, which improve the energy efficiency in the edge devices like smart phones, wearable sensors, and unmanned vehicles. (3) Hardware security has to be considered during data communication and information sharing. The increased security threats to the internet and sensor networks must be simultaneously addressed to improve data confidentiality[13].

The solutions to the above challenges in AIoT cannot be separated from the exploration of emerging nano-devices. One of the most promising candidates is the memristor, which was proposed by Chua in 1971 as the fourth elemental circuit component[14]. Memristors have advantages of simple structure, high 3D integration potential, high compatibility with complementary metal oxide semiconductor (CMOS)

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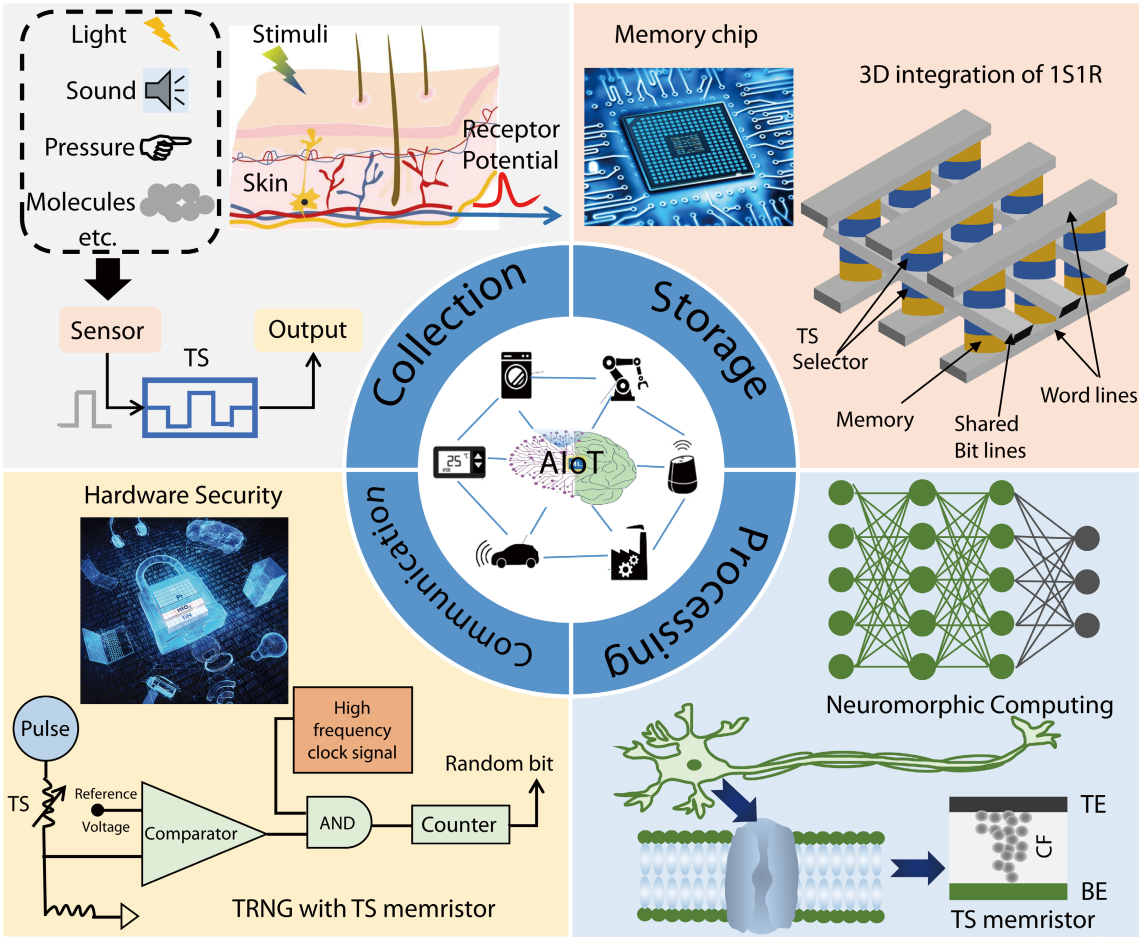

Fig. 1. (Color online) Overview of volatile TS memristors enabling the entire process of data and information collection, storage, processing, and communication in AIoT systems.

and low power consumption. According to the retention time of low resistance state (LRS), memristors can be divided into volatile and nonvolatile types. As for nonvolatile memristors, LRS can be maintained after the removal of voltage bias. Nevertheless, the volatile memristors would spontaneously return back to HRS from LRS after the removal of the external electric field in milliseconds to nanoseconds. Volatile memristors, also known as threshold switching (TS) devices, have broad applications in the various fields[15–20] of perceptron, memory array, neuromorphic computing, true random number generation (TRNG), *etc.* As shown in Fig. 1, volatile TS memristors help to enable the entire process of data and information collection, storage, processing, and communication in AIoT systems.

In the review, we introduce the device, switching mechanisms, and applications of volatile TS memristors. In Section 2, volatile TS memristors are classified into three categories: metallic conductive filament (CF) type, amorphous chalcogenide-based ovonic threshold switching (OTS), and metal-insulator transition (MIT) type. Their materials, structures, switching mechanisms, and characteristics are summarized. The applications of volatile TS memristor in selectors, artificial neurons, nociceptors, and hardware security are discussed in details in Section 3. In the last section, the challenges and perspectives are presented.

2. Categories and physics

The volatile TS memristor is one kind of two-terminal devices with sandwich structures (electrode/dielectric/electrode), where the dielectric layer plays a key role in resistive switching. A great number of materials have been explored as the switching layer in the past few decades including oxides[21–29], 2D films[30–32], perovskites[33], chalcogenides[34–36] and others[37–39]. In fact, there is no difference in structure and materials between volatile and nonvolatile memristors, and even one device could exhibit both volatile and nonvolatile properties at different compliance currents[39]. According to the switching mechanisms, volatile TS memristors can be divided into three categories: metallic conductive filament, OTS and MIT. Their typical structures and *I*–*V* characteristics are presented in Fig. 2 and switching mechanisms will be discussed below in detail.

2.1. Metallic conductive filament type

Volatile TS devices principally enabled by metallic conductive filaments are also called diffusive memristors, which have attracted tremendous attention because of the simple device structure, easy fabrication, and high compatibility with CMOS lines[40, 41]. Metallic CF formation involves the following three successive processes: (I) oxidation of the metal atoms into mobile cations ($X \rightarrow X^{n+} + ne^-$) at the interface between the active electrode (Ag or Cu) and dielectrics under an influence of external electric field, (II) migration of cations towards the inert electrode, (III) reduction of cations ($X^{n+} + ne^- \rightarrow X$) and the nucleation of active metal nanocluster. When the discrete nanoclusters grow and connect the electrodes, the fila-

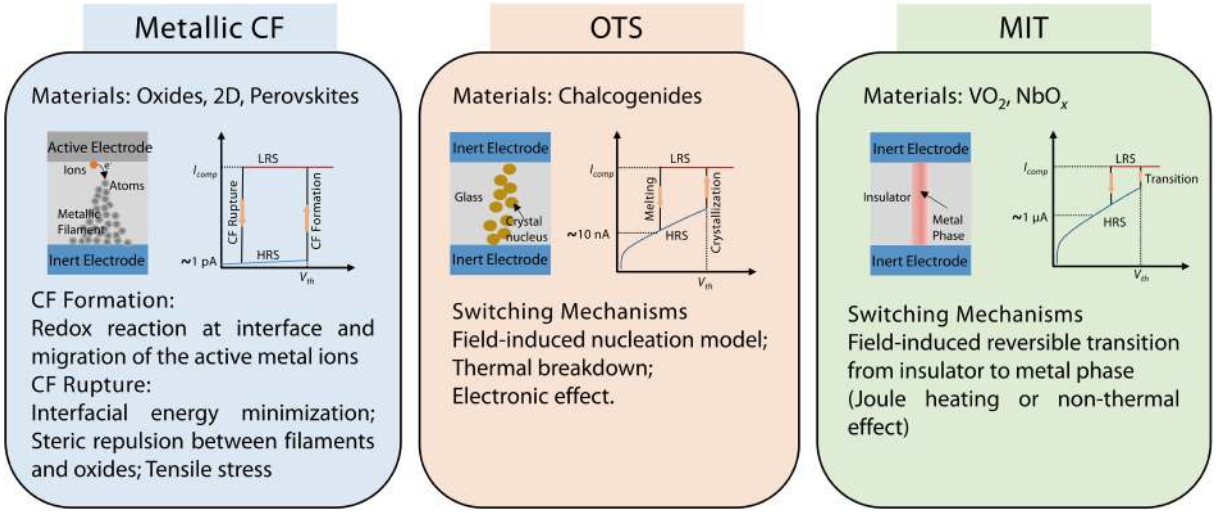

Fig. 2. (Color online) Categories and switching mechanisms of volatile TS memristors.

ment forms and the device turns into low resistance state. The transition from HRS to LRS occurs within a finite time duration, known as delay time. The delay effect is believed to be a consequence of ionic or atomic motion induced filament growth, and delay time is dependent on the amplitude and width of the applied voltage pulse. Yang *et al.*[42, 43] performed an experimental observation of filament growth via *in-situ* high-resolution transmission electron microscopy (HRTEM) technology, and constructed the relationship between filament evolution and the kinetic parameters of dielectrics including ion mobility (μ_i) and redox rate (Γ). The growth modes can be roughly categorized into four types: (1) an inverted cone shape with growing from the inert electrode when both μ and Γ are high, (2) a forward cone shape with discrete nanoclusters growing from the active electrode when both μ and Γ are low, (3) nucleation inside the dielectric and re-connection with the source when μ is low but Γ is high, and (4) a branched structure growing from the inert electrode when μ is high but Γ is low.

Once the filaments form, the interplay between filament and surrounding environments determines their evolution. With the decrease or removal of the external electric field, the filament tends to rupture spontaneously, leading to the transition from LRS to HRS within a finite time duration (relaxation time). To have a better understanding on the spontaneous rupture features of diffusive memristors, researchers have paid huge efforts to study the relevant physics[44–48]. Among them, the theory of interfacial energy minimization is widely adopted. Wang *et al.*[45] observed the spontaneous relaxation in Au/SiO_xN_y:Ag/Au device using *in-situ* HRTEM, and it was demonstrated that minimizing the interfacial energy between Ag nanoparticles and the dielectrics served as the driving force for these diffusive memristors. The material systems exhibiting a substantial relaxation dynamics are those with large contact angles[49], such as MgO_x:Ag, SiO_xN_y:Ag, HfO_x:Ag. The spontaneous rupture of filaments is dominated by the surface diffusion of metal atoms. Apart from the interfacial energy minimization, Song *et al.*[50] proposed that there was steric repulsion between Ag filaments and TiO_2 matrix in Ag/TiO_2 systems. To minimize the steric repulsion, Ag 5s electrons in filaments are transferred to the Ti 3d states, leading to the oxidation (rupture) of Ag filaments and the formation of localized Ti^{3+} ions. In addition, Ambrogio *et al.*[51] indicated that the tensile stress existed in the dielectrics, changing the migration barriers to/from the active electrode and accelerating the atoms back to the active electrode, which resulted in the spontaneous rupture of the filament.

2.2. OTS type

In the 1960s, Ovshinsky[52] systematically described the OTS phenomenon and patented his discovery, which opened up a new field of research. The OTS phenomenon was found in many disordered materials, particularly amorphous chalcogenides with band gap between 0.6 and 1.4 eV. Fig. 2 shows a typical *I*–*V* curve of the OTS glass, in which the device initially presents off-current at the level of nA. When the applied voltage exceeds the threshold value V_{th}, the device switches into LRS and turns back to the original HRS if the voltage decreases lower than the hold value V_{hold}. The switching process is highly repeatable and the *I*–*V* characteristics remain almost unchanged with millions of cycles in a well-processed OTS device. In some amorphous chalcogenides, Joule heating induced crystallization of glass may happen, and unexpected memory switching (MS) occurs where LRS remains after removing the applied voltage. They are also called phase-change materials and widely used in the next-generation information storage products such as PCRAM. To fabricate the OTS device without an MS effect, amorphous chalcogenides with high activation energy of crystallization are advised.

To date, various theories have been developed to explain the OTS behavior. The field-induced nucleation model[53] points out that the electric field reduces the energy barrier of nucleation and the critical nucleus size, promoting the spontaneous growth of crystal nucleus. Once the electric field is removed, the energy barrier recovers and the as-grown crystalline nucleus become unstable and quickly dissolve. The nucleation model, even though similar to the growth of conductive filaments, does not totally comply with the experimental facts. The crystallization rate of OTS materials is usually extremely fast (~nanoseconds), and the nucleus size easily grows large enough over the critical value, inevitably resulting in the memory switching. The number of the filaments in the devices are also far less than the required defect density (~ 10^{19} cm^{-3}) for the TS behavior[54].

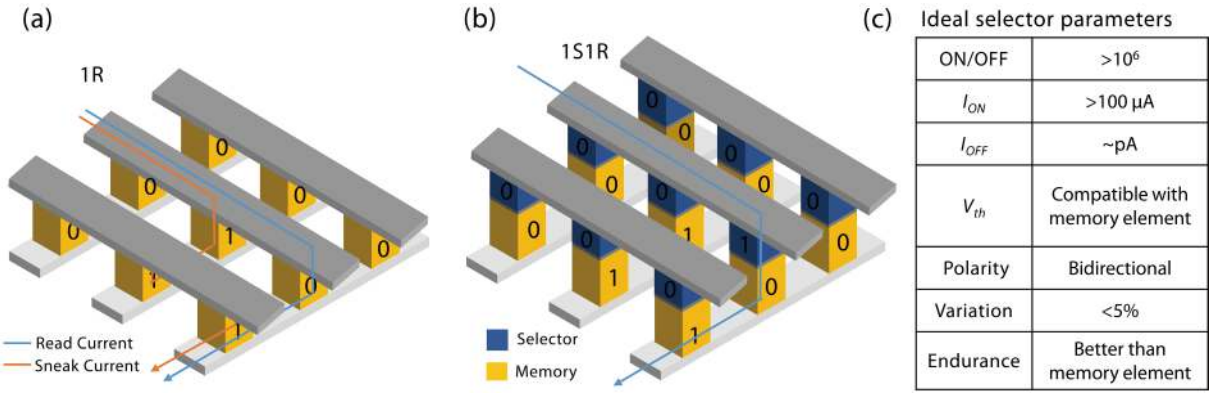

Fig. 3. (Color online) Cross-point memory technology in 1S1R configuration. (a) Schematic illustration of sneak path current in cross-point array during read operation. "0" means off-state, while "1" stands for on-state. (b) Memory with integration of selector to limit the sneak current. (c) Requirements of an ideal selector in cross-point memory.

A more competent model to explain the OTS phenomenon is the electronic effect instead of the atomic movement. In early years, researchers believed that the voltage bias could heat the semiconductor and activate electrons to the conduction band, increasing the current density which results in higher temperature and more conducting electrons, leading to a "thermal breakdown". Later, Ielmini *et al.*[55] revealed that Joule heating is not a mandatory process in the OTS devices. It is well known that the band gap in the amorphous semiconductors is filled by localized trap states due to the Anderson localization of electronic wave functions and defective homopolar bonds, and the conducting electrons are easily trapped in these defect states. The external voltage could reduce the energy barriers to activate the trapped electrons, and thus increase the conductivity, similar to the trap-limited Poole-Frank mechanism. This pure electronic effect can explain the fast and durable switching of OTS devices well. However, the theory was recently challenged by a few research groups who discovered that there are subtle structural and bonding changes upon the TS process. Guo *et al.*[56] found that some homopolar filaments formed in the glass and Raty *et al.*[57] believed that the electric excitation drives the formation of the meta-valent bonds (a new type of chemical bond in PCMs proposed by Wuttig *et al.*[58, 59]). The switching mechanisms in OTS devices are still elusive and need in-depth explorations.

2.3. MIT type

The MIT in vanadium oxides (VO_x) and niobium oxide (NbO_x) has been extensively studied for almost one century[60], but the exact mechanism remains a challenge in the contemporary condense matter physics, impeding the applications of these materials on modern electronic devices. The transition of VO_2, the archetypal material, takes place at about 341 K, where VO_2 transforms from a high-temperature metallic rutile structure (TiO_2-type) to a low-temperature insulating monoclinic phase. The transition can be triggered by various perturbations, such as temperature, light, pressure and chemical doping. In electronic devices, the MIT phenomenon occurs under an influence of external electric field and leads to resistive switching, as presented in Fig. 2.

There has been a debate over the mechanism of the transition: structure distortion (Peierls type)[61] versus electron correlation (Mott-Hubbard type)[62]. The metallic phase at high temperature is naturally due to the overlap of the valence band and conduction band, leading to free electron transport. The controversy mostly concentrates on the low-temperature insulator. Schulz *et al.*[63] performed unconstrained ab-initio molecular dynamics simulations (single-electron approximation) on the insulating phase of VO_2, and found that the low-temperature ground-state structure indeed exists and it opens the band gap because of the Peierls distortion. They concluded that the insulating behavior could be simply ascribed to structure transition that leads to the change of electronic structure, and thus the strong electron–electron correlation becomes obsolete to account. However, the vast majority of literature[64, 65] pointed out that the low-temperature VO_2 is a Mott-Hubbard insulator, raising strong opposition to the above "band insulator" view. The theory contributes insulating feature to the Coulomb repulsion between electrons instead of the lack of free electrons in the conduction bands, and the transition is a consequence of strong correlative interaction between electrons rather than structure distortion. Recently, the above two mechanisms could be simultaneously investigated in the same MIT materials[66, 67].

Concerning the electric field-induced transition in electronic devices, the mechanism is also under heavy debate in the scientific community. Joule heating due to current flow is an obvious candidate for explaining the transition[68–70]. However, it has been argued that the electric field applied in the process may induce the transition non-thermally without heating the materials to its critical temperature. Kalcheim *et al.*[71] demonstrated that a purely non-thermal electrical MIT can occur in both VO_2 and V_2O_3 nanowires. The mechanism behind the non-thermal effect was identified as field-assisted carrier generation leading to a doping-driven MIT. Later, Valle *et al.*[72] used in-operando optical reflectivity to capture the growth dynamics of the metallic phase with space and time resolution. They demonstrated that growth of the metallic phase during the field-driven MIT can be explained just by considering the effect of Joule heating, but the transition of the first metallic domains remained unclear.

3. Roles of volatile TS devices in AIoT applications

3.1. Selectors

To meet the demand of high-density storage in AIoT systems, resistive memory technology with 3D cross-point architecture appears and attracts much attention[45, 73]. Resistive

Table 1. Summary of the recent reported volatile threshold switching devices and their corresponding characteristics. "–" means that no such characteristic was found.

Device/Materials	V_{th} (V)	I_{on}	I_{off}	ON/OFF	Endurance	Speed	Polarity
Cu/Cu:HfO_2/HfO_2/Pt[85]	0.4	10 μA	1 pA	10^7	–	50 ns/100 ns	Unidirectional
Cu/SiO_2/Pt[21]	0.7	500 μA	10 pA	5×10^7	50	4 ms/1 ms	Unidirectional
Ag/ZrO_2/Pt[175]	0.25	1 mA	100 pA	10^7	200	–	Unidirectional
Ag/SiTe/TiN[176]	0.6	100 μA	10 nA	10^4	10^5	5 μs/3 μs	Unidirectional
Ag/DDG/SiO_2/Pt[83]	0.6	500 μA	1 pA	5×10^8	10^6	100 ns/1 μs	Bidirectional
Ag/HfO_2/Pd[75]	0.15	1 mA	0.1 pA	10^{10}	10^8	75 ns/250 ns	Unidirectional
Ag/HfO_2:N/Pt[173]	0.2	500 μA	1 pA	5×10^8	10^6	1.5 μs/5 μs	Unidirectional
Ag/MoS_2/Au[32]	0.35	100 μA	100 pA	10^6	5×10^6	–	Unidirectional
Pt/Cu_2O/Ag:Cu_2O/Cu_2O/Pt[177]	0.5	1 μA	1 nA	10^3	–	–	Bidirectional
Ag/TaO_x/TaO_y/TaO_x/Ag[178]	0.15	1 mA	1 pA	10^9	10^6	75 ns/500 ns	Bidirectional
Ag nanodot/HfO_2/Pt[76]	0.25	1 mA	1 pA	10^9	10^8	110 ns/240 ns	Bidirectional
$AgTe_{35\%}$/TiN/TiO_2/Pt[169]	0.4	100 μA	0.1 pA	10^9	10^8	10 ns/100 ns	Unidirectional
AgGeSe/Al_2O_3/Pt[81]	0.4	3 mA	0.1 pA	10^{10}	10^5	300 ns/30 μs	Unidirectional
Ag/TiN/HfO_2/Pt[82]	0.2	100 μA	10 pA	10^7	10^5	28 ns/50 μs	Unidirectional
Pt/Ag:ZnO_2/Pt[84]	0.7	1 mA	10 fA	10^{11}	10^6	38 ns/64 ns	Unidirectional
Ag/TiN/HfO_x/HfO_y/HfO_x/Pt[86]	0.25	3 mA	0.1 pA	10^{10}	10^6	60 ns/500 ns	Unidirectional
Ge–Se[90]	1.4	450 μA	129 nA	10^3	10^8	2 ns	Bidirectional
$Ge_{58}Se_{42}$[91]	3.5	10 μA	100 pA	10^5	10^9	50 ns	Bidirectional
Ge–Se–N[92]	4	450 μA	2 nA	10^5	10^8	–	Bidirectional
Ge–Se–As[93]	2.5	10 mA	1 nA	10^7	5×10^5	–	Bidirectional
Ge–Se–Sb–N[94-96]	1.94	100 μA	10 pA	10^6	10^9	–	Bidirectional
$GeTe_6$[97]	1.6	650 μA	–	10^5	600	5 ns	Bidirectional
Ge–As–Se–Te[98]	1	1 μA	200 pA	10^3	10^{10}	–	Bidirectional
Ge–As–Te–Si[99]	1.2	100 μA	1 μA	10^2	10^2	–	Bidirectional
Ge–As–Te–Si–Se[100, 101]	2.2	420 μA	1.9 nA	10^5	10^{10}	50 ns	Bidirectional
Si-Te[102]	1	100 μA	100 nA	10^3	10^8	2 ns	Bidirectional
Si–As–Te[103]	1.49	–	10^3 nA	–	10^3	–	Bidirectional
C–Te[104]	0.65	400 μA	5 nA	10^5	10^8	2 ns	Bidirectional
B–Te[105]	0.75	380 μA	2 nA	10^5	10^8	2 ns	Bidirectional
$Zn_{35}Te_{65}$[106]	0.6	6 mA	60 nA	10^5	–	–	Bidirectional
AlTe[107]	0.7	200 μA	4 nA	10^5	10^7	2 ns	Bidirectional
Te[110]	1.3	1 mA	1 μA	10^3	10^9	11 ns	Bidirectional
GeTe–C–N[179]	1.3	200 μA	10 nA	10^4	10^{11}	–	Bidirectional
$GeTe_x$–C[34]	1.26	2 mA	2 nA	4.2×10^4	10^7	8.5 ns	Bidirectional
GeS[180]	3.2	10 mA	10 nA	10^6	10^8	10 ns	Bidirectional
SiOTe[111]	1.2	–	3 nA	10^4	10^9	3 ns	Bidirectional
SiGeAsTe[181]	2.2	100 μA	0.8 nA	10^5	10^{11}	–	Bidirectional
TiN/VO_2/HfO_2/TiN[182]	0.7	400 μA	20 μA	20	–	30 ns	Bidirectional
Pt/Ti:NbO_x/TiN[115]	1.3	66 mA	–	10	10^3	–	Bidirectional
V/VO_x/TiN[183]	1	10 mA	10 μA	1000	10^9	60 ns	Bidirectional
Pt/VO_xN_y/VO_x/VO_xN_y/Pt[184]	1.38	20 μA	2 μA	10	10^3	–	Bidirectional
Pt/Ti:NbO_x/Pt[114]	1.5	–	50 pA	50000	10^5	20 ns	Bidirectional
Pt/NbO_x/Ru[185]	0.7	500 μA	–	100	10^6	90 ns	Bidirectional
Pt/Nb_2O_5/Pt[186]	–	–	–	–	10^9	0.7/2.3 ns	Bidirectional
Pt/$(V_{1-x}Cr_x)_2O_3$/TiN[187]	1.7	450 μA	11 μA	–	10^{12}	10 ns	Bidirectional
Pt/NbO_2/TiN[116]	1.08	1 mA	2 μA	500	10^{12}	10 ns	Bidirectional
V/VO_x/HfWO_x/Pt[188]	1	1 mA	10 μA	100	10^{12}	25/30 ns	Bidirectional
Pt/NbO_x/ZrO2/TiN[189]	0.53	500 μA	6 μA	84	–	–	Bidirectional

memory devices have extremely high densities and ultra-low power consumption due to its simple two-terminal structure and reducing device size as small as $4F^2$ (F is the minimal feature size). However, the cross-point array is always suffering from the sneak path current from neighbor cells during write or read operations, as shown in Fig. 3(a). The problem would reduce the read accuracy and increase power consumption, which hinder the large-scale integration. Consequently, selectors are integrated with memory devices at each cross-point cell to deal with the sneak current problem[19]. Among various types of selectors, two-terminal selectors are more prone to 3D cross-point integration, which is considered as one-selector-one-resistor (1S1R) configuration (Fig. 3(b)). To limit the sneak current from the unselect or half-select memory element during both read and write operation, an ideal selector should have high non-linearity (on/off ratio) and ultra-low leak-

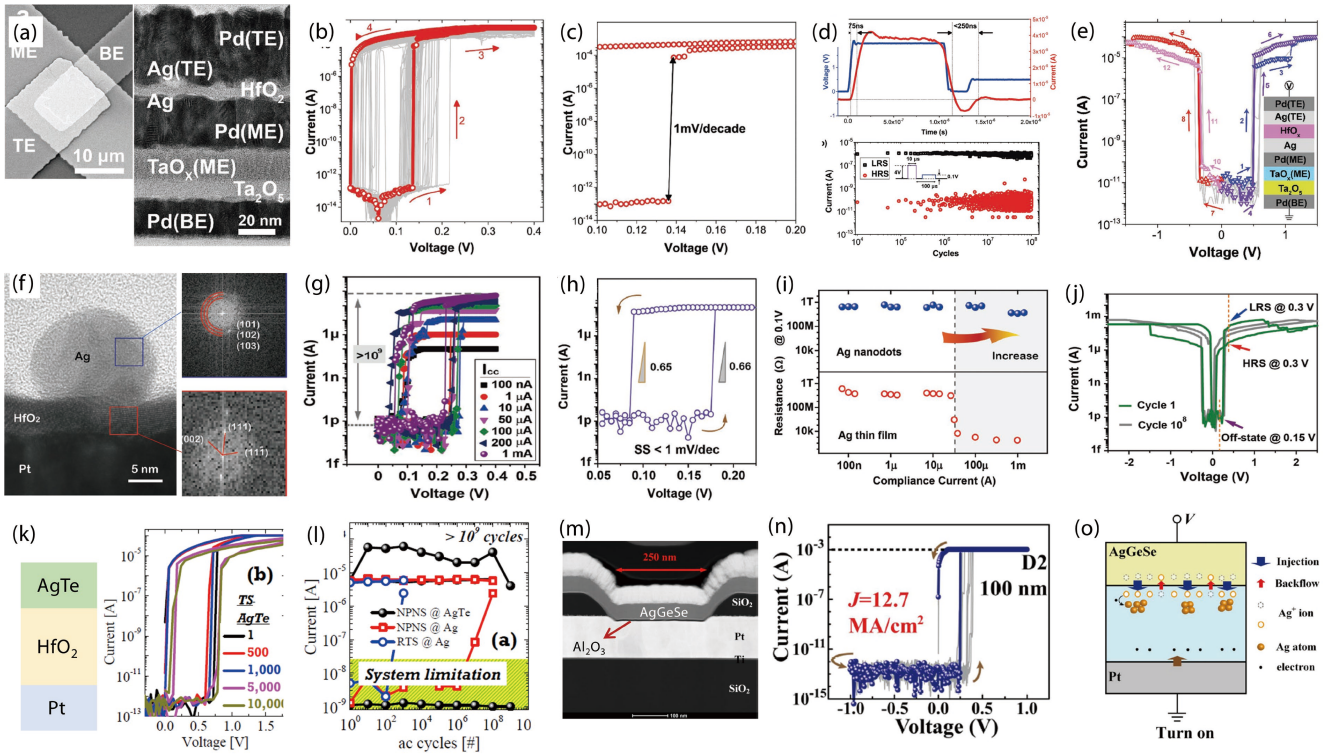

Fig. 4. (Color online) Performance enhancement of CF-based selectors from active electrode engineering. (a) SEM image and cross-sectional TEM image of Pd/Ag/HfO_2/Ag/Pd/TaO_x/Ta_2O_5/Pd devices. (b) DC *I*–*V* characteristic of the Ag/HfO_2/Pd selector yields a selectivity of 10^{10}. (c) The device shows a switching slope of 1 mV/decade. (d) switching speed and endurance performance of the selectors. (e) DC *I*–*V* characteristic of the vertically integrated selector and RRAM (1S1R). (f) Cross-sectional TEM image of the Ag nanodots/HfO_2/Pt device. (g) Threshold switching behavior at different compliance currents from 100 nA to 1 mA. (h) The device has an extremely small switching slope of <1 mV/decade. (i) Read resistance following turn-on operation with compliance currents. (j) DC *I*–*V* characteristic of the integrated 1S1R device before and after 10^8 cycles. (k) Highly improved stable TS in AgTe alloy device with 10^4 DC cycles. (l) Endurance of the AgTe alloy TS device (10^9 cycles). (m) Cross-sectional TEM image of the AgGeSe/Al_2O_3/Pt device. (n) The selector with a 100 nm feature size shows repeatable TS characteristics at a compliance current of 1 mA, providing a 12.7 MA/cm^2 on-current density. Reproduced with permission from (a–e) Ref. [75] Copyright 2017 Wiley-VCH, (f–j) Ref. [77] Copyright 2019 Wiley-VCH, (k, l) Ref. [80] Copyright 2020 IEEE Publishing, (m-o) Ref. [81] Copyright 2021 IEEE Publishing.

age current (I_{off} ~ 1 pA), as presented in Fig. 3(c). In addition, the selector should be compatible with the memory (PCRAM or RRAM), including threshold voltage V_{th}, resistance, polarity and endurance. Herein, selectors based on three-types of TS devices are discussed in detail below.

3.1.1. CF-based selectors

As an emerging memory technology, RRAM is often used for embedded or standalone applications. To reach a high integration density, the most important characteristics of selectors are high selectivity (low I_{off} and large I_{on}), low operation voltage, and steep switch slope. The TS devices dominated by metallic CF formation and spontaneous rupture can meet these strict requirements. Taking TaO_x RRAM[74] as an example, the reset operation happens at the current of 50 μA, implying that the CF selectors should maintain volatility above 50 μA. Other performance and reliability metrics should also match with the state-of-the-art RRAMs, such as switching speed (less than 10 ns), endurance (over 10^{12}), threshold voltage, uniformity, and bidirectional switching.

Until now, there have been various dielectrics demonstrating superior threshold switching characteristics with the active top electrode (Ag or Cu), such as HfO_2, ZrO_2, SiO_2, TaO_x, MoS_2, SiTe alloys, amorphous Si, amorphous C, *etc.* Their performances are listed in Table 1. Among them, oxides are widely exploited due to their high compatibility with RRAM and relatively reliable performances. Midya *et al.*[75] achieved an extremely high non-linearity (10^{10}) with an Ag/HfO_2/Pd device, as shown in Figs. 4(a)–4(e). The device had an ultra-low leakage current at the level of 0.1 pA, and threshold switching happened at ~0.15 V with slope less than 1 mV/decade. The on-current also reached 1 mA. The Ag/HfO_2/Pd selector was integrated with TaO_x RRAM and *I*–*V* curves of the 1S1R cells were exhibited in Fig. 4(e). The switching on and off speed was 75 and 250 ns, respectively. However, the endurance was unsatisfactory (~10^8 cycles). The cycle-to-cycle (C2C) and device-to-device (D2D) uniformity of V_{th} were poor. These days, in order to improve the performance of metallic CF-based selectors, numerous methods are proposed to regulate and control the CF evolution.

Firstly, the device can be optimized from the aspect of the active electrode, which works as metal reservoirs of the filaments. Ag or Cu thin films as active electrodes cause the stochastic filament formation and stuck-on issues, which leads to poor cycle endurance. Therefore, Hua *et al.*[76] proposed highly ordered Ag nanodots with diameter of ~15 nm to replace Ag thin films. With the help of rapid thermal annealing (RTA) at 500 °C for 30 s[77], the Ag nanodots/HfO_2/Pt device exhibited excellent threshold switching characteristics, as shown in Figs. 4(f)–4(j). The on-current reached 1 mA and the endurance was improved to 10^8 cycles. The mechanisms

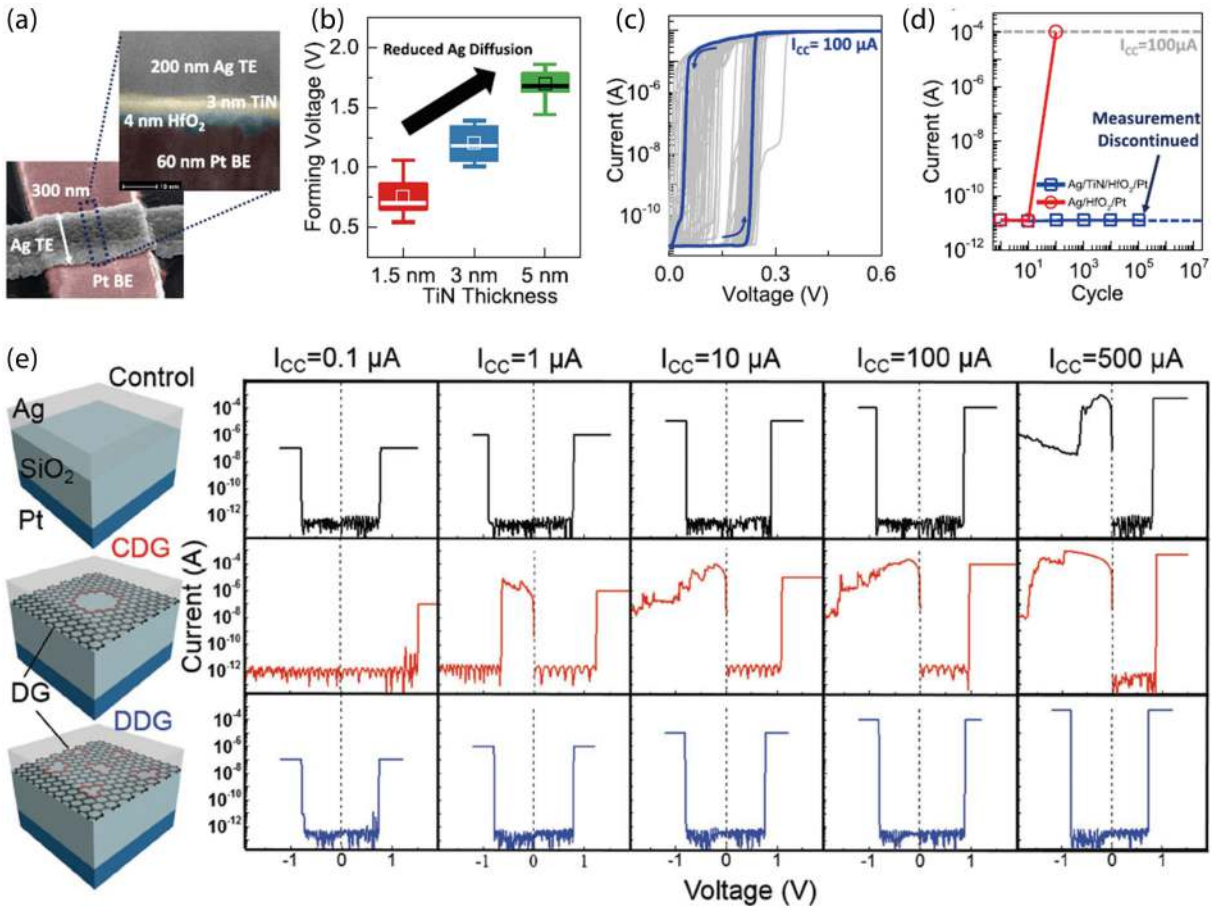

Fig. 5. (Color online) Performance enhancement of CF-based selectors from interface engineering. (a) False colored SEM and cross-sectional TEM images of the Ag/TiN/HfO_2/Pt device. (b) Forming voltage dependence on TiN diffusion barrier thickness for 25 devices. (c) *I*–*V* characteristics of the selector with 3 nm TiN barrier. (d) Endurance comparison of the selectors with and without the TiN barrier. (e) Cell structure and typical DC *I*–*V* characteristics of the Ag/defective-Graphene/SiO_2/Pt devices. Reproduced with permission from (a–d) Ref. [82] Copyright 2019 IEEE Publishing, (e) Ref. [83] Copyright 2018 Wiley-VCH.

were believed to be the formation and rupture of multiple weak filaments. Ag nanodot structure restricted the silver atoms/clusters distribution at the interface of the top electrode and HfO_2 dielectrics, inhibiting the excessive migration of silver. The RTA treatment could contribute to pre-diffusion of Ag atoms into the HfO_2 matrix, which induced multiple narrow channels. The formed channels maintained weak filament formation at high compliance current. Apart from nanodots, nanotip electrodes are also demonstrated to be helpful in improving device performances. The compound electrode is another common method. Firstly reported by Goux *et al.*[78] in 2011, a CuTe electrode helped improve the performance of TS devices. Due to larger Cu-Te bonding energy, Cu ions preferred to diffuse back to the active electrode when removing the external electric field, which could impair filament stability. An optimum composition range was determined considering thermal stability and surface morphology[79]. Based on a similar mechanism, Banerjee *et al.*[80] used AgTe alloys as the active electrode and obtained higher endurance >10^9 cycles (Figs. 4(k) and 4(l)). Later, Wan *et al.*[81] prepared AgGeSe compounds as the top electrode and achieved the highest on-current density ~12.7 MA/cm^2 in the CF-based TS device (Figs. 4(m)–4(o)). Different from active electrodes, the inert electrode has a relatively indirect impact on the characteristics of CF selectors. Grisafe *et al.*[82] investigated the influence of inert metal work function on the threshold voltage. The work function difference between top and bottom electrodes could induce a built-in electric field, which could offset external bias. The V_{th} value increased as the work function of the inert electrode decreased. This effect offers a method to modulate the operating voltage of CF-based selectors.

Secondly, the interface between the electrodes and dielectric layer can be modified to improve device performances. According to the working mechanism of CF-based selectors, the interfaces greatly affect the redox reactions, charge transfer and ion migration. In the traditional active electrode/dielectrics/inert electrode structure, the oxidization and migration processes of active atoms are highly stochastic and the injection amount of active metal atoms is hard to control. Hence, a barrier layer is always inserted into the interface between the active electrode and dielectric layer to block active metal atoms. The most commonly used materials are TiN[27] due to the high impermeability. Figs. 5(a)–5(d) show performances of the Ag/TiN/HfO_2/Pt device established by Grisafe *et al.*[82]. The stuck-on issues were solved and endurance was improved with the adoption of diffusion barrier. The thicker TiN layer caused higher forming voltage (Fig. 5(b)), which indicated that a proper injection amount of active metal atoms was important for performance improvement. Although the TiN barrier layer can effectively block the active atoms, it is still challenging to control the size and distribution of filaments precisely. Thanks to the unique characteristics of 2D ma-

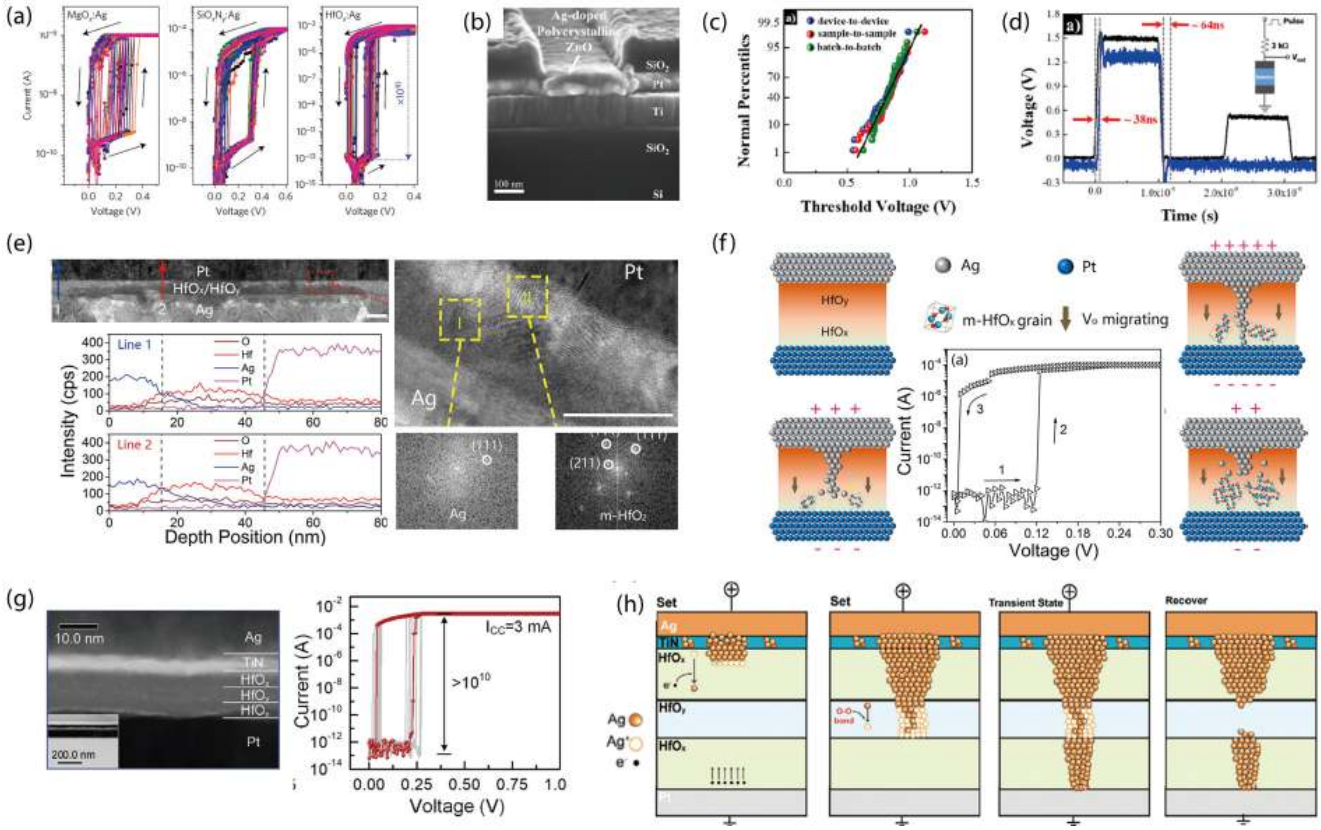

Fig. 6. (Color online) Performance enhancement of CF selectors from dielectric engineering. (a) Repeatable highly nonlinear threshold switching *I*–*V* characteristics for devices with different host lattices doped with silver. (b) Cross-sectional SEM image of the Pt/Ag:ZnO/Pt selector device. (c) Normal probability plot of Vth variation for selector devices in the case of device-to-device, sample-to-sample and batch-to-batch. (d) Transient characteristics of the selector devices with AC pulse test showing switching speed and relaxation time. (e) Cross-sectional TEM images and composition results of the Ag/HfO_y/HfO_x/Pt selector. (f) Schematic demonstration of the coupling mechanism between crystallite kinetics and Ag filaments. (g) Cross-sectional TEM image and DC *I*–*V* characteristic of the HfO_x/HfO_y/HfO_x selector. (h) Schematic illustrations of the proposed TS model. Reproduced with permission from (a) Ref. [45] Copyright 2017 Springer Nature, (b–d) Ref. [84] Copyright 2021 IEEE Publishing, (e, f) Ref. [87] Copyright 2018 ACS Publishing, (g, h) Ref. [86] Copyright 2022 Wiley-VCH.

terials, Zhao *et al.*[83] used defective graphene to have a better control of the filament formation process. As shown in Fig. 5(e), the control device Ag/SiO_2/Pt transformed into nonvolatile memory at an I_{CC} larger than 100 μA. The Ag/concentrated-defect graphene (CDG)/SiO_2/Pt device exhibited nonvolatile behaviors at a relatively low current (1 μA). However, the device with discrete-defect graphene (DDG) could maintain volatility at current up to 500 μA. Besides, the device could exhibit bidirectional switching characteristics.

Thirdly, the optimization of the dielectric layer is also an effective strategy since the cations migrate and react inside this layer. Plenty of methods can modify the microscopic structure of the dielectrics. For instance, doping is a common method. Yoo *et al.*[44] doped amorphous Si with hydrogen in an Ag/a-Si/Pt device. Hydrogen not only removed sneak paths in amorphous Si but also enhanced Ag diffusivity, which induced lower off-current and higher hold voltage. To realize bi-directional switching, active metal atoms are often directly doped into the dielectric layer as ion reservoir, as shown in Fig. 6(a). In this way, both positive or negative voltage can induce filament formation. Recently, Sahota *et al.*[84] achieved highly reliable selection behavior with controlled Ag doping of nano-polycrystalline ZnO layer (Fig. 6(b)). 0.01 pA of leakage current was obtained and at the same time, C2C and D2D variation of V_{th} was less than 10% (Figs. 6(c) and 6(d)). The reduced variations were attributed to anisotropic diffusion of Ag ions in the well-developed preferred *c*-axis oriented (002) crystalline ZnO (wurtzite) phase, in addition to restricted Ag ion influx modulated by doping. Multilayer structure is another simple and effective method. In a study of back-end-of-the-line (BEOL) compatible selectors, Luo *et al.*[85] inserted an undoped HfO_2 layer into a Cu/Cu:HfO_2/Pt device. The tunneling layer reduced the leakage current by more than 5 orders of magnitude, which could greatly increase the array density. Yin *et al.*[87] constructed homogeneous bilayer oxide TS device Ag/HfO_y/HfO_x/Pt where $x < y$, as shown in Fig. 6(e). The device exhibited electroforming-free properties, low threshold switching voltage of ~0.28 V, high on-current of ~300 μA, and extremely sharp switching slope of ~0.6 mV/dec. The coupling mechanism between crystallite kinetics of the homogeneous interface and the evolution of Ag CFs was revealed (Fig. 6(f)). Migration of oxygen vacancy (V_O) induced not only phase transformation of hafnium oxide from amorphous to monoclinic but also the rotation of grains, which interfered with the bonding strength of Ag filaments, assisted the evolution of Ag filaments, and generated selective effect. Heterogeneous bilayer oxides with different ion mobility are also proposed and exhibit good threshold switching characteristics, for example, Cu/GeTe/Al_2O_3/Pt[28]. More recently, tri-layer homogeneous oxides of HfO_x/HfO_y/

HfO_x ($x<y$) were reported by Lu *et al.*[86], showing high non-linearity >10^{10} and high on-current up to 3 mA (Figs. 6(g) and 6(h)). It was revealed that the discrete O–O bonds existed in the oxygen-rich HfO_y layer, which could oxidize Ag atoms and result in weak filaments. The filament formation and rupture mainly happened in the HfO_y layer and the interfaces between dielectrics could impair filament stability, which helps to increase the on-current.

Herein, we have discussed many effective methods for performance improvement and some devices exhibit quite satisfying characteristics. However, CF-based selectors are still far from industrial application. Poor uniformity limits the operation accuracy in a dense crossbar array. As filaments rupture spontaneously, the turn-off speed (hundreds of nanoseconds) is relevantly slow compared to RRAM. Endurance is also not sufficient to match with RRAM since excess active metal atoms can easily cause stuck-on issues. Another challenge is the fabrication process. Although some methods mentioned above can improve performance greatly, they are not efficient and suitable for wafer-scale fabrication, such as nano-dots and defective graphene. High-quality selectors with compatible materials and simple structures are still demanded.

3.1.2. OTS selectors

OTS selectors usually provide large on-current I_{on} to drive the phase transition in PCRAM cells, in which the current should be large enough to heat and melt the phase-change material. Meanwhile, the highly densified 3D structure requires large selectivity and low I_{off} as well. Besides the above critical parameters, an applicable OTS selector should present high endurance (several times more switching cycles than PCRAM materials), comparable switching speed to the PCRAM cell, and high stability to sustain high temperature in the BEOL process. To this end, the chalcogenide materials which contain S, Se, and Te elements stand out due to their excellent performance and full compatibility to PCRAM materials[88, 89]. The doped chalcogenide glasses with high crystallization temperature remain amorphous when the electrical current breaks down. Strong covalent elements typically forming tetrahedral sp^3 bonds (C, Si, As, *etc.*) are usually favorable to be added in the chalcogenides because the mixed amorphous alloys are rendered low fragility and slow crystallization rate.

The thermal stability of binary Ge_xSe_{1-x}-based selectors can exceed 350 °C, and V_{th} can be adjusted by changing the thickness and compositions. The device shows the high on-current density of 23 MA/cm^2 with a fast-switching speed of 2 ns and withstands 10^8 writing cycles. However, the I_{off} and selectivity are still not satisfactory. To this end, Navarro *et al.*[91] fabricated the Ge-rich Ge–Se compounds by co-sputtering of Ge and $Ge_{30}Se_{70}$ targets. In principle, the increase of Ge content results in more defect states, which can be easily excited by electric fields[110, 111]. The $Ge_{58}Se_{42}$ selector showed an improved selectivity (~10^5), low I_{off} (<10^{-10} A), and good device endurance up to 10^9. But the switch speed (~50 ns), J_{on} (1.5 MA/cm^2), and V_{th} (3.4 V) remain insufficient. It was demonstrated that the performance of the Ge–Se OTS device could be tailored by changing the stoichiometry and there was a trade-off between V_{th} and the crystallization temperature (T_c)[90]. To break the performance limit of Ge–Se materials, the strong covalent dopants[92–96] such as N, C, and As were used to enhance the amorphous network and further increase T_c. For example, N doping could both reduce I_{off} and improve the thermal stability (up to 600 °C). Addition of N will introduce strong Ge–N bonds to replace the homopolar Ge–Ge bonds, enhancing the barrier to break these bonds and weakening the diffusion of elements. The Ge–Se–N OTS device[92] shows low I_{off} (2 nA), high selectivity of 10^5, high on-current density of 23 MA/cm^2, and endurance of 10^8 cycles. The As-doped Ge-Se appears to be more balanced in all parameters. Ab initio simulations found that As ions can act as donors to pump electrons to the shallow states which originate from the nonbonding electrons in the defective tetrahedral clusters. The Ge–Se–As device presented J_{on} of 11.1 MA/cm^2, V_{th} of 2.5 V, and selectivity of 10^6 (as shown in Figs. 7(a) and 7(b))[93].

Te-based glasses are also one of the most developed materials family, such as $GeTe_4$[108], $GeTe_6$[97], B–Te[105], and C–Te[109], showing large on-current density (J_{on} >10 MA/cm^2), relatively large selectivity (I_{on}/I_{off} >10^5), and ultrafast switching speed (several nanoseconds). The first Te-based selector material $GeTe_6$, unfortunately, has poor thermal stability with low crystallization temperature (T_c) of ~300 °C and the phase separation issue is rather prominent after several hundreds of cycles. Reducing the content of Te and adding Si into compounds could improve thermal stability due to the formation of strong Si-Te bonds. Koo *et al.*[102] replaced Ge by Si, demonstrating a low I_{off} of 1 nA, high selectivity of 10^6, and fast switching speed of 2 ns. But at high temperature around 300°C, the leakage current will increase by one order of magnitude. Alternatively, $C_{0.35}Te_{0.65}$, $B_{0.25}Te_{0.75}$ and $Al_{0.3}Te_{0.7}$ selectors[104–107] also present good selectivity (>10^5) and low I_{off} (<5 nA). The thermal stability of C–Te and B–Te based devices can reach up to 450 °C, but they suffer from low V_{th} (~0.7 V) and insufficient endurance (< 10^8). Figs. 7(c) and 7(d) shows the thermal stability of several Te-based binary OTS devices. The high-entropy-like materials such as Ge–As–Te–Si and Ge–As–Te–Si–N OTS materials[98–101] could overcome the above drawbacks. It made the As-contained materials the state-of-the-art OTS selectors in modern 3D phase-change memory products. However, the alloying of As is not environment-friendly and they also suffer from the chemical composition complexity which are not compatible with CMOS lines.

Recently, Shen *et al.*[110] reported a single-element tellurium (Te) OTS device, exhibiting large J_{ON} (>11 MA/cm^2), fast switching speed (<20 ns), and high endurance (10^9 cycles), as shown in Figs. 7(e) and 7(f). In-situ HRTEM investigations were carried out for monitoring the switching process of the TiN/Te/TiN devices, and the crystalline-liquid-crystalline phase transition mechanism was confirmed in the pure elemental-Te switch. It was demonstrated that the device performance matched well with those of GST-based PCRAM cells, which did not deteriorate severely after series connection with PCRAM cells. The intrinsically homogeneous composition and BEOL compatibility of the Te device not only cut the time-consuming material-optimization process but also enable aggressive size downscaling toward sub-10-nm dimensions for realizing 3D memory chips with the highest density. Hence, simplifying the composition as well as new device structures becomes the next battlefield for the OTS research.

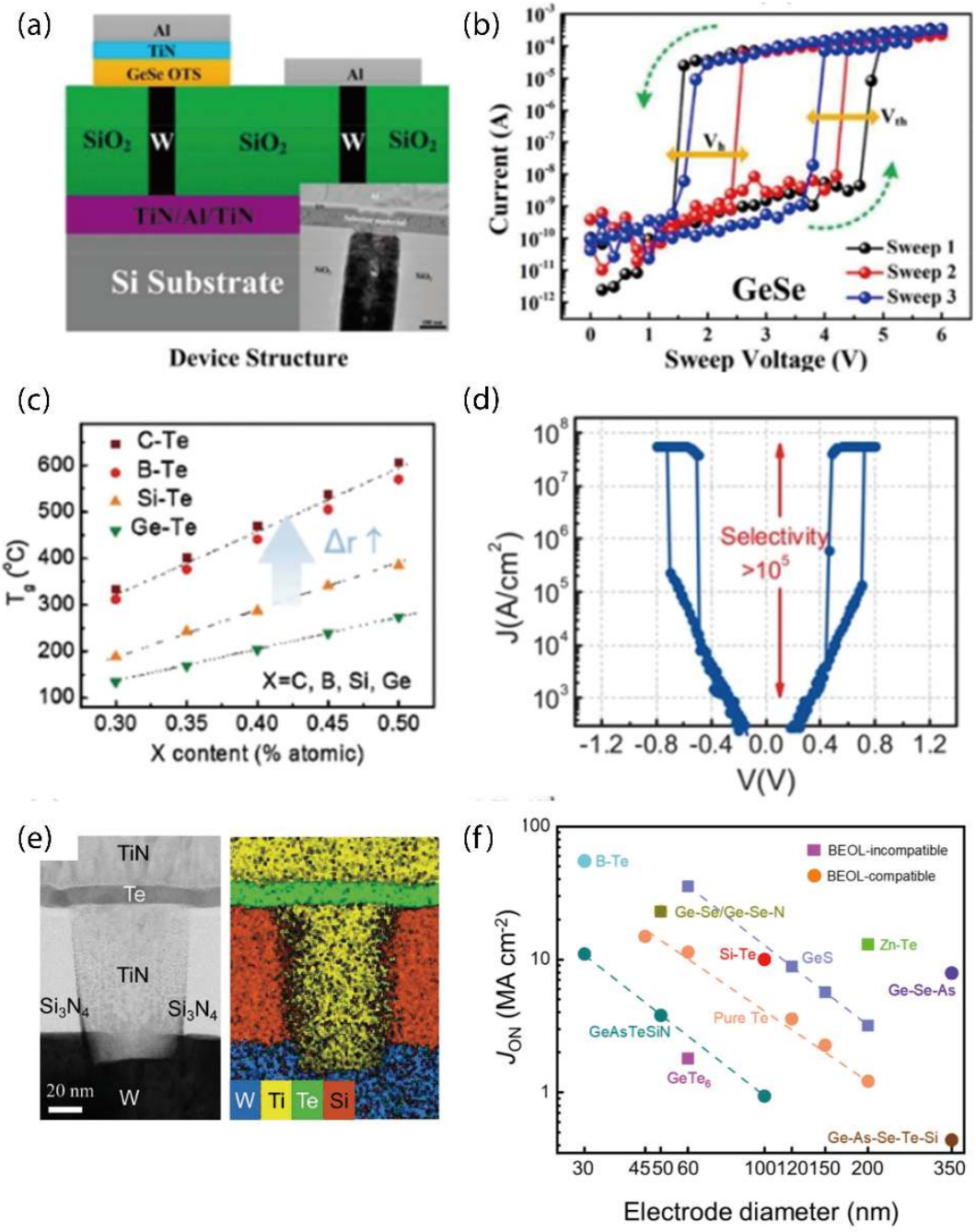

Fig. 7. (Color online) Te-based and GeSe-based OTS selectors. (a) Schematic of the TiN/Ge-Se/W device structure in an As-doped GeSe OTS selector. (b) The OTS *I*–*V* curves of the GeSe-based device. (c) Four Te-based OTS materials show good thermal stability. (d) The *J*–*V* characteristics of the W/C-Te/W device with good selectivity of >10^5. (e) Cross-sectional TEM images of single-element Te device. (f) J_{ON} parameters versus electrode diameter in various OTS devices. Reproduced with permission from (a, b) Ref. [104] Copyright 2018 IEEE Publishing, (c, d) Ref. [93] Copyright 2019 ACS Publishing, (e, f) Ref. [110] Copyright 2021 Science Publishing.

3.1.3. MIT selectors

Although MIT devices have a fairly high on-state current (>1 mA) and relatively high endurance (>10^8), small on/off ratio (~100) limits their developments in the selector field. Meanwhile, VO_2, one of the main MIT materials with a transition temperature of only 341 K possesses poor thermal stability. The other main material, NbO_2, has multiple oxidation states[112] limiting the NbO_2-based MIT selector.

Many efforts have been made to improve the performance of MIT devices. One reliable option is doping such as Al and Ti elements[113–115]. Metal impurities help to decrease the leakage current. They also induce oxygen vacancy pathways in the electroforming process, which improve the uniformity. In addition, the precise control of the oxygen content in the film can also help performance enhancements of NbO_x-based MIT devices. Luo *et al.*[116] and their subsequent work[117] performed an in-depth study on the effect of oxygen flux in magnetron sputtering, and achieved extremely high endurance (~10^{12}), fast switching speed at the level of 10 ns, and large on-current density (4.8 MA/cm^2).

In summary, the three types of selectors have distinct characteristics. CF-based selectors have the highest selectivity

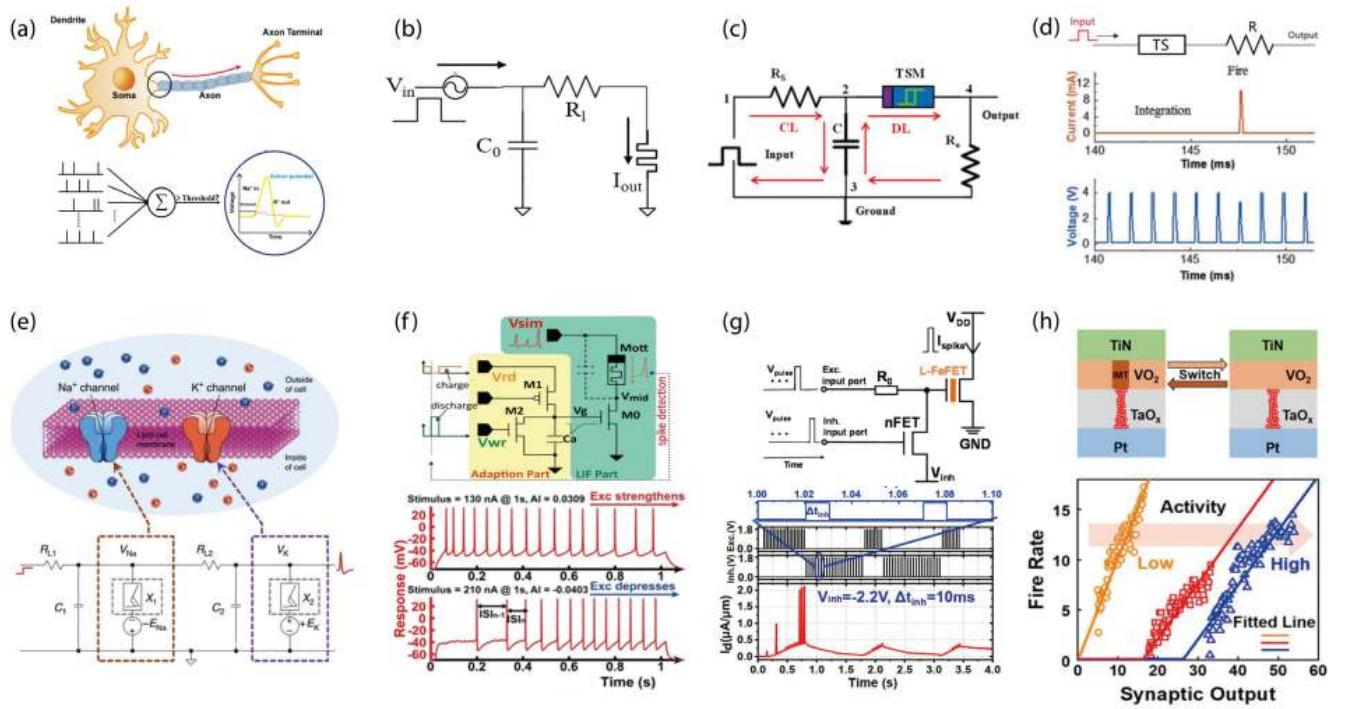

Fig. 8. (Color online) (a) Schematic diagram of biological neurons. Presynaptic currents are integrated in neurons. When the membrane potential reaches a certain threshold, an action potential is generated. (b) The circuit of LIF neuron. The capacitor acts as the membrane and implements integration effect via the charging process. The resistor is used to limit the current through the VO_2-based MIT device, which is the output signal of the neuron. (c) LIF neurons with voltage spike output. (d) Neurons based on single volatile TS memristors and its voltage input and current output. (e) HH neurons based on two VO_2 devices, detailed simulation of biological neuronal cell membrane ion channels with over 30 neural dynamic characteristics. (f) The device used to achieve neuron intrinsic plasticity and the frequency of the output spike of this neuron versus the strength of the presynaptic input signal. (g) FeFET-based LIF neurons with inhibitory synaptic inputs, and their pulse input and output signals. (h) LIF neuron circuit with spiking frequency adaptation, and the output spiking waveform (frequency becomes stable over time). Reproduced with permission from (b) Ref. [122] Copyright 2016 IEEE publishing, (c) Ref. [123] Copyright 2017 IEEE publishing, (d) Ref. [124] Copyright 2018 Wiley-VCH, (e) Ref. [127] Copyright 2018 Springer Nature, (f) Ref. [129] Copyright 2021 IEEE publishing, (g) Ref. [130] Copyright 2019 IEEE publishing, (h) Ref. [131] Copyright 2022 IEEE publishing.

and lowest leakage current, which are promising for 1S1R memory technology, but they have the poorest endurance and uniformity due to the intrinsic stochasticity, which greatly limit the applications. Improvements of endurance and on-current are still in development. OTS selectors have very high compatibility with PCM devices, but the selectivity and leakage current have to be improved. The advantages of MIT selectors are fast switching speed, but they have the smallest selectivity. Devices with CMOS compatible materials and simple structures should be considered to reduce fabrication cost. In addition, co-design of selector and memory should be paid more attention because an inappropriate match can cause severe performance degradation.

3.2. Neuromorphic computing

3.2.1. Artificial neuron

With the restriction of the von Neumann bottleneck and the ending of Moore's law, search for advanced computing technologies is in high demand. Therefore, brain-inspired neuromorphic computing technologies with non-von Neumann architectures appear and play important roles in AIoT systems. They attract much attention from industry and academia owing to its parallel computing capability and lower energy consumption. Hardware implementation is an important step during the development of neuromorphic computing. Among various nueromorphic devices, artificial neuron is one of the crucial issues.

In a biological system, as shown in Fig. 8(a), dendrites work as the input of the neuron which receive and integrate the signals from other neurons through the synapses, while the axon works as the output of the neuron, connected with the dendrites of the nearby neurons through synapses[118]. To describe the behavior of neurons, many mathematical models have been established, such as integrate-and-fire (IF)[119], leaky integrate-and-fire (LIF) and Hodgkin–Huxley (HH) model[120]. The HH model systematically describes the dynamic behavior of the membrane potential in terms of various ion channels of the soma and dendrites, which is very complicated for hardware implementation. The IF model, however, gives a concise description of biological behavior, *i.e.* the neuron receives input from the presynaptic neuron and then generates excitatory or inhibitory postsynaptic currents. The membrane potential will gradually increase and the action potential is triggered when the membrane potential reaches a threshold value. The LIF model solves the problem that the membrane potential keeps constant when the input is withdrawn, which is contrary to the actual biological behavior. Thus, the LIF model is widely applied in the current SNN.

Artificial neurons based on CMOS circuits suffer from problems like low integration density and high power consumption[121]. Fortunately, the introduction of volatile memristive devices greatly simplifies the circuits and improves efficiency

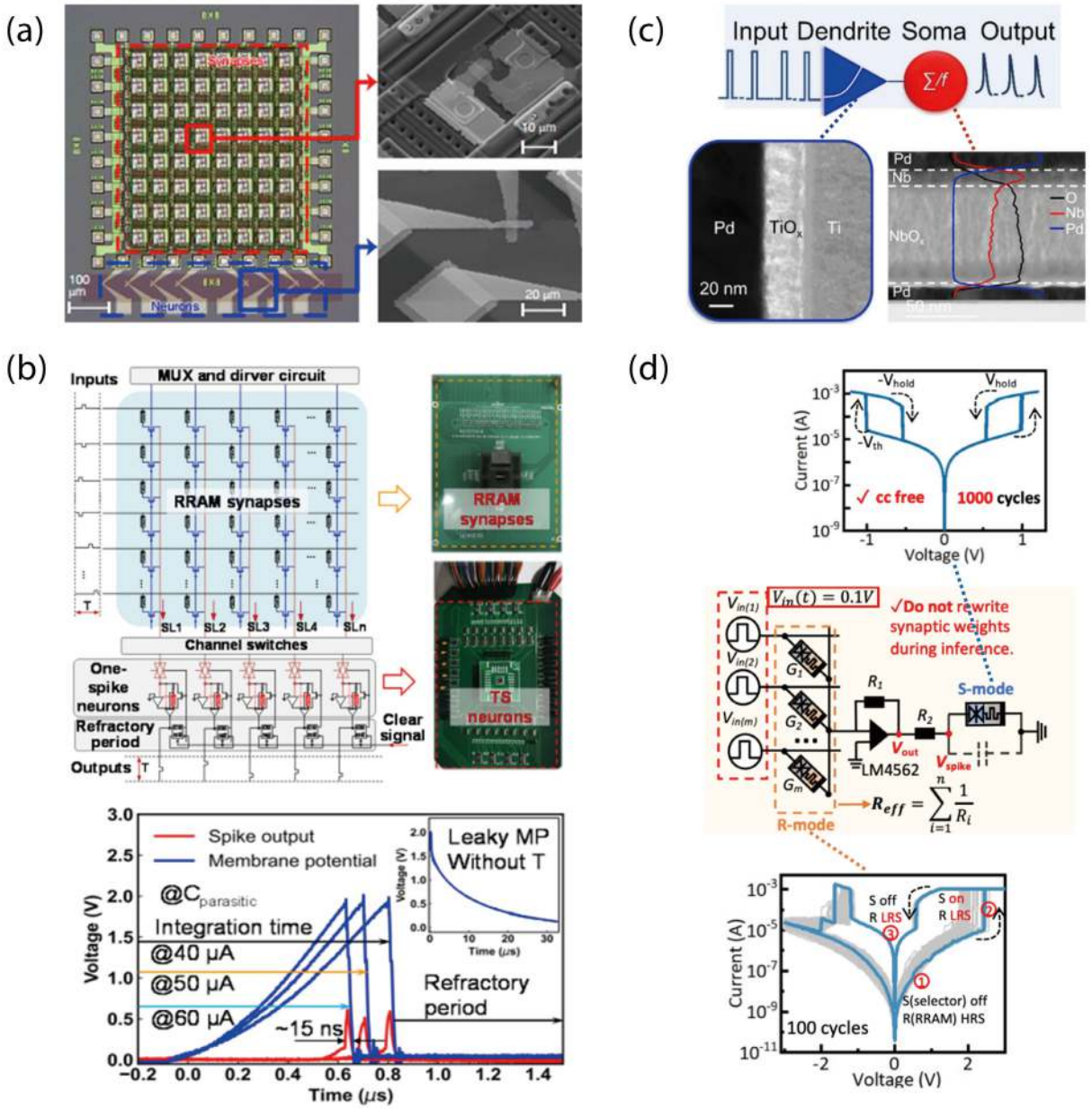

Fig. 9. (Color online) (a) An 8 × 8 artificial neural network integrated by Pt/HfO$_x$/Pd non-volatile memristors and Pt/Ag/SiO$_2$:Ag/Ag/Pt MCF-TS memristors. (b) Schematic of the constructed fully memristive Temporal Coding 256 × 5 SNNs and the hardware implementation. (c) Artificial neuron integrated with dendrite and soma, where Pt/TiOx/Ti volatile memristor is used as dendrite and Pd/NbO$_x$/Nb/Pd MIT device is used to generate action potential. (d) A simple neural network demonstration, using the same device in the synaptic and neuronal parts, and showing *I*–*V* sweeping operating in resistive switching mode and threshold switching mode, respectively. Reproduced with permission from (a) Ref. [138] Copyright 2018 Springer Nature, (b) Ref. [143] Copyright 2022 Wiley-VCH, (c) Ref. [141] Copyright 2020 IEEE publishing, (d) Ref. [144] Copyright 2022 Wiley-VCH.

due to their similar properties with the biological neuron. In 2016, Lin *et al.*[122] demonstrated an LIF neuron using VO$_2$-based MIT device, which is integrated in series with a resistor and in parallel with a capacitor (Fig. 8(b)). The capacitor acted as the membrane and achieved integration effect via the charging process, while the resistor was used to limit the current across the MIT device. When the membrane potential reached the threshold, the neuron would output current spikes. Later, the neurons were modified to achieve voltage spiking output (Fig. 8(c))[123]. To establish neurons with low energy consumption, CF-based TS devices of Ag/FeO$_x$/Pt[124] were employed to construct a compact artificial neuron without peripheral circuits due to its ultra-low I_{off} and ultra-narrow pulse tunability (Fig. 8(d)). Recently, Cao *et al.*[125] proposed $Hf_{0.2}Zr_{0.8}O_2$ anti-ferroelectric film to achieve neurons with low energy consumption (37 fJ/spike) and high reliability (>10^{12} cycles). The above LIF neurons can achieve at least three basic functions: membrane potential leakage and integration, threshold-excited spiking action potential, and an input-modulated output spike frequency. Nevertheless, they do not characterize in detail the intrinsic properties of biological neurons. Thus, Pickett *et al.*[126] reported an HH neuron using two NbO$_2$-based devices as ion channels of biological neurons. Subsequently, further optimization was made by Yi *et al.*[127] where the neuron possessed all three types of excitability and almost all biological neuronal dynamics (Fig. 8(e)). These

years, more attention is focused on modifications of the LIF model to achieve more biological neuron functions with lower hardware cost and energy consumption. Liu *et al.*[128] achieved output frequency adaption (homeostasis function) by connecting an analog memristor under the influence of continuous input pulses in series to the neuron circuit. Later, Wei *et al.*[129] reported the similar function more reliably using an additional transistor circuit (Fig. 8(f)). With continuous pulse stimulation, the output spike frequency will stabilize at a constant value. Compared to LIF neurons without frequency adaption, the recognition accuracy was improved by 3 percentage points in the simulation based on MNIST dataset. Luo *et al.*[130] added an inhibitory pulse input by using a transistor as a voltage controlled leaky channel in FeFET-based LIF neurons, as shown in Fig. 8(g), resulting in an accuracy of 93% in the network simulation. Most of the above optimization efforts rely on external components, which is clearly detrimental to the circuit area. Wu *et al.*[131] proposed a combined device, as shown in Fig. 8(h). It consisted of a TaO_x non-volatile memristor and a VO_x volatile threshold switching memristor. By regulating the conductance of TaO_x layer, it was possible to modulate the excitation threshold of the neurons. Wang *et al.*[132] reported a similar scheme where the delay of the output spike relative to the input pulse could be modulated by changing the initial state of the device. It is important to maintain the accuracy of the entire network even when some of the synapse devices suffer from stuck-on failures.

3.2.2. Fully memristive neural network

Artificial neural network arrays based on memristive synapse devices and CMOS neurons have been widely reported[133–136], and even the corresponding chips have been produced[137]. However, in order to achieve high density and high efficiency, fully memristive neural networks are still demanded. In 2018, Wang *et al.*[138] realized fully memristive neural networks employing volatile and non-volatile memristors, as shown in Fig. 9(a). The neuron consisted of an CF-based TS memristor and a capacitor in parallel to implement a simple LIF function. Duan *et al.*[139] and Li *et al.*[140] also demonstrated the inference process of small-scale memristive neural networks. These works demonstrated the potential of memristive neural networks for unsupervised or supervised learning and pattern classification compared with CMOS solutions with a large number of transistors, but it also left several questions.

The first and foremost problem is the power consumption of the hardware network, although volatile TS memristor-based neurons have advantages in terms of area and energy consumption compared to CMOS circuits, facilitating large-scale integration. Zhang *et al.*[141] exploited the feature that the first output spike of a neuron has different delays under different input signal strength to change the common spiking frequency coding to the first spike arriving time coding. Only the first excitation spike is valid, and all other outputs will be suppressed, which is also consistent with synaptic spiking-time-dependence-plasticity (STDP), as shown in Fig. 9(b). Both Wang *et al.*[142] and Li *et al.*[143] took the approach of filtering the tiny signals, which means that only the strong enough signals can excite neurons. Among them, Li *et al.*[143] used TiO_x-based volatile memristors as dendrites instead of the common parallel capacitor or parasitic capacitance of neural components to filter out the weaker presynaptic current, as shown in Fig. 9(c). The energy consumption is only 5.6% of the GPU while processing the same task. By avoiding the accumulation of unimportant current information on neurons, this scheme not only improves the energy efficiency of the whole neural network, but also improves the recognition accuracy.

Nevertheless, it is worth noting that the above fully memristive neural networks use at least 2 or even more than 2 types of memristors, which inevitably brings some problems such as the interaction of multiple materials and the mismatch of different kinds of devices. Moreover, the above memristive neural networks only demonstrated the inference process of single layer network without afferent neurons, have not addressed the question of whether afferent neurons and interneurons' output spikes can drive postsynaptic devices. Thus, heterogeneous integrated neural networks using different kinds of devices may have lurking perils in terms of synergy. The brand-new V/$HfWO_x$/Pt memristor proposed by Fu *et al.*[144], as shown in Fig. 9(d), can work in both non-volatile resistive switching mode and volatile threshold switching mode, so it can be used as a synaptic device or to construct artificial neurons. Yu *et al.*[145] also reported similar homogeneous integration schemes, which effectively solves the mismatch of device parameters and improves the reliability of the entire hardware network. Of course, there are still many problems limiting the development of fully memristive neural networks, including slight changes in the conductance of synapse devices under the influence of continuous output spikes from anterior neurons, and degradation of neuron devices under the continuous stimulation of presynaptic current, etc. Therefore, the road to fully memristive neural networks has a long way to go.

3.2.3. Artificial sensory neuron

The sensory system is an important part of AI, for example, ANN can be used for real-time image processing and pattern classification in the field of autonomous driving, robotics, *etc.*[146,147]. But traditional AI sensory system relies on complex sensors, signal processing circuits, processors and memory, which means a lot of energy is consumed while processing real-time external information at excessive hardware cost[148]. It's clearly detrimental to the edge devices of the IoT for real-time information processing.

Fortunately, volatile TS memristor based sensory neurons can encode external information into spikes, which can be directly exploited by SNNs, helping system reduce unnecessary power consumption[22, 149–158]. In fact, many sensory spiking neurons, some also called nociceptors, have been currently reported to respond to external stimuli, including mechanical force[156–158], light[152], heat[154], curvature[157], etc. Examples of neurons that can perceive mechanical forces, light and heat are shown in the Figs. 10(a)–10(c). Interestingly, their circuit structure is almost similar to that of the previously reported LIF model spiking neurons. The difference is that the resistor originally connected in series with the neuron is replaced by a tunable resistor that can be adjusted by different stimuli, which will result in different output spiking frequency response from the neuron depending on the voltage division between the sensory resistor and the neuron device under a fixed input voltage amplitude. These works usually re-

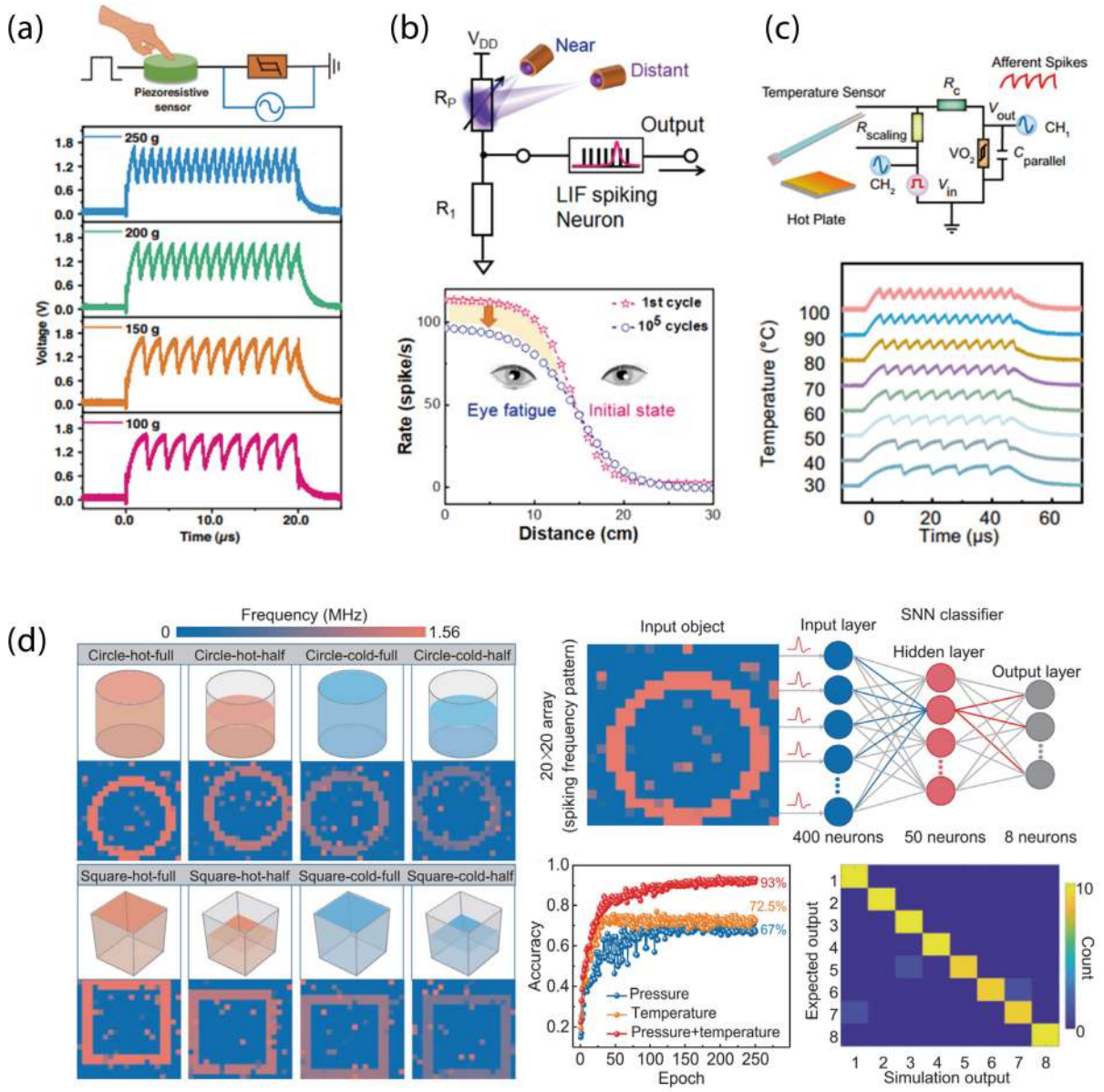

Fig. 10. (Color online) (a–c) The environmental input signal are mechanical force, light, and heat, respectively. The sensory neurons, and their output signal characteristics are also shown. Essentially, the load resistors of the common LIF neurons are replaced with various types of sensing resistors. (d) A 20 × 20 sensory neuron array for object classification simulation, which shows 8 objects with different shapes and temperatures, having 400 afferent neurons, 50 hidden layer neurons, and 8 output neurons. The final result is a reliable classification. Reproduced with permission from (a) Ref. [154] Copyright 2022 Wiley-VCH, (b) Ref. [152] Copyright 2022 Wiley-VCH, (c) Ref. [157] Copyright 2022 Springer Nature, (d) Ref. [158] Copyright 2022 Wiley-VCH.

quire an additional power supply, which has to occupy a certain area and generate static power consumption. Zhang *et al.*[156] and Song *et al.*[155] solved this problem in force-sensing neurons and heat-sensing neurons by using piezoelectric nanogenerator and thermocouple, respectively. However, as a simulated human sensory system, sensory neurons at this stage tend to be used as nociceptors, *i.e.* the spiking responses are available as soon as the stimulus input, which corresponds to the stimulus maladaptation of biological sensory neurons. In fact, humans can adapt to a certain intensity of external stimuli without reacting. Moreover, current visual neurons can only respond to light intensity, and then when it comes to image recognition or spatial perception tasks, neurons that can only process one-dimensional information are more than adequate. Therefore, it is necessary to urgently develop sensory neurons with richer functions, better perception ability and more comprehensive perceptual information.

As a kind of afferent neuron, current works have demonstrated their ability to convert analog signals into SNN-applicable spikes, but relative reporter, which demonstrates sensory neurons with SNN synaptic devices as well as output neurons, is rare. Zhu *et al.*[158] showed a small in-sensor computing network at the simulation level that allows accurate recognition of the shape, weight, and temperature of objects, as shown in Fig. 10(d). However, there is still no hardware level demonstration, which we think is the inevitable trend of future development. While there is certainly the same difficulty of integrating different hardware together as in FHMNNs, some solutions to help the FHMNNs implementation have been proposed in the previous section, which can be a guideline for implementing in-sensor computing at the hardware level.

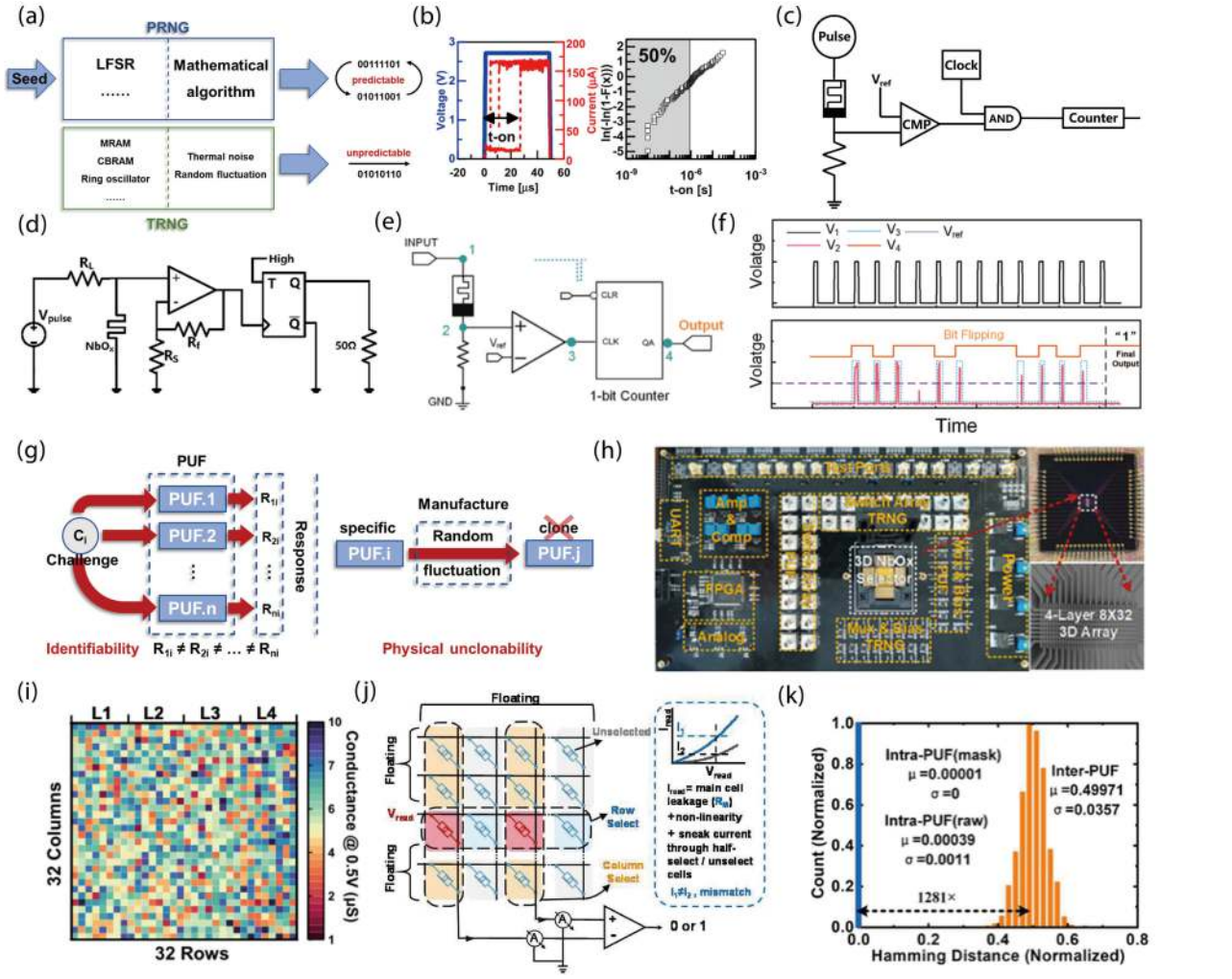

Fig. 11. (Color online) (a) Schematic illustration of TRNG and its difference with PRNG. (b) OTS-based TRNG using the Weibull distribution of on-time to generate random bits. (c) One of the mainstream TRNG structures containing comparator, AND, clock and counter. (d) NbO_x-based TRNG circuits. (e) The circuit design of a recent reported TRNG based on CF-TS devices. (f) 15 excitation pulses are applied to the diffusive memristor (V_1). The stochastic fire spikes (V_2) are sent to a comparator and will induce the random number of voltage pulses at node 3 (V_3). V_3 will be then sent to a one-bit counter as the clock signal. The output of the one-bit counter represents the odd or even of the fire spikes. "1" and "0" represent that the numbers of fire spikes are ODD and EVEN, respectively. (g) Demonstration of the basic conception of PUF. (h) Hardware implementation of the PUF. (i) Read-conductance of each device at 0.5 V in the array. (j) Operation principle of the PUF in the array. (k) The uniqueness (inter-PUF) and reliability (intra-PUF) performances of the TS-based PUF. Reproduced with permission from (b) Ref. [159] Copyright 2019 IEEE publishing, (c) Ref. [160] Copyright 2017 Springer Nature, (d) Ref. [163] Copyright 2021 Springer Nature, (e, f) Ref. [81] Copyright 2022 Wiley-VCH, (h–k) Ref. [164] Copyright 2021 IEEE publishing.

3.3. Hardware security

With the rapid development of AIoT, massive privacy information and encrypted data is stored and communicated in the edge. How to protect the data with low cost becomes a serious problem. Hardware-intrinsic security primitives such as true random number generator (TRNG) and physical unclonable function (PUF) units can be the solutions, which recently attract great attentions. Many researchers have proposed various devices (SRAM, STT-MRAM, RRAM) to achieve TRANG or PUF. Among them, random raw noises are used as an entropy source, and then a post-processing circuit is combined to generate random signal. These methods suffer from the problem of high energy consumption and large device area, which is not appropriate for the edge devices. The volatile TS memristors feature intrinsic stochasticity, high density and low energy consumption, which have great potential to break the dilemma. Consequently, volatile TS memristor-based TRNG and PUF becomes promising hardware security primitives of the AIoT system and deserve in-depth explorations.

3.3.1. True random number generator

As shown in Fig. 11(a), random numbers generated by PRNG are driven by mathematical algorithms. Though the very-long-period pseudo random sequence could be designed, it is still predictable due to the defect of algorithm and the social engineering attack. Instead, TRNGs are driven by random parameters, such as thermal noise, random oscillations, *etc*. These random parameters are usually derived from the physical mechanism of the device, or the oscillator. It produces an unpredictable and fully random sequence.

The inherent variability in threshold voltage results in a bimodal distribution of on/off states which can be easily converted into digital bits. Chai *et al.*[159] found that the GeSe-based OTS device had an equal probability in on or off states

Table 2. Comparisons of TRNGs based on different types of TS devices. "–" means that no such characteristic was found.

Device	Entropy source	Throughput (kb/s)	Energy consumption (pJ/bit)	Endurance	NIST test
TiN/GeSe/TiN [159]	Threshold voltage	1000	–	1×10^{11}	12 tests passed
Pt/Ag/Ag:SiO_2/ Pt [160]	Switching time	6	0.17	6×10^{7}	15 tests passed
Pt/HfO_2/TiN [161]	Switching time	6	–	–	8 tests passed
Pt/HfO_2/TiN [162]	Switching time	16	–	–	15 tests passed
Pt/Ti/NbO_x/Pt [163]	Oscillation time	40	5230	2.4×10^{7}	15 tests passed
$Cu_{0.1}Te_{0.9}$/HfO_2/Pt [74]	Switching time	32	–	–	15 tests passed
Ag/TiN/HfO_x/HfO_y/HfO_x/Pt [81]	Firing spiks	108	–	1×10^{6}	15 tests passed

when the amplitude and width of the applied voltage pulse was 2.7 V and 1 μs, respectively (Fig. 11(b)). Although a random bit stream of 0 and 1 can be generated, the TRNG approach owns few disadvantages. The method greatly depends on the exact distribution of the measured parameters (V_{th} or t_{on}), and the set threshold values (amplitude and width of pulse) must be based on amounts of statistical data, which easily induce inaccuracy if the sample size is not big enough. In addition, the poor D2D uniformity makes the determination of threshold values hard and leads to inaccuracy. To avoid the insufficiency, Jiang *et al.*[160] introduced the voltage-to-time conversion scheme and used switching time of diffusive memristors as entropy sources in their work (Fig. 11(c)). After that, the TRNG containing flip-flops or counters has gradually become one of the mainstream structures[161, 162]. Although the accuracy problem is solved, the generated random bit rate is too low to match with the computer system. To increase the throughput of TRNG, Kim *et al.*[163] reported a self-clocking TRNG based on the MIT device, as shown in Fig. 11(d). The randomness was processed by the T flip-flop and output as binary bits. The throughput was improved to 40 kb/s. Recently, Lu *et al.*[81] designed a TRNG based on Ag/TiN/HfO_x/HfO_y/HfO_x/Pt CF-TS device (Fig. 11(e)). The comparator sent a high-level output to the 1-bit counter when the voltage of firing spikes exceeded the reference value (Fig. 11(f)), and then the 1-bit counter flipped, which converted the number of even or odd firing spikes to random binary bits. The throughput was enhanced to 108 kb/s and passed the standard statistical test package developed by the National Institute of Standards and Technology (NIST). The entropy source, throughput, energy consumption, endurance, and NIST test of the TS-based TRNG works are listed in Table 2.

The three types of TS devices have different switching mechanisms, which make their own advantages and disadvantages in throughput, energy consumption, and endurance. Due to ultralow leakage current, CF-based TS devices are good at energy consumption control, while their throughput and endurance are limited by the slow switching speed and poor cycle endurance. In contrast, MIT devices have faster switching speed, which result in faster throughput. However, the thermal and phase instability of MIT materials (VO_x and NbO_x) block their endurance and reliability. As for OTS devices, they have relatively better switching speed and endurance, but bad power consumption control. There are some suggestions for TRNG performance enhancements from device perspectives. Firstly, if the application has higher requirements on the throughput, and attention should be paid to the switching time of the device, and the swing of the oscillation voltage (threshold voltage - hold voltage), which are negatively correlated with throughput, and thus, OTS and MIT devices will be more suitable. Secondly, when energy consumption is the crucial indicator of the application, CF-based TS devices are recommended for TRNG design. Meanwhile, the leakage current and operation current are also the main parameters to be considered, which are benefited to the control of energy consumption. Lastly, if the endurance is significant in the application, OTS and MIT devices are suggested to be used in design. And the pulse endurance of the device is very important, which is positively relevant to the TRNG endurance.

Considering the serial structure of the entropy source and post-processing circuit of the TS-based TRNG, there are also several details worth attention in terms of circuit design. The entropy source generation circuit is usually composed of TS devices, while the post-processing circuit is usually composed of CMOS-based digital or analog chips. Therefore, the speed and endurance bottlenecks of TS device-based TRNG mainly lie in the entropy source generation circuit, while the energy consumption limitation primarily lies in the post-processing circuit. Firstly, the throughput of the TRNG could be promoted by increasing the rate of operations that stimulate entropy source or by increasing the number of random bits generated per operation. Secondly, endurance could also be improved by increasing the number of random bits generated per operation. Lastly, if designers want to reduce the overall energy consumption of the TRNG, it is recommended to choose low-power chips or to reduce the size of the post-processing circuit. In summary, not any type of TS device is almighty for TRNG design. Different types of TS devices can bring different performance advantages such as low energy consumption, high throughput, and high durability in TRNG. Designers need to select devices according to actual application scenarios. In the future, performance breakthroughs of TS devices are also expected to push the developments of TRNG.

3.3.2. Physical unclonable function

For the information security, the digital data is protected through confidentiality and authentication technologies. The TRNG can work as a random key generator for the authentication, but these keys still need to be stored in digital memory, which could be dangerous. The PUF can solve the problem to act as both key generator and key storage. The basic concept of PUF is illustrated in Fig. 11(g). It takes advantage of the unavoidable fluctuation during the manufacturing process, which means there will not be two identical devices. In other words, a PUF is the fingerprint of a physic object. Mathematically, the configurable part of the PUF is generally called *challenge*, which can also regard as the input. The particular measurement of the physical state under a challenge is called *re-*

sponse. When a challenge is imposed on the PUF, each unit of the PUF will give a sub-response to the challenge. As the challenge changes, so does the response. There are slight technique differences in the manufacturing process, which makes it challenging to observe the topography differences of the device and reproduce the differences, and generate random fluctuations in the device performance. Even if fabricated with the same process parameters, it is almost impossible to manufacture a device with identical performance. Therefore, identifiability and physical unclonability are two core properties to be satisfied in PUF units.

Recently, PUF units based on volatile TS devices attract great attention due to the intrinsic stochasticity that the device can randomly switch to LRS or stay at HRS under a certain voltage pulse. Ding *et al.*[164] reported a PUF based on the MIT device, where the hardware system contained TS device array and peripheral circuits, as shown in Fig. 11(h). Fig. 11(i) exhibited a random distribution of the read-conductance at 0.5 V in a 32 × 32 array. According to the PUF operating principle in Fig. 11(j), the selecting signal of row-column pair is the challenge, and the current on each selected wire is the sum of main cell leakage, non-linearity, and sneak current through half-selected or unselected cells. Due to the random distribution of conductance, the respective sums of the read currents of the two columns were not equal. By comparing the current magnitudes of two selected columns with a comparator, a response corresponding to the challenge could be obtained. As shown in Fig. 11(k), the mean value of inter-die and intra-die Hamming distance is 0.49971 and 0.00039 respectively, which is close to the ideal value and the uniqueness of proposed PUF was verified.

There is a corresponding relationship between the performances of the PUF, such as uniformity, uniqueness, reliability, endurance, and strength, and the performances of TS devices, such as randomness of entropy source, C2C and D2D variation, endurance, and scale of the array. However, there are several problems to be solved for the TS-based PUF. Firstly, the array scale is still small, which makes challenge-response pairs (CRPs) too few to guarantee security. Secondly, due to the limited endurance of the TS device, it is hard to store the key for a long time. It might induce the response generated at the beginning to be different from that after several operations, which means it cannot be reproduced. Hence, improving the stability of the TS device and the scale of the TS array will be of significance for TS-based PUF applications.

3.4. Other applications

3.4.1. Steep subthreshold slope transistor

Metal oxide semiconductor field-effect-transistor (MOSFET) is an important type of electronic device in the large-scale integrated circuit industry. The power consumption becomes one of the main challenges as the dimensions scale down. To achieve high energy-efficiency in MOSFET, the transistor should have a steep subthreshold slope (SS = dV_g/dlogI_d, *i.e.* the gate voltage required to increase the drain current by ten times in sub-threshold regime, in the unit of mV/decade), low leakage current, and low working voltage. However, the sub-threshold slope of conventional MOSFETs is limited to 60 mV/decade due to the thermionic carrier injection mechanism. The lowest limit of SS value has caused to exponentially increase the off-state leakage current with monotonically decreasing the threshold voltage, and thereby, it is difficult to control the passive power consumption in integrated circuit and it also influence the further decrease of operation voltages. Several solutions have been proposed in the material and device community, including impact ionization MOSFET based on avalanche breakdown, tunnel FET based on band-to-band tunneling, hyper-FET based on the metal-to-insulator transition in VO_2[165–168]. Nevertheless, these methods either cannot achieve an ultralow subthreshold slope or demand high drain voltages. As listed in Table 1, the CF-based TS devices possess ultra-low leakage current and steep switching slope less than 1 mV/decade. Consequently, the configuration of CF-based TS device in series with the drain of the MOSFET is suggested to construct steep subthreshold slope transistors. Song *et al.*[169] connected a AgTe/TiO_2-based TS device in the series with the drain of a transistor in 2016 and the SS value of 5 mV/decade was obtained. The leakage current was also at a small value ~1 pA. After that, some other TS devices used for steep subthreshold slope transistor were reported successively, such as W/Cu_2S/W[170], Ag/HfO_2/SiO_2/p-Si[171], Ag/Ti/HfO_2/Pt[172]. However, all the above TS-based transistors exhibit the subthreshold slope at the level of ~5 mV/decade. It is still an urgent demand to further develop transistors with an ultra-steep subthreshold slope.

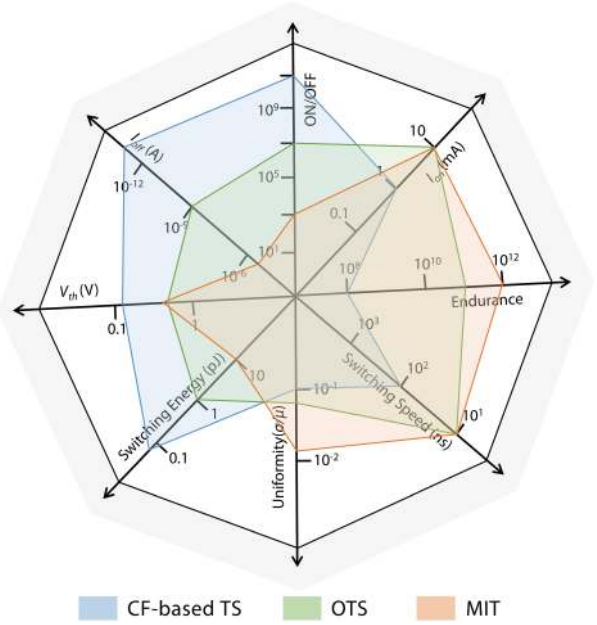

Fig. 12. (color online) Selected performance of three types of TS devices. The selected values are the maximum or minimum values of the performances in Table 1 from Refs. [75, 84, 86, 90, 93, 104, 116, 181, 183, 188, 189]. Switching energy is roughly estimated from voltage pulse measurements, $E = VIt$ where V and t are the amplitude and width of the applied voltage pulse, respectively, I is the current response to the pulse[27].

3.4.2. volatile memristor as logic device

Boole logic is part of the basic of digital circuit and the device realization of it is an important issue in electronics. In literature, non-volatile memristor devices are always used for Boole logic application. A recent study by Park *et al.*[173] revealed that the TS devices also could be used for realization of Bool logic. They fabricated Ag/HfO_x:N/Pt/Ti device to accomplish the AND and OR logic in a 2 × 2 array. The inputs are

the two separated voltages applied on the two TS devices, and the output is the voltage measured at the shared top electrode of the devices. The state "1" and state "0" represent that the voltage is 0.35 and 0 V separately. For AND operation, only if the input of the two devices are both "1" (0.35 V), will the output be state "1" (0.35 V). Unfortunately, only the functions of AND and OR logic were accomplished in this work. Realization of all the sixteen Boole logic function with TS devices is to be continued.

4. Conclusions and perspectives

Volatile threshold switching memristors play an import role in AIoT systems, enabling the entire processes of data and information collection, storage, analysis and communications. In the review, three types of TS devices are discussed in details from the views of materials, switching mechanisms and applications. The distinctive characteristics of CF-based TS, OTS and MIT devices are summarized in Fig. 12 including on/off ratio, leakage current (I_{off}), on-state current (I_{on}), threshold voltage (V_{th}), switching speed, uniformity (σ/μ), and endurance. The CF-based TS devices present excellent on/off ratio, small V_{th}, and ultra-low leakage current, while OTS and MIT devices exhibit good switching speed and on-current. However, the performance enhancements are still urgently demanded for the commercialization of TS devices. The suggestions are shown below.

(1) *On-off ratio.* On/off ratio enhancement includes the reduction of leakage current and the increase of on-current. CF-based TS devices have a high on/off ratio because of the ultra-low leakage current (even at the level of 0.01pA), which results from the highly insulating properties of dielectrics when the filament is dissolved. In order to fulfill the requirements of selectors in cross-point 1S1R memory technology, the on-current should reach at least 1 mA. The main idea for on-current enhancement is to guide the formation of multiple weak filaments at the high compliance current. There are various strategies from the aspects of active electrode, interface and dielectrics. Changing the active electrode structure (for example, nanodots/nanotips) or material component (for example, alloys or compounds) instead of active metal thin films can control and modulate the strength of filaments. Employment of multi-layer (bilayer or trilayer) dielectrics can constrain the filament formation in the specific switching layer. In addition, defective graphene film with nanoscale holes at the interface between active metal electrode and dielectrics work as atom filter and constrain the position and size of the filaments, which greatly raises the on-current. As for OTS and MIT devices, small on/off ratio and high leakage current are the main challenges for the selector applications. After electroforming (soft breakdown) process, the resistance of dielectric becomes lower than the initial state and cannot recover. Therefore, a more insulating dielectric (also known as electron barrier), for example, Al_2O_3, is always added in the switching layer to reduce the leakage current.

(2) *Switching speed*. The switching speed includes both the delay time of turn-on and relaxation time of turn-off under the voltage pulses. The high switching speed of the OTS and MIT devices is induced by the extremely fast crystallization rate and fast phase transition, respectively. But the mobility of the active metal ions in the dielectrics limits the switching speed, especially the turn-off speed of CF-based TS devices. To accelerate the spontaneous rupture process, some effective methods are proposed. The relaxation time has linear dependence on the amplitude and width of the applied voltage pulse. In addition, it is also related to the nucleation barrier energy W_0 of the dielectric materials from the view of nucleation theory. Since the W_0 value is related to surface tension, searching for materials possessing high interface energy against metallic filaments would be the key to modulate relaxation time.

(3) *Uniformity*. All the three types of TS devices have poor uniformity and large variation of operation parameters (for example, V_{th}, I_{off}) due to the stochastic atomic arrangements during the processes of filament formation and rupture. The intrinsic stochasticity of TS devices is good for some specific applications. For example, the requirement of the random entropy source makes TS devices the perfect unit for the security application like TRNG and PUF. However, the stochasticity has a negative effect on selector and neuromorphic devices. CF-based TS devices show large variation of V_{th} value (σ/μ, standard deviation divided by average value) even up to 20%. To reduce the stochastic formation and rupture of filaments, the main solution is to restrict the filament formation in specific positions from the view of electrode and dielectric modification. The variation of 20% could be reduced to less than 5%, but the employed methods are not compatible with CMOS and memory devices, for example, chemical synthesis of Ag nanoparticles.

(4) *Endurance*. The reliable characterization of endurance is the first issue to be solved. Lanza *et al.*[174] claim that most endurance tests based on resistance *versus* cycle plots contain very few data points (even<20), which is highly inaccurate and unreliable because it cannot reliably demonstrate that the device effectively switches in every cycle and it ignores C2C and D2D variability. They constructed endurance plots showing one data point per cycle and resistive state and combined data from multiple devices. According to the characterization rule, the endurance of MIT and OTS devices is usually less than 10^{10} cycles, while CF-based TS devices show relatively poor endurance less than 10^8 cycles due to the excessive injection of active metal ions after several operations leading to the stuck-on issues. Diffusion barrier layers such as TiN are always used to inhibit the excessive injection. In addition, alloy or compound electrodes are also proved to be effective for endurance enhancement. High endurance ensures that the response of the devices after repetitive operations can still be consistent, which is valuable for the security applications and large memory array.

For the practical implementation of memristors-based system, the devices would be required for mass production using mainstream manufacturing technology. Most of the present peripheral circuits/components for neuromorphic computing and hardware security are based on the current CMOS technology. Realizing the excellent integration and compatibility between TS and CMOS devices/techniques is very important. The above materials and methods have been reported for improving performances of TS devices. However, some of the methods are not compatible with the CMOS technology, which would not be accepted by the IC industry. Apart from device optimization, there is no uniform theory on switching

mechanisms of TS devices due to the lack of effective characterizations. *In-situ* HRTEM characterization and first principles calculation are helpful to observe and understand the evolution of metallic conductive filaments. However, when the filament composition becomes complex especially with various performance optimization schemes, the traditional evolution model of Ag or Cu conductive filaments is obviously insufficient to meet the demand. For example, multi-metal (CuAg) filaments and oxygen vacancy-metal coupling filaments (*Vo*-Ag) lack effective observation methods and theoretical models. With a combination of materials and physics theories, breakthrough can be carried out from the views of electronic structure and crystal structure of materials. Therefore, we should further investigate the switching mechanisms of TS devices and find proper materials or methods that are suitable for commercial applications.

At last, the research of TS devices cannot be separated from the basic requirements of AIoT applications, including data and information collection, storage, processing and communication. To solve the sneak current problem, an ideal selector should be scalable and stackable with high nonlinearity, low leakage current (~pA), high on-current (>100 μA), fast switching speed (~ns), excellent endurance (>10^{10}), and good uniformity. The selectors reported in recent years are only prominent in some aspects even in the single device. To realize the large-scale memristive storage array, in-depth studies on the material system and mechanisms of TS-based selectors are indispensable. For artificial neurons, a simple circuit design, which can exhibit superior performance without capacitor, is desired for high density and efficiency. Employment of the parasitic capacitance of two-terminal TS devices could be a good scheme, but operation voltage, endurance and uniformity should be paid more attention for device performance enhancements. As for TRNG or PUF applications, the device optimization should be aimed at high-frequency operation (>1 GHz), high endurance, low energy consumption for each random bit (~fJ range), and small device area (~nm range). At the circuit level, smaller area occupation and simple design are more desirable. Finally, novel multi-functional applications are expected in future, which should be closely based on the feature of spontaneous decay and stochasticity. We are looking forward that volatile TS devices occupying a crucial role in the AIoT era.

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