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A novel SiC high-*k* superjunction power MOSFET integrated Schottky barrier diode with improved forward and reverse performance

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Abstract: A new SiC superjunction power MOSFET device using high-*k* insulator and p-type pillar with an integrated Schottky barrier diode (H*k*-SJ-SBD MOSFET) is proposed, and has been compared with the SiC high-*k* MOSFET (H*k* MOSFET), SiC superjunction MOSFET (SJ MOSFET) and the conventional SiC MOSFET in this article. In the proposed SiC H*k*-SJ-SBD MOSFET, under the combined action of the p-type region and the H*k* dielectric layer in the drift region, the concentration of the N-drift region and the current spreading layer can be increased to achieve an ultra-low specific on-resistance ($R_{on,sp}$). The integrated Schottky barrier diode (SBD) also greatly improves the reverse recovery performance of the device. TCAD simulation results indicate that the $R_{on,sp}$ of the proposed SiC H*k*-SJ-SBD MOSFET is 0.67 mΩ·cm^2 with a 2240 V breakdown voltage (BV), which is more than 72.4%, 23%, 5.6% lower than that of the conventional SiC MOSFET, H*k* SiC MOSFET and SJ SiC MOSFET with the 1950, 2220, and 2220 V BV, respectively. The reverse recovery time and reverse recovery charge of the proposed MOSFET is 16 ns and18 nC, which are greatly reduced by more than 74% and 94% in comparison with those of all the conventional SiC MOSFET, H*k* SiC MOSFET and SJ SiC MOSFET, due to the integrated SBD in the proposed MOSFET. And the trade-off relationship between the $R_{on,sp}$ and the BV is also significantly improved compared with that of the conventional MOSFET, H*k* MOSFET and SJ MOSFET as well as the MOSFETs in other previous literature, respectively. In addition, compared with conventional SJ SiC MOSFET, the proposed SiC MOSFET has better immunity to charge imbalance, which may bring great application prospects.

Key words: SiC; MOSFET; specific on-resistance; breakdown voltage; high-*k*; superjunction; switching performance; reverse recovery characteristic

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1. Introduction

Silicon carbide (SiC) power metal–oxide–semiconductor field-effect transistors (MOSFETs) have attracted more and more attention and gradually replaced traditional silicon-based power switching devices due to their excellent electrical and thermal properties[1–6]. The vertical SiC power MOSFETs have been commercialized and widely used in many power electronics systems[7–9]. Compared with the conventional SiC power MOSFET, the specific on-resistance ($R_{on,sp}$) of the SiC superjunction (SJ) power MOSFET is drastically lowered at the same breakdown voltage (BV)[10–12]. However, the SJ structure needs to consider the problem of charge imbalance. Once charge imbalance exists due to random process variation, the BV will decrease by a relatively large margin[13, 14]. On the other hand, the silicon high-*k* (H*k*) insulator MOSFETs have been extensively studied because it does not easily suffer from charge imbalance and the process flow is less complex than SJ MOSFETs [15–18]. However, in order to bring its advantages into full performing, the permittivity of H*k* insulators in silicon H*k* MOSFETs needs to be very large, typically greater than 200[15]. At present, a lot of high-*k* insulator materials are considered for H*k* MOSFETs, e.g., $SrTiO_3$, $BaTiO_3$, PZT and other materials[19–21]. However, most of them are ferroelectric materials and may not be suitable for high-speed switching applications[15].

Up to now, the H*k* MOSFET based on SiC has been rarely studied. In order to solve the above problems, this article proposes a SiC high-*k* superjunction integrated Schottky barrier diode (H*k*-SJ-SBD) MOSFET structure (high-*k* insulator combined p-pillar in the drift region), which not only solves the problem of charge imbalance in the SJ structure, but also solves the problem that H*k* materials in the H*k* structure require a large permittivity. Moreover, a Schottky barrier diode (SBD) is also employed in the proposed H*k*-SJ-SBD MOSFET, which results in a greatly improvements on the reverse recovery performance of the proposed device.

2. Device structure and mechanism

Fig. 1 shows the device structures of the conventional SiC MOSFET, SiC H*k* MOSFET, the SiC SJ MOSFET and the proposed SiC H*k*-SJ-SBD MOSFET, respectively. All the SiC MOSFETs have the same 11 μm drift region thickness. In the SiC

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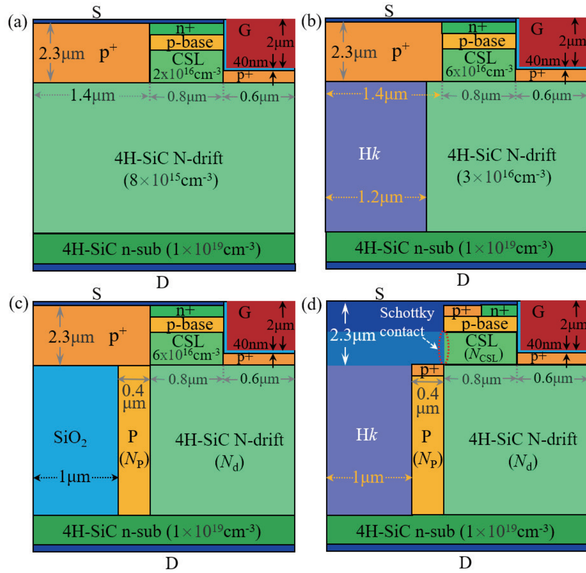


Fig. 1. (Color online) (a) Conventional SiC MOSFET. (b) H*k* SiC MOSFET. (c) SJ SiC MOSFET. (d) Proposed H*k*-SJ-SBD SiC MOSFET.

MOSFETs, the p⁺ shielding layers under the trench oxide of all the devices are used to relieve the electric field of the bottom corner of the trench[22]. The current spreading layer (CSL) is used to suppress the junction field-effect transistor (JFET) effect and reduce the specific on-resistance ($R_{on,sp}$) of the devices[23]. In the H*k* SiC MOSFET structure (Fig. 1(b)), a part of the drift region is filled with a high-*k* insulating layer, and the doping concentration of the drift region can be increased dramatically from 8×10^{15} to 3×10^{16} cm^{-3}[15, 24]. At the same time, the doping concentration of the CSL region can also be increased from 2×10^{16} to 6×10^{16} cm^{-3}. In the SiC SJ MOSFET structure (Fig. 1(c)), the ion implantation is performed to form the p-type pillar region after the trench being etched, and then SiO_2 is deposited. This structure is beneficial to realize low-cost SiC superjunction devices[25]. And the optimized p-region concentration (N_p) and drift region concentration (N_d) can also achieve charge balance. In the proposed 4H-SiC H*k*-SJ-SBD MOSFET (Fig. 1(d)), the SiO_2 dielectric filled in the trench is replaced by a high-*k* dielectric layer, and an Schottky contact with titanium metal (work function is 4.33 eV) is introduced in the side wall of the trench as a part of the source to form a reverse freewheeling Schottky barrier diode (SBD). And in the proposed structure, the CSL region doping concentration (N_{CSL}) and the drift region doping concentration (N_d) can be further increased to further reduce the $R_{on,sp}$. At the same time, the N_p and N_d can be optimized to achieve charge balance and better performance. In the reverse conduction state of the proposed SiC H*k*-SJ-SBD MOSFET, the CSL is not completely depleted, so the integrated SBD is turned on. The electrons flow through the Schottky contact, CSL and N-drift region to the drain electrode, which enhances the reverse freewheeling capability of the proposed H*k*-SJ-SBD 4H-SiC MOSFET.

3. Simulation results and discussion

Based on the device simulation parameters in Fig. 1, TCAD numerical simulations are performed to authenticate the performances of the four SiC trench power MOSFET devices, respectively. The main physical models for device simulation include SRH, Fermidirac, AUGER, CVT, FLDMOB, CONMOB, BGN, INCOMPLETE and IMPACT ANISO. And the channel mobilities of all four devices in the simulation are set to 40 cm²/(V·s) based on the experimental results in Ref. [26]. Fig. 2(a) shows the breakdown voltages (BVs) of the conventional SiC MOSFET and the SiC H*k* MOSFET with different permittivity of high-*k* insulators. As can be seen from the figure, the conventional MOSFET achieves a BV of 1950 V, and the BV of the H*k* MOSFET increases with the increase of the permit-

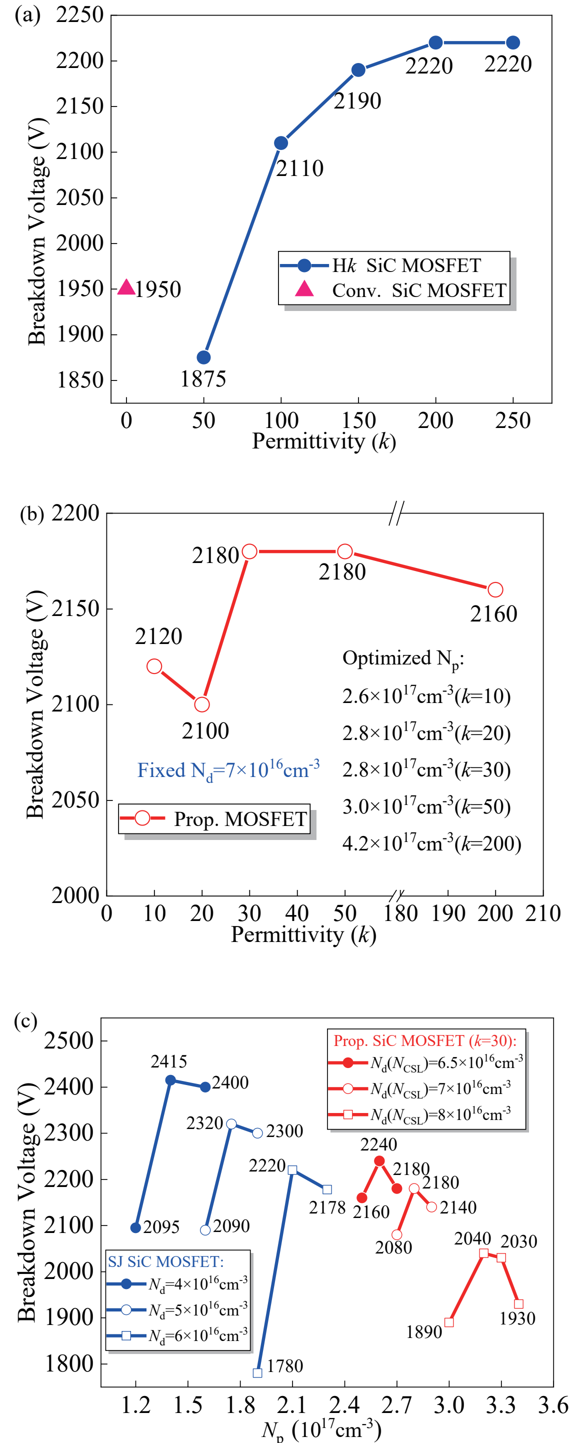


Fig. 2. (Color online) (a) BVs of the conventional MOSFET and H*k* MOSFET with different permittivity of high-*k* insulators. (b) BVs of the proposed H*k*-SJ-SBD MOSFET with different permittivity of high-*k* insulators. (c) BVs of different N_d, N_{CSL}, N_p in SJ MOSFET and proposed H*k*-SJ-SBD MOSFET ($k = 30$).

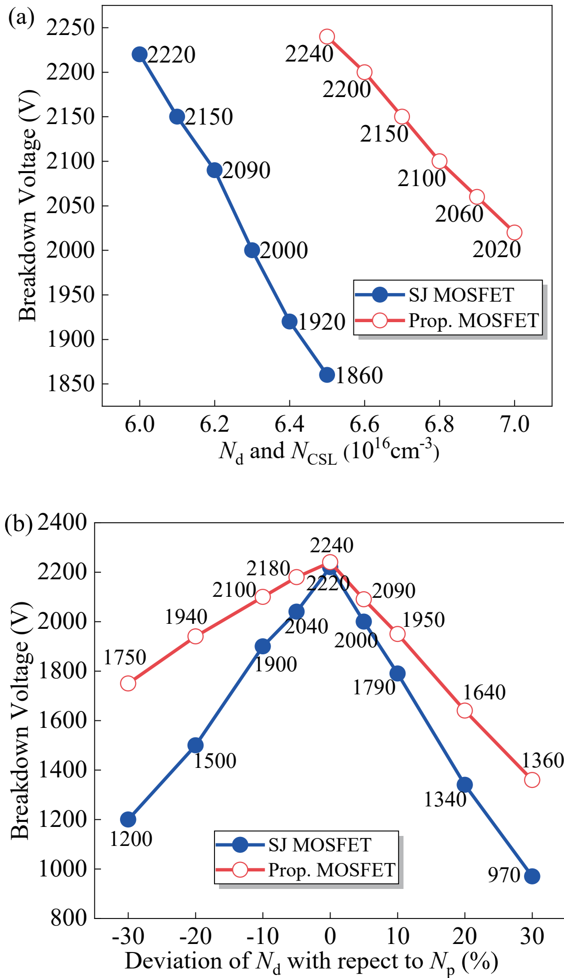


Fig. 3. (Color online) (a) Breakdown voltage of SJ MOSFET and proposed H*k*-SJ-SBD MOSFET at different N_d and N_{CSL}. (b) Breakdown voltages versus the deviation of N_d for SJ MOSFET and proposed H*k*-SJ-SBD MOSFET.

tivity, but when the permittivity is up to 200, the BV tends to be saturated with a value of 2220 V. This is because as the permittivity increases, more electric field lines generated by ionized donors in the n-region enter the high-*k* insulating layer laterally, and when the permittivity reaches 200, the electric field lines tend to be saturated. Therefore, the optimized minimum value of permittivity for the H*k* MOSFET is 200. Fig. 2(b) shows the BVs of the proposed SiC H*k*-SJ-SBD MOSFET with different permittivity (*k*) of high-*k* insulators under the optimized N_d and N_p[27]. It can be seen from the figure that when the high-*k* permittivity changes in a large range, the change in breakdown voltage is small, indicating that the high-*k* permittivity has little effect on the breakdown voltage of the proposed H*k*-SJ-SBD MOSFET. In the proposed H*k*-SJ-SBD MOSFET, the high-*k* insulator dramatically increases the effective permittivity ε_{eff} ($\varepsilon_{eff} \approx \varepsilon_I + \varepsilon_S$) of the semiconductor region, where ε_I and ε_S are the permittivity of the high-*k* insulator and semiconductor (SiC), respectively. Therefore, if the drift region is considered as a one-dimensional case, the Poisson's equation of it can be given by the following formula (1)[27].

$$-\frac{\partial^2 V}{\partial y^2} = \frac{\partial E}{\partial y} = \frac{qN_{eff}}{\varepsilon_{eff}} \approx \frac{qN_{eff}}{\varepsilon_I + \varepsilon_S}, \quad (1)$$

where N_{eff} and ε_{eff} are the effective doping concentration and

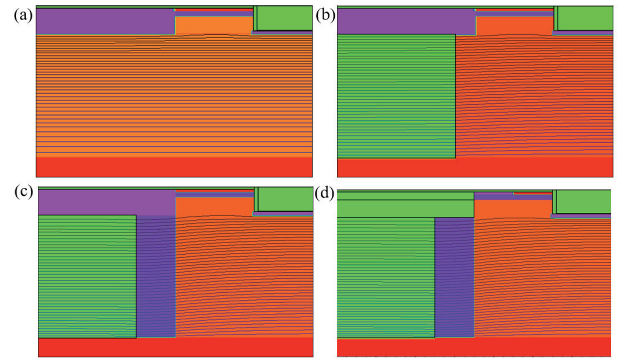


Fig. 4. (Color online) Equipotential line distributions of (a) the conventional MOSFET, (b) the H*k* MOSFET, (c) the SJ MOSFET, and (d) the proposed H*k*-SJ-SBD MOSFET (50V/line) at their own breakdown voltage.

effective permittivity of the semiconductor region. When the structure is charge-imbalanced ($N_{eff} \neq 0$), only a small amount of ε_{eff} is required to mitigate the effect of excess ionized impurities on BV. Therefore, the permittivity of the high-*k* insulator required for the proposed H*k*-SJ-SBD MOSFET is much lower than that of H*k* MOSFET. So, the permittivity *k* of the insulator with a value of 30 is selected for design the proposed SiC H*k*-SJ-SBD MOSFET. And there are many non-ferroelectric insulators with a permittivity of around 30, such as La_2O_3[28], $LaAlO_3$[29] and Ta_2O_5[30]. These materials have been used in SiC power devices and can easily be prepared in SiC power devices[31–33]. And their critical breakdown electric fields are 4 MV/cm[34], 11 MV/cm[35], 4.5 MV/cm[36] respectively, all are higher than 3MV/cm of SiC materials[37], so they are all suitable for H*k* insulators. Fig. 2(c) depicts the BVs of the SJ MOSFET and proposed H*k*-SJ-SBD MOSFET (k = 30) at different N_d, N_{CSL} and N_p. In order to achieve the BV of SJ MOSFET at about 2200 V, and to meet the charge balance condition and low specific on-resistance ($R_{on,sp}$) at the same time, the optimum value of N_d and N_p for the SJ MOSFET are set to be 6×10^{16} and 2.1×10^{17} cm^{-3}, respectively. When there are some excess ionized acceptors in the p-type region, N_{eff} in Eq. (1) becomes a negative value at the macro level. Thus, with the same BV, the N_d can be increased[27]. Therefore, the optimum value of N_d and N_p for the proposed H*k*-SJ-SBD MOSFET are 6.5×10^{16} and 2.6×10^{17} cm^{-3}, respectively, and the BV is 2240 V.

Fig. 3(a) shows the breakdown voltages of SiC SJ MOSFET and proposed H*k*-SJ-SBD MOSFET at different N_d and N_{CSL}, respectively. As can be seen from the figure, the breakdown voltages decrease with the increasing of N_d (the N_{CSL} is set to the same as N_d), which is due to the increased lateral electric field caused by the charge imbalance[38]. The breakdown voltage of SiC SJ MOSFET drops faster than the proposed SiC H*k*-SJ-SBD MOSFET because the proposed MOSFET is less affected by charge imbalance than the SJ MOSFET. And from the figure, when the SJ MOSFET and the proposed MOSFET are charge balanced, the BV is 2220 and 2240 V, respectively. Fig. 3(b) shows the breakdown voltage versus the deviation of N_d for the SiC SJ MOSFET and proposed SiC H*k*-SJ-SBD MOSFET. As can be seen from the figure, the charge imbalance caused by the deviation of N_d and N_{CSL} will cause the breakdown voltage to drop, and the breakdown voltage of SJ MOSFET drops faster than that of proposed H*k*-SJ-SBD MOSFET, which indicates that the proposed MOSFET has better im-

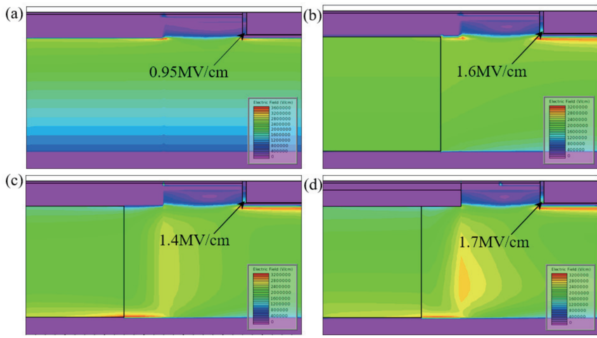


Fig. 5. (Color online) Electric field distributions of the oxide at the trench corner of (a) the conventional MOSFET, (b) the H*k* MOSFET, (c) the SJ MOSFET, and (d) the proposed H*k*-SJ-SBD MOSFET at their own breakdown voltages.

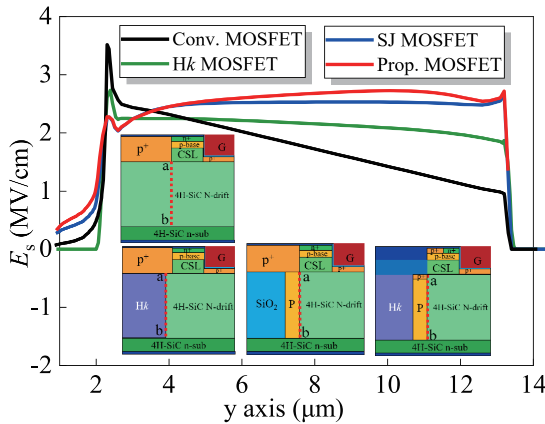


Fig. 6. (Color online) Electric field distributions along the dotted line *ab* of the four devices at their own breakdown voltages.

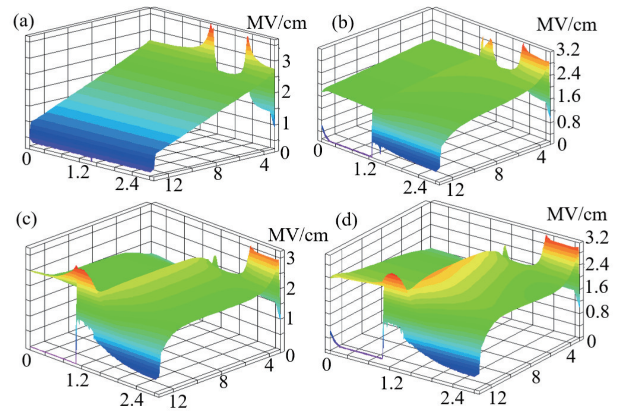


Fig. 7. (Color online) Three-dimensional electric field distributions of the (a) the conventional MOSFET, (b) the H*k* MOSFET, (c) the SJ MOSFET, and (d) the proposed H*k*-SJ-SBD MOSFET at their own breakdown voltages.

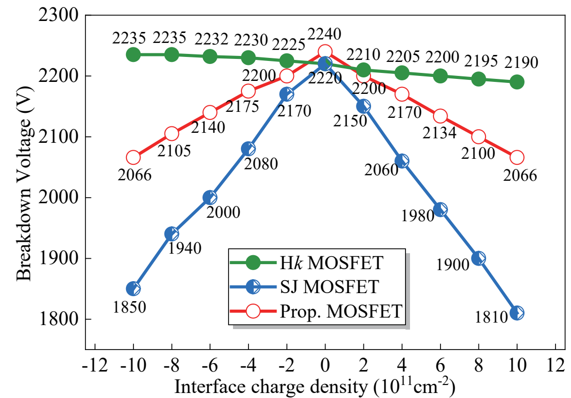


Fig. 8. (Color online) Breakdown voltages at different interface charge densities in SJ MOSFET, H*k* MOSFET and proposed H*k*-SJ-SBD MOSFET.

munity against charge imbalance.

Fig. 4 shows the equipotential line distributions of the conventional MOSFET, the H*k* MOSFET, the SJ MOSFET and the proposed H*k*-SJ-SBD MOSFET (50V/line) at their own breakdown voltages, respectively, which indicates that the equipotential line distributions of the drift region of the proposed H*k*-SJ-SBD MOSFET is more uniform compared with the conventional MOSFET device. And the equipotential line distributions of the SJ MOSFET and H*k* MOSFET are similar to that of the proposed H*k*-SJ-SBD MOSFET, which indicates the excellent blocking voltage performance of the proposed MOSFET.

Fig. 5 reveals the electric field distributions of the oxide at the gate trench corner of the conventional MOSFET, the H*k* MOSFET, the SJ MOSFET and the proposed H*k*-SJ-SBD MOSFET at their own breakdown voltages, respectively. It can be seen from the figures that the electric field of oxide at the trench corner of the conventional SiC MOSFET, SiC H*k* MOSFET, SiC SJ MOSFET and the proposed SiC H*k*-SJ-SBD MOSFET at their own breakdown voltages is 0.95, 1.6, 1.4, and 1.7 MV/cm, respectively. The electric field of the oxide at the gate trench corner of the four devices is much lower than that of the critical electric field of SiC material, so the breakdown voltage and reliability of the devices will not be affected.

Fig. 6 illustrates the electric field distributions along the dotted line *ab* of the four devices at their own breakdown voltages. As can be seen from the figure, except for the conventional MOSFET, the electric field distributions of the other three devices is relatively uniform. The conventional MOSFET has the largest peak electric field and the smallest BV. Compared with the conventional SiC SJ MOSFET, the proposed MOSFET has a slightly higher electric field because the doping concentrations in the p-pillar and n-drift regions of the proposed MOSFET is higher[27]. Therefore, the proposed MOSFET has the highest breakdown voltage.

Fig. 7 demonstrates the three-dimensional electric field distributions of the conventional MOSFET, the H*k* MOSFET, the SJ MOSFET and the proposed H*k*-SJ-SBD MOSFET at their own breakdown voltages, respectively. It can be seen from the figure that the electric field distribution in the drift region of the proposed H*k*-SJ-SBD MOSFET is very uniform and the electric field is the largest, which again proves that the proposed H*k*-SJ-SBD MOSFET has a larger BV.

Fig. 8 plots the breakdown voltages at different interface charge densities in SJ MOSFET, H*k* MOSFET and proposed H*k*-SJ-SBD MOSFET. For the proposed H*k*-SJ-SBD MOSFET and the SJ MOSFET, both positive and negative interface charges will lead to charge imbalance, resulting in a drop in breakdown voltage. The breakdown voltage of the SJ MOSFET drops faster because it is more sensitive to charge imbalance. For the H*k* MOSFET, the effective doping density $N_{\rm eff}$ is defined as[39],

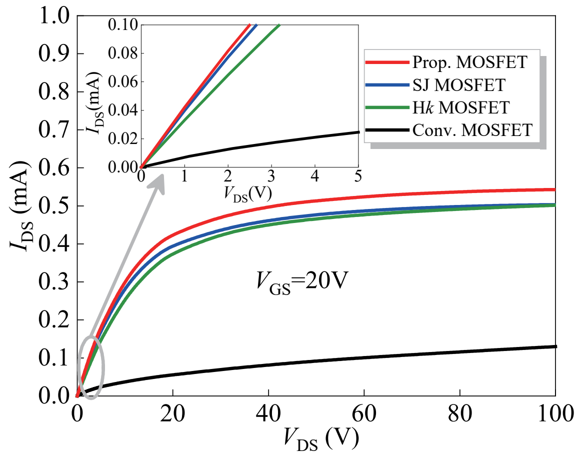


Fig. 9. (Color online) I–V curves of the four devices at V_{GS} = 20 V.

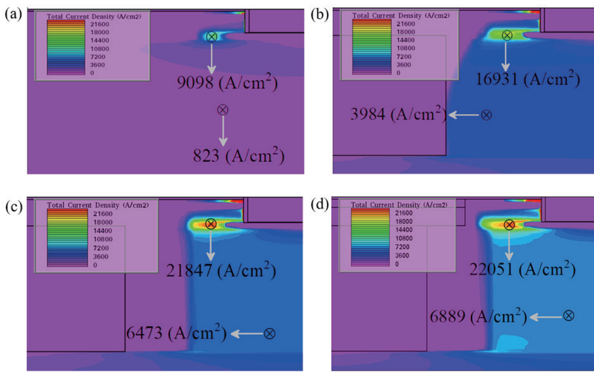


Fig. 10. (Color online) Current density distributions at V_{GS} = 20 V, V_{DS} = 2 V of (a) the conventional MOSFET, (b) the Hk MOSFET, (c) the SJ MOSFET, and (d) the proposed Hk-SJ-SBD MOSFET.

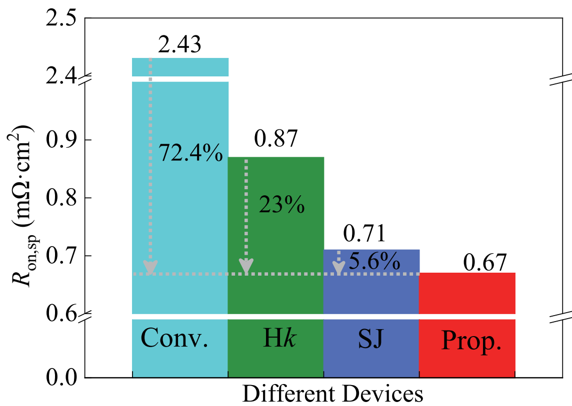


Fig. 11. (Color online) $R_{on,sp}$ results of the Hk MOSFET, SJ MOSFET and conventional MOSFET compared with that of the proposed Hk-SJ-SBD MOSFET device.

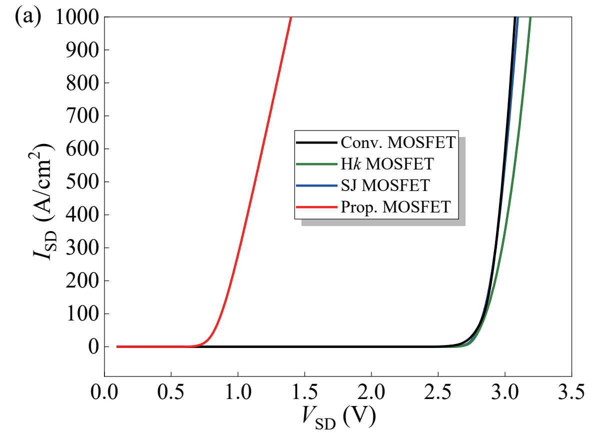
$$N_{eff} = N_D + \frac{\alpha N_{it}}{w}, \tag{2}$$

where N_{it} is the interface charge density, α is an adjustment ratio of N_{it} and the w is the width of the n-drift region. When the interfacial charge density changes from -1×10^{12} to 1×10^{12} cm^{-2}, the breakdown voltage decreases because the effective doping density increases. And the deposited SiO_2 followed by N_2O annealing is effective to decrease the interface state density[40].

Fig. 9 depicts the on-state I–V curves of the four devices at V_{GS} = 20 V. It is clear from the figure that the on-state drain current I_{DS} of the proposed Hk-SJ-SBD MOSFET is the largest at the same V_{GS} and V_{DS}. This is because the proposed Hk-SJ-SBD MOSFET has the largest N_{CSL} and N_d. And the conventional MOSFET has the lowest current, since the lowest doping concentration of the N_{CSL} and N_d.

Fig. 10 shows the current density distributions at V_{GS} = 20 V and V_{DS} = 2 V of all the devices, respectively. It can be seen from the figure that the proposed Hk-SJ-SBD MOSFET has the highest current density because the proposed Hk-SJ-SBD MOSFET has the largest N_d and N_{CSL}.

Fig. 11 shows the $R_{on,sp}$ comparison results of the proposed Hk-SJ-SBD MOSFET and the other three SiC MOSFET devices. And the $R_{on,sp}$ of the proposed Hk-SJ-SBD MOSFET is the smallest, which is 72.4%, 23% and 5.6% lower than those of the conventional MOSFET, Hk MOSFET and SJ MOSFET, respectively.



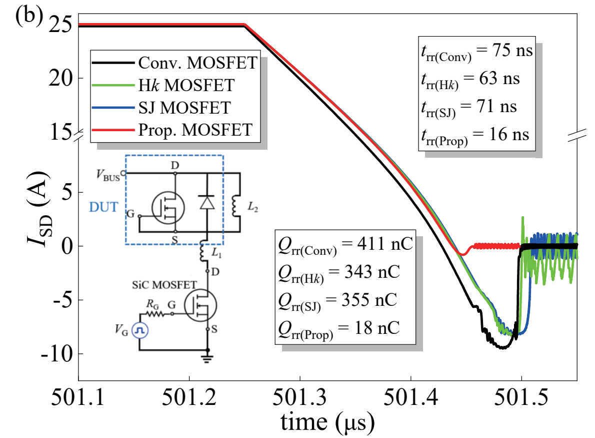


Fig. 12. (Color online) (a) Reverse conduction characteristics of the four devices. (b) Reverse recovery characteristics and the simulation circuit diagram of the four devices.

Fig. 12(a) plots the reverse conduction I–V characteristics of the four devices. The turn-on voltage drop (V_F) of the integrated SBD in the proposed MOSFET is about 0.7 V with a metal work function of 4.33 eV (titanium), while the V_F of the body intrinsic SiC p–n diode of all the other three devices is about 2.7 V[41]. Therefore, the V_F of the proposed Hk-SJ-SBD MOSFET is much smaller than that of the other three devices. Fig. 12(b) reveals the reverse recovery characteristics and the simulation circuit schematic of the four devices. And the peak reverse recovery current (I_{rrm}) of the conventional MOSFET, Hk MOSFET, SJ MOSFET and proposed MOSFET are 9.5, 8.3,

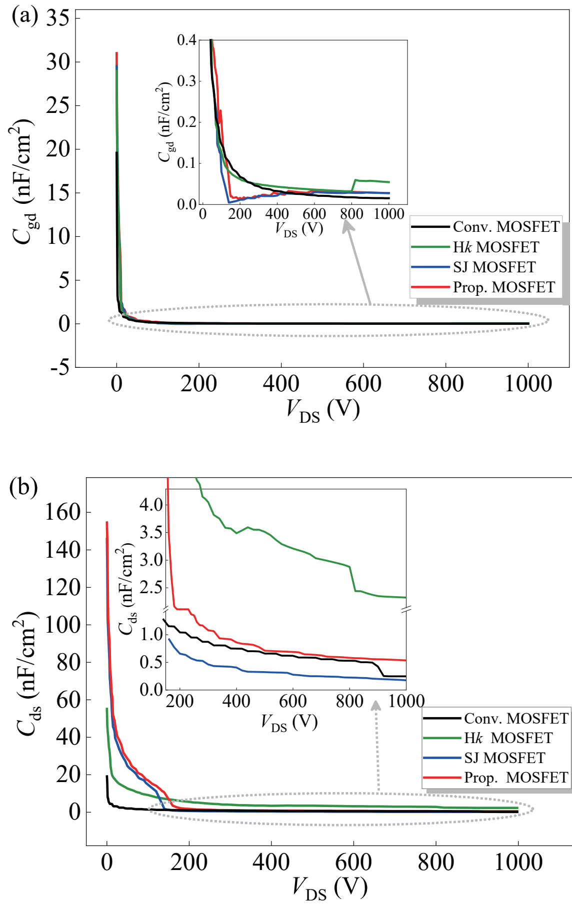


Fig. 13. (Color online) (a) the drain-gate capacitance (C_{gd}) and (b) the drain-source capacitance (C_{ds}) of the conventional MOSFET, H*k* MOSFET, SJ MOSFET and proposed H*k*-SJ-SBD MOSFET.

8.2, 1.9 A, respectively. The reverse recovery time (t_{rr}) of the conventional MOSFET, H*k* MOSFET, SJ MOSFET and proposed MOSFET are 75, 63, 71, 16 ns, respectively. The reverse recovery charge (Q_{rr}) of conventional MOSFET, H*k* MOSFET, SJ MOSFET and proposed MOSFET are 411, 343, 355, 18 nC, respectively. In short, the I_{rrm}, t_{rr} and Q_{rr} of the proposed SiC MOSFET are greatly reduced by more than 76%, 74% and 94% in comparison with those of all the conventional SiC MOSFET, H*k* SiC MOSFET and SJ SiC MOSFET respectively, so the reverse recovery capability of proposed H*k*-SJ-SBD MOSFET is greatly improved due to the integration of the SBD.

Fig. 13(a) shows the drain–gate capacitance (C_{gd}) of the four SiC MOSFETs. Since the gate structures of the four devices are identical, the C_{gd} of the four devices are close to each other. It can be seen from the figure that when the drain-source voltage (V_{DS}) is greater than 300 V, the C_{gd} of H*k* MOSFET is the largest, because the permittivity of the high-*k* insulator in the drift region of H*k* MOSFET is very high (up to 200). Fig. 13(b) shows the drain-source capacitance (C_{ds}) of the four SiC MOSFETs. As can be seen from the figure, when the drain-source voltage (V_{DS}) is greater than 150 V, the C_{ds} of H*k* MOSFET is the largest, and the C_{ds} of SJ MOSFET is the smallest. This is because the H*k* MOSFET has the largest ε_{eff} ($\approx \varepsilon_I + \varepsilon_S$), resulting in the largest C_{ds}. The C_{ds} of the conventional MOSFET is between the proposed H*k*-SJ-SBD MOSFET and SJ MOSFET because the permittivity of SiC is 9.7, which is larger than that of SiO_2, but less than 30[42].

Fig. 14(a) shows the simulation circuit of four SiC MOSFETs switching transients. Fig. 14(b) exhibits the switching performances of the four SiC MOSFETs. Fig. 14(c) exhibits the switching loss (E_{on} + E_{off}) of the four SiC MOSFETs. It can be seen from the figure that H*k* MOSFET has the largest switching loss because H*k* MOSFET has the largest C_{gd} + C_{ds}. And the switching loss of the proposed device is also only slightly higher than those of the conventional SiC MOSFET and SiC SJ MOSFET.

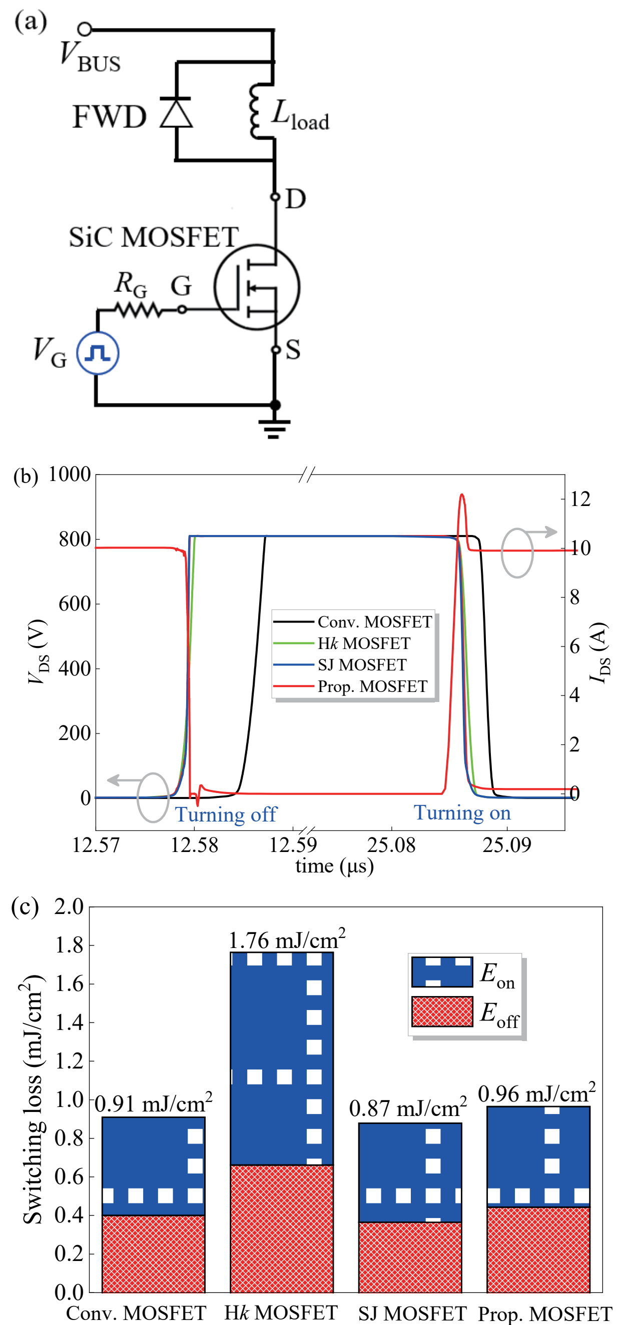


Fig. 14. (Color online) (a) Simulation circuit of four SiC MOSFET switching transients (R_G = 5 Ω). (b) Switching performances of the four SiC MOSFETs. (c) Switching loss (E_{on} + E_{off}) of the four SiC MOSFETs.

Table 1 lists the comparison results among the proposed SiC H*k*-SJ-SBD MOSFET, H*k* MOSFET, SJ MOSFET and the conventional MOSFET. The figure of merit (FOM = $BV^2/R_{on,sp}$) of the proposed H*k*-SJ-SBD MOSFET is the largest, reaching 7489 MV/cm². In addition to the superiority of the FOM, the switching performance of the proposed device is very close to that of the conventional MOSFET and the SJ MOS-

Table 1. Comparison between proposed H*k*-SJ-SBD MOSFET, H*k* MOSFET, SJ MOSFET and conventional MOSFET.

Parameter	Conv. MOSFET	H*k* MOSFET	SJ MOSFET	Prop. MOSFET
BV (V)	1950	2220	2220	2240
$R_{on,sp}$ (mΩ·cm²)	2.43	0.87	0.71	0.67
E_{on}+ E_{off} (mJ/cm²)	0.91	1.76	0.87	0.96
t_{rr} (ns)	75	63	71	16
I_{rrm} (A)	9.5	8.3	8.2	1.9
Q_{rr} (nC)	411	343	355	18
FOM (MV/cm²)	1565	5665	6941	7489

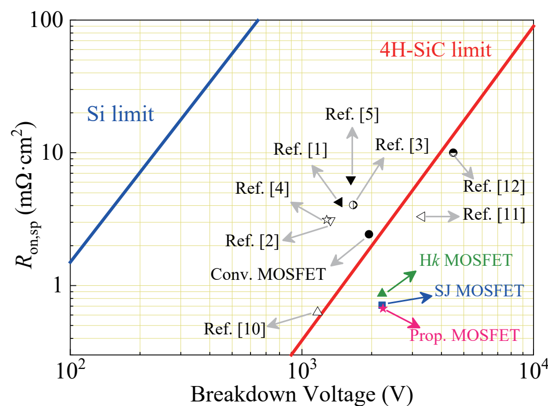


Fig. 15. (Color online) Trade-off relationship between the $R_{on,sp}$ and BV of the four SiC MOSFET devices and other SiC MOSFET devices.

FET, and is better than that of the H*k* MOSFET. And the reverse recovery performance (I_{rr}, Q_{rr} and t_{rr}) of the proposed device is greatly improved compared with the other three devices. Besides, from the above analysis, the proposed MOSFET is much less affected by charge imbalance than the SJ MOSFET.

Fig. 15 shows the trade-off relationship between the $R_{on,sp}$ and BV of the four SiC MOSFET devices and other reported SiC MOSFET devices. As can be seen from the figure, the proposed H*k*-SJ-SBD MOSFET achieves a better compromise between the $R_{on,sp}$ and BV compared to that of the conventional MOSFET, H*k* MOSFET and SJ MOSFET as well as SiC MOSFETs in other previous literature. This excellent compromise relationship of the proposed H*k*-SJ-SBD MOSFET is mainly attributed to the increase on the doping concentration of the drift region and the CSL layer.

4. Brief fabrication process

Fig. 16 shows brief fabrication process flow of the proposed H*k*-SJ-SBD 4H-SiC MOSFET, in which a possible method to manufacture the proposed device is presented. The fabrication process starts with a SiC epitaxial wafer (Fig. 16(a)). And the deep trench etching and ion implantation are performed to form the p-type region (Fig. 16(b)). Next, the gate trench and the top of the p-type region are etched (Fig. 16(c)). Then, the ion implantations are carried out to form the p-base, n⁺ and p⁺ regions, respectively (Fig. 16(d)). Next, the high-*k* insulating layer and the trench bottom source metal are deposited; and the gate oxide and polysilicon are deposited by atomic layer deposition (ALD) and chemical vapor deposition (CVD) to form the trench gate, respectively (Fig. 16(e)). Finally, the drain and source metal deposition and annealing are conducted to form Schottky and ohmic contacts (Fig. 16(f)) [43–45].

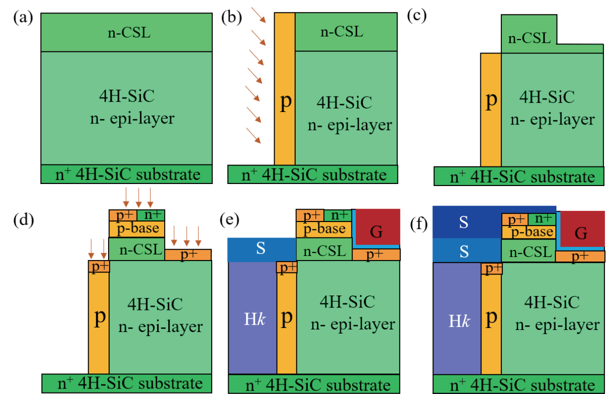


Fig. 16. (Color online) Brief fabrication process flow of the proposed 4H-SiC H*k*-SJ-SBD MOSFET. (a) The process starts with a SiC epitaxial wafer. (b) Deep trench etching and ion implantation to form p-type region. (c) Gate trench etching and p-type region etching. (d) Ion implantation and annealing to form p-base, n⁺ and p⁺ regions, respectively. (e) Deposition of high-*k* insulating layer, depositing the trench bottom source metal, formation of gate oxide by atomic layer deposition (ALD) and deposition of polysilicon by chemical vapor deposition (CVD) to form the gate. (f) Drain and surface source metal deposition and annealing to form Schottky and ohmic contacts.

5. Conclusion

A novel SiC high-*k* superjunction power MOSFET with an integrated sidewall Schottky barrier diode to achieve a better trade-off relationship between the specific on-resistance and the breakdown voltage is proposed and investigated in this article. The proposed SiC MOSFET not only alleviates the problem of charge imbalance in the SJ structure, but also solves the problem that the H*k* materials in the SiC H*k* MOSFET structure require a large permittivity. Compared with the SiC SJ MOSFET, H*k* MOSFET and the conventional MOSFET, the proposed SiC MOSFET not only has a better trade-off relationship between specific on-resistance and breakdown voltage, but also has much better reverse recovery capability. It is expected to be applied to the SiC power electronics. Also a brief manufacturing process flow is presented.

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