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Homojunction structure amorphous oxide thin film transistors with ultra-high mobility

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Abstract: Amorphous oxide semiconductors (AOS) have unique advantages in transparent and flexible thin film transistors (TFTs) applications, compared to low-temperature polycrystalline-Si (LTPS). However, intrinsic AOS TFTs are difficult to obtain field-effect mobility (μ_{FE}) higher than LTPS (100 $cm^2/(V{\cdot}s)$). Here, we design ZnAlSnO (ZATO) homojunction structure TFTs to obtain μ_{FE} = 113.8 $cm^2/(V{\cdot}s)$. The device demonstrates optimized comprehensive electrical properties with an off-current of about 1.5×10^{-11} A, a threshold voltage of –1.71 V, and a subthreshold swing of 0.372 V/dec. There are two kinds of gradient coupled in the homojunction active layer, which are micro-crystallization and carrier suppressor concentration gradient distribution so that the device can reduce off-current and shift the threshold voltage positively while maintaining high field-effect mobility. Our research in the homojunction active layer points to a promising direction for obtaining excellent-performance AOS TFTs.

Key words: thin film transistors; homojunction; carrier mobility; amorphous oxides

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1. Introduction

In the past decade, amorphous oxide semiconductor (AOS) thin-film transistors (TFTs) have become intensively attractive for the next generation of electronics[1–3]. In the field of large-area flat panel displays (FPDs), amorphous silicon (a-Si) as an active layer is gradually replaced by AOSs, due to the low field-effect mobility (μ_{FE}), generally less than (1 $cm^2/(V{\cdot}s)$)[4]. With the use of n-type AOSs, the higher electrical performance of TFT devices could be achieved, of which practical μ_{FE} exceeds 5 $cm^2/(V{\cdot}s)$. However, low-temperature poly-silicon (LTPS) TFTs with μ_{FE} of over 100 $cm^2/(V{\cdot}s)$ are widely used in active-matrix organic light-emitting diode (AMOLED) displays, which are difficult to be replaced by AOS TFTs due to the high field-effect mobility despite serious disadvantages of high cost and non-uniform device properties over large areas[5]. Accordingly, the need for AOS TFTs with high field-effect mobility is very urgent.

Amorphous indium–gallium–zinc–oxide (a-IGZO) was first reported as a channel material for thin-film transistors in 2004[6]. For a period of time afterward, the reported μ_{FE} of AOS TFTs was (5–30 $cm^2/(V{\cdot}s)$)[7–9]. The dual active layer for TFTs was found to achieve high field-effect mobility effectively. In 2012, Kim *et al.*[10]. reported the double-layer structure of HfInZnO/InZnO, with the μ_{FE} reaching 48 $cm^2/(V{\cdot}s)$. In 2014, Song *et al.*[11] reported ZnO/graphene hybrid structure, the device exhibited strikingly high mobility of 329.7 $cm^2/(V{\cdot}s)$, but the other device properties were unsatisfactory. In 2016 and 2018, Choi *et al.*[12] and Yang *et al.*[13] reported the double-layer structure of AlSnInZnO/InZnO, with the increase of the thickness of InZnO thin layer, the μ_{FE} of devices increased significantly to 50–60 $cm^2/(V{\cdot}s)$. However, for TFTs with homogeneous uniform AOS active layers, μ_{FE} of more than 100 $cm^2/(V{\cdot}s)$ has almost not been reported, and most of the reported AOS TFTs with high field-effect mobility exhibited high off-currents (I_{off}), poor on/off current ratios (I_{on}/I_{off}) and excessively negative threshold voltages (V_{th}).

To solve the problem, we designed a homojunction AOS active layer for TFT device. Although a-IGZO has been widely studied and shown excellent performance[14, 15], due to insufficient global reserves and the high cost of In and Ga, we chose amorphous ZnSnO (ZTO) instead of InZnO (IZO) based material in this work. It is mainly for the reason that In^{3+} and Sn^{4+} have similar electron configurations of $4d^{10}5s^0$ as the route of carrier transportation in the AOSs, which are the key factor to ensure high field-effect mobility[16, 17]. Aluminum was selected to be the carrier suppressor in amorphous ZnAlSnO (ZATO), because of Al^{3+} with a low standard electrode potential (SEP, –1.66 V), large reserves and strong Al–O bonding energy (512 kJ/mol)[18]. We successfully prepared TFT devices' homojunction active layer with the physical manufacturing process of ZATO (unannealed) / ZATO (annealed) /

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ZTO. The microstructure and electrical properties of the homojunction layer were studied in detail. With the distribution difference of micro-crystallization extent and carrier suppressor concentration in the homojunction layer, the carrier concentration would present distinctive throughout the layer correspondingly. The electrical performance of the homojunction structure TFTs was investigated in detail. The devices achieve μ_{FE} more than 100 $cm^2/(V{\cdot}s)$, ameliorating other electrical properties including I_{off}, I_{on}/I_{off} ratio and V_{th} at the same time. A unique carrier transport mechanism through the low carrier suppressor region of the homojunction structure was proposed to explore the high field-effect mobility. The homojunction active layer made of AOS will greatly promote the application of high-performance transparent and flexible electronics.

2. Experimental section

2.1. Preparation of homojunction ZATO active layer TFTs

Bottom-gate, top-contact structure TFTs were fabricated on 300 nm SiO_2/n++Si wafers. The substrates were ultrasonically cleaned respectively with acetone, ethanol, de-ionized water and ethanol for 30 min, and then dried in flowing nitrogen gas before being used. The homojunction channel of ZATO (unannealed) / ZATO (annealed) / ZTO (annealed) was fabricated by Magnetron sputtering (Kurt J. Lesker PVD-75). The targets were prepared from high purity of ZnO (99.99%), SnO_2 (99.99%), and Al_2O_3 (99.99%) powders with the molar ratios of Zn : Sn : Al= 4 : 9 : 0 and Zn : Sn : Al = 3 : 10 : 0.5. The ZTO film was deposited by RF magnetron sputtering with a total Ar&O_2 pressure of 1.5 mTorr (Ar : O_2 = 100 : 30) at 100 W at room temperature for 10 min and annealed at 900 °C in Ar atmosphere for 1 h. Then, the ZTO film was treated with a pressure 20 mTorr Ar&O_2 plasma (Ar : O_2 = 50 : 50) at 20 W for 10 min. Above the ZTO film, the ZATO film was deposited by RF magnetron sputtering with a total Ar+O_2 pressure of 7.52 mTorr (Ar : O_2 = 100 : 40) at 120 W at room temperature for 10 min and annealed at 500 °C in Ar atmosphere for 1 h. Then, the ZATO film was cured with a pressure 20 mTorr Ar&O_2 plasma (Ar : O_2 = 50 : 50) at 20 W for 10 min. Afterward, another layer of ZATO was sputtered by RF magnetron sputtering with the same process for 5 min without thermal post-annealing. Finally, 100-nm-thick Al source and drain electrodes were evaporated by electron beam evaporation at room temperature with a metal mask to avoid error of overestimation due to the absence of patterns[19]. The channel width (W) and length (L) dimensions were patterned W/L = 1000 μm / 200 μm. The 300-nm-thickness SiO_2 and heavily doped n-type Si were used as the gate insulator layer and the gate electrode, respectively. The corresponding process of uniform ZATO thin films deposited on SiO_2/n++Si substrates for the comparative study were also consistent as shown above.

2.2. Characterization of the homojunction structure and device properties

The EDS mapping of the films was carried out by EDAX-Team attached to field-emission scanning electron microscopy (FE-SEM Hitachi S-4800). The cross-sectional microstructure, crystal properties and energy dispersive X-ray (EDX) line profile of the homojunction active layer were obtained by high-resolution transmission electron microscopy (HR-TEM, Tecnai G2 F20 S-Twin). The carrier concentration and electrical resistivity of the films was measured by a Bio-Rad HL5500PC Hall system. The chemical bonding states were investigated by X-ray photoelectron spectroscopy (XPS, Thermo ESCALAB 250Xi). The electrical performances of the TFTs were measured in the dark by an Agilent E5270B semiconductor parameter analyzer.

3. Results and discussion

The elemental distribution of Zn, Sn, Al and O of a ZTO thin film annealed at 900 °C and a ZATO thin film annealed at 500 °C are shown in Fig. S1 of the Supporting Information, as obtained from EDS mapping attached to FE-SEM. The chemical composition in these films measured by EDS is Zn : Sn = 4.35 : 9.12 and Zn : Sn : Al = 6.90 : 20.5 : 1 (in atomic ratio), which are nearly consistent with ratios in the targets. The microstructure of the homojunction layer, as shown in the schematic diagram in Fig. 1(a), can be observed by transmission electron microscopy (TEM). The cross-sectional HRTEM images of the same sample with a 10 nm scale bar and 2 nm scale bar are illustrated in Figs. 1(b) and 1(c), respectively. The inset in Fig. 1(b) illustrates the selected area electron diffraction (SAED) result of the homojunction layer, showing a pattern of mixing polycrystalline (rings) and amorphous (diffuse rings). The thickness of the homojunction layer measured from the HRTEM images is approximately 20 nm. Clearly, there is a transition from amorphous to polycrystalline, from the top to the bottom of the homojunction layer, in which the thickness of the amorphous region is about 5 nm corresponding to the unannealed ZATO films. It is worth emphasizing that the 900 °C annealing only acts on the ZTO layer, which is the main factor for the generation of the polycrystalline structure at the bottom of channel. However, the annealed ZATO layer and the ZTO layer are practically indistinguishable due to the diffusion effect of high-temperature annealing which also leads to a gradient distribution of Al as a carrier suppressor. It is worth emphasizing that an Al-deficient layer is formed in the ZTO part after the diffusion, compared to as-deposited ZATO. Meanwhile, the polycrystalline formation in the active layer could result in high field-effect mobility of TFTs, which were repeatedly demonstrated in previous reports[20–22].

Fig. 1(d) exhibits the corresponding energy dispersive X-ray (EDX) line profile of the homojunction layer. Aluminum element is much less than other elements, which makes it not easy to discriminate the distribution of aluminum in Fig. 1(d). Hence, Al is shown separately in Fig. 1(e). Zn, Sn and O elements exhibit stable distributions in the homojunction layer, and the final sharp increase of O ratio is because of SiO_2 insulator. The Al element first stabilizes and then gradually decreases with increasing depth, probably owing to the Al diffusion during high-temperature treatment, which results in that Al^{3+} as carrier suppressor exhibits a decreasing gradient distribution from the top to the bottom layer through the whole layer. This is also the reason why it is named the homojunction active layer. In general, there are two trends in the homojunction layer with depth. One is the increase of micro-crystallization extent, and the other is the decrease of carrier suppressor concentration. It would profoundly affect the electrical performance of the device.

The oxygen vacancies (V_O) are dominant defects of AOSs, which are related to the generation of carriers for charge trans-

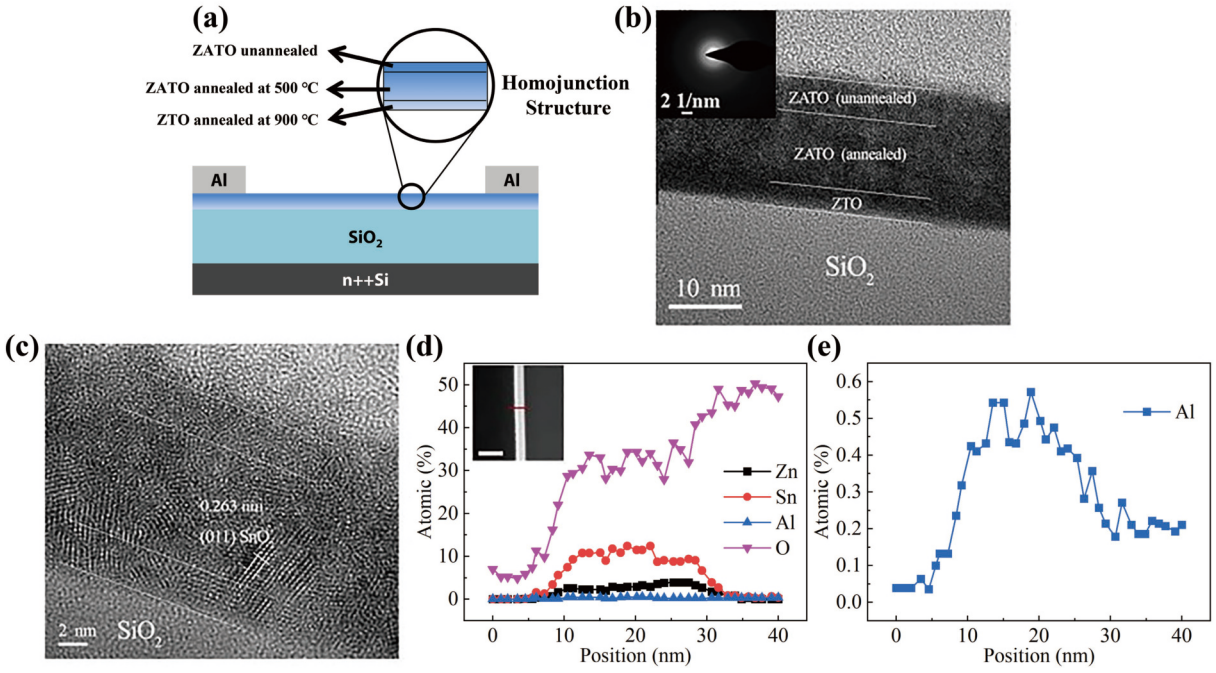

Fig. 1. (Color online) HRTEM cross-sectional images of the homojunction layer on a SiO_2/Si substrate. (a) Schematic diagram of the TFT device with homojunction amorphous ZnAlSnO active layer. (b) Scale bar, 10 nm, inset: SAED pattern; (c) scale bar, 2 nm. (d, e) Energy dispersive X-ray (EDX) line profile of the homojunction layer.

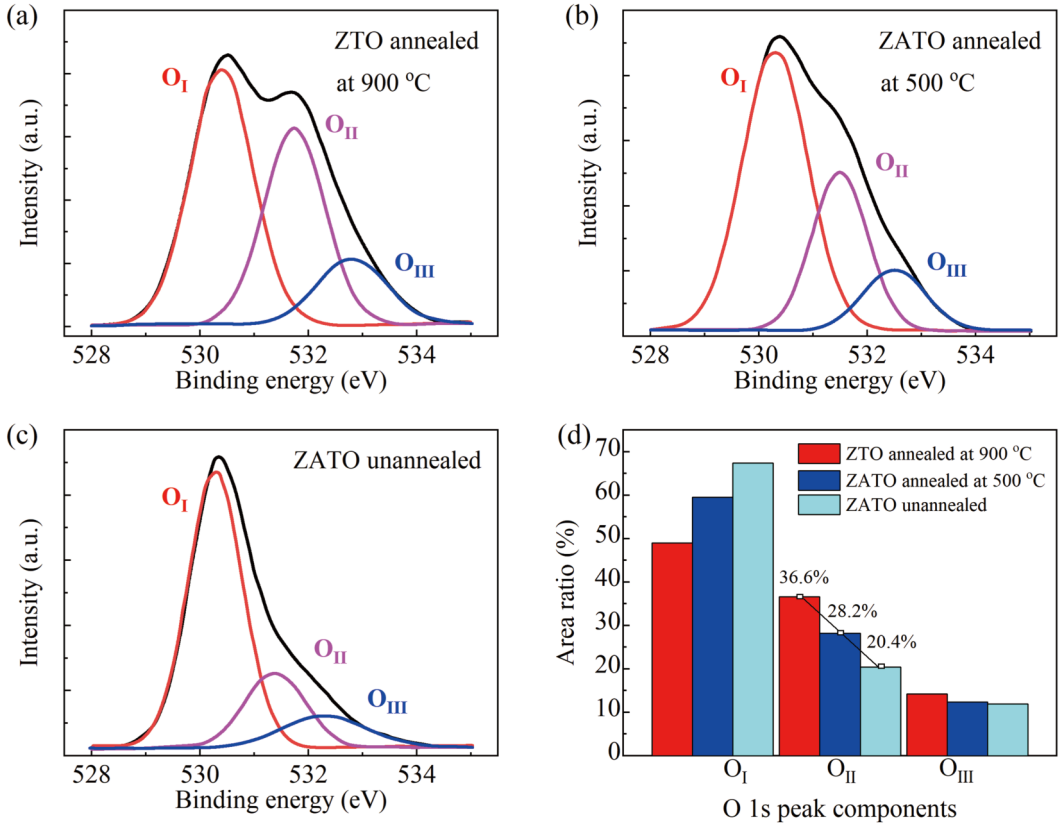

Fig. 2. (Color online) XPS spectra of O 1s. (a) ZTO film annealed at 900 °C. (b) ZATO film annealed at 500 °C. (c) ZATO film unannealed. (d) Areal ratios of the three O sub-peaks (O_I, O_{II} and O_{III}).

port[23]. To investigate the relative V_O concentration of each film deposited on a SiO_2/Si substrate, X-ray photoelectron spectroscopy (XPS) was used. As shown in Figs. 2(a)–2(c), the O 1s XPS spectra of the ZTO (annealed at 900 °C), ZATO (annealed at 500 °C) and unannealed ZATO thin film were typically divided into three peaks by using a mixed Gaussian-Lorentz function, labeled as O_I, O_{II} and O_{III} peaks, respectively, while the other Zn $2p_{3/2}$, Sn $3d_{5/2}$ and Al $2p_{3/2}$ XPS spectra are depicted in Fig. S2 of the Supporting Information. All binding energy data have been calibrated by taking C 1s reference at 284.8 eV for compensation of any charge-induced shifts. The Zn $2p_{3/2}$, Sn $3d_{5/2}$ and Al $2p_{3/2}$ XPS spectra are centered at ap-

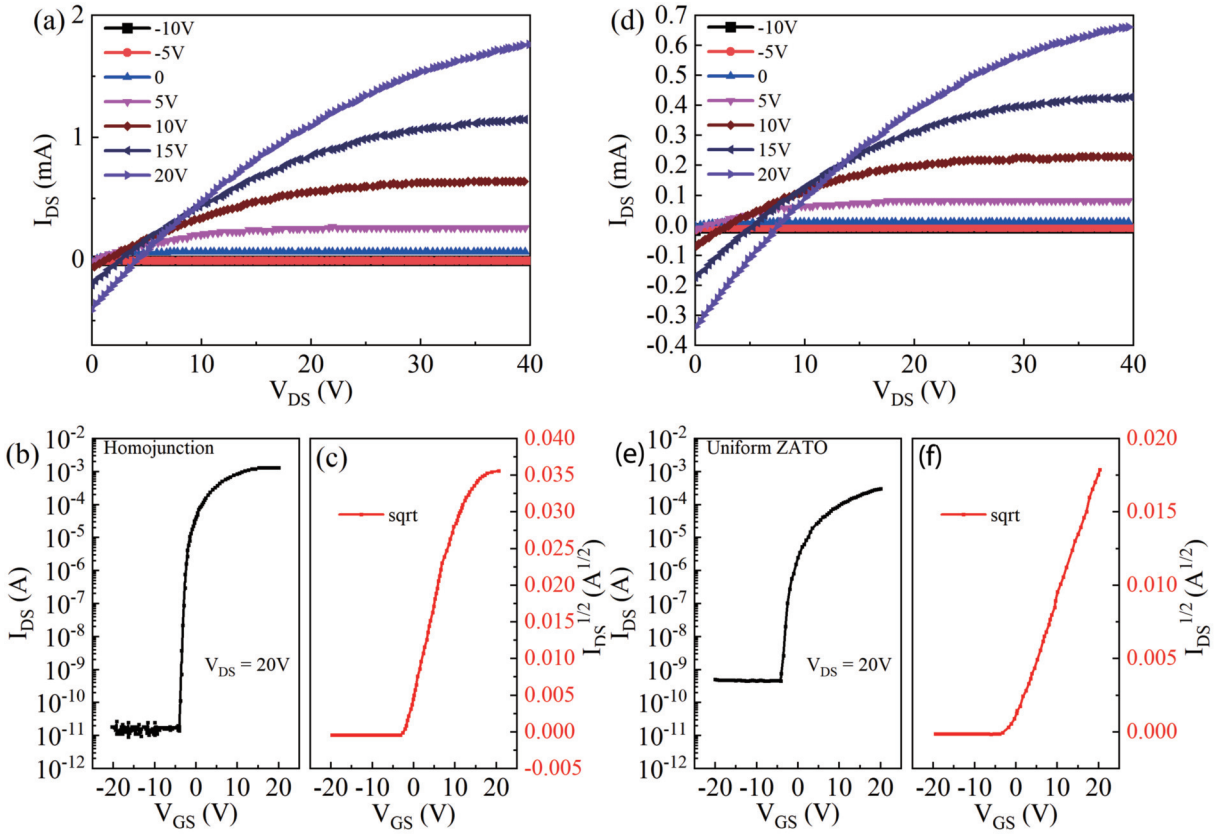

Fig. 3. (Color online) Electrical characteristics of TFTs with different active layers. (a) Output characteristics, (b) transfer curve at V_{DS} = 20 V and (c) the corresponding curve of $I_{DS}^{1/2}$ versus V_{GS} of the TFT device constituted by the homojunction layer. (d–f) TFT with uniform ZATO active layer.

proximately 1021.6, 486.5, and 73.90 eV, indicating Zn–O, Sn–O and Al–O bonds, respectively. Whereas, the O_{I} peak, located at about 530.3 eV, is conventionally related to O^{2-} anions surrounded by metallic elements forming metal-O bonds[24, 25], such as Zn–O, Sn–O and Al–O bonds. The O_{II} peak, located at approximately 531.4 eV, is generally attributed to O^{2-} anions in oxygen-deficient regions, which is proportional to the concentration of V_O. Although some studies have shown that surface defects such as adsorbed oxygen and hydroxyl (-OH) also generate signals at 531.4 eV, oxygen vacancies dominate for amorphous oxides[26, 27]. The O_{III} peak, located at closely 532.3 eV, is assigned to weakly bound oxygen impurities on the surface[28], such as CO_2.

Therefore, it is veritable to reflect the V_O concentration by means of the area ratio of $O_{II}/(O_{I}+O_{II}+O_{III})$. The relative fraction of O_{I}, O_{II} and O_{III} peak is compared in terms of their area ratio with different film samples, as indicated in Fig. 2(d). The V_O percentage of ZTO, ZATO annealed and ZATO unannealed are 36.6%, 28.2% and 20.4%, respectively. Considering that the annealed ZTO films and the ZATO films are protected by the unannealed ZATO films at the surface, the total gas adsorption of the surface is reduced (less O_{III}), which indicates that the O_{II} composition should actually be larger than the measured values. The V_O percentage of ZATO films increases, while the fraction of metal–O bonds (O_{I} area ratio) slightly decreases after annealing, mainly for the reason that the thermal treatment ameliorates the microstructure of ZATO by reducing metal–O bonds (O_{I})[28, 29] through the formation of grain boundaries. In contact with the source and drain electrodes, the ZATO unannealed at the top of the homojunction layer holds a low V_O concentration comparatively leading to a limited carrier concentration, which may move the Fermi level downward[30], reduce off-state current and shift the V_{th} towards the positive direction. In addition, it is worth noting that oxygen deficiencies can mainly form shallow donors and a small amount of deep electron-trap[31]. The shallow donor states can simultaneously enhance carrier transport capabilities, which is positively related to field-effect mobility, while the deep trap states may cause degradation in carrier transport by an excess of charge trapping after prolonged operation of devices at a certain bias voltage[32].

Fig. S3 of the Supporting Information lists the carrier concentration and resistivity of the ZATO film unannealed, the ZATO film annealed at 500 °C and the ZTO film annealed at 900 °C. Each sample in Hall measurement is individually deposited on a SiO_2/Si substrate with the same corresponding process parameters for the homojunction layer. The carrier concentration rises by over three orders of magnitude, from 2.4×10^{16} to 3.7×10^{19} cm^{-3}, after the ZATO film is processed by 500 °C annealing. Thus, the amorphous ZATO film annealed at 500 °C itself shows great potential that it is suitable for preparing TFT devices even as a uniform active layer. However, the ZTO film annealed at 900 °C has a quite high carrier concentration of 1.2×10^{20} cm^{-3}, compared to the ZATO films, which could not bring about a proper off-state current or accessible transfer characteristic. Meanwhile, Hall measurement reveals that the heightened carrier conductivity originates from the enhanced carrier concentration, reflecting that the resistivity of the films is inversely proportional to carrier concentration. The high conductivity of ZTO or Al-deficient region results in the fast transport of the gathered electrons away under positive bias. In summary, the gradient increase

Table 1. Key electrical parameters of TFT devices with distinct active layer.

Layer structure	I_{off} (A)	I_{on}/I_{off}	V_{th} (V)	μ_{sat} (cm^2/(V·s))	SS (V/dec)
Homojunction	~1.5×10^{-11}	8.53×10^7	–1.71	113.8	0.372
Uniform ZATO	~4.9×10^{-10}	6.59×10^5	–2.91	22.9	0.896

of carrier concentration is achieved by the decrease of carrier suppressor concentration and micro-crystallization extent increase in the homojunction layer.

To investigate the electrical performance of TFTs with the homojunction layer, bottom-gate TFT devices were fabricated incorporating with unannealed ZATO, in contrast with uniform ZATO (annealed at 500 °C) device. The representative output characteristics of which are shown in Figs. 3(a) and 3(d), respectively. Obvious current saturation is exhibited in the curves. Moreover, there is no current crowding at a low drain–source voltage (V_{DS}), indicating ohmic contacts at the electrode interface. Homojunction device and homogeneous ZATO device exhibit the same degree of charge trapping. It may be related to gas adsorption on the channel surface, which could be mitigated by encapsulation. Figs. 3(b) and 3(e) exhibit the transfer characteristics of the TFTs at V_{DS} = 20 V. All the devices illustrate typical n-type features and favorable switching properties. The key characteristics of TFTs are summarized in Table 1. Both TFTs show off-current (I_{off}) of less than 10^{-9} A. Among them, the device with a homojunction structure possesses an order of magnitude lower off-current of about 1.5×10^{-11} A than another device due to low carrier concentration at the electrode interface, agreeing with the results of Hall measurements and XPS analysis. The devices fabricated by the homojunction layer have a larger on-current (I_{on}) at the same time, thus, resulting in better switching performance and higher on/off current ratios (I_{on}/I_{off}) of approximately 10^7. The V_{th} and saturation mobility (μ_{sat}) is calculated from drain-source current (I_{DS}) versus gate bias (V_{GS}) according to the following Eq. (1):

$$I_{DS} = \frac{W}{2L} C_i \mu_{FE} (V_{GS} - V_{th})^2, \quad V_{DS} \geqslant V_{GS} - V_{th}, \qquad (1)$$

where C_i is the capacitance per unit area of gate insulator ($C_i = \varepsilon_0 \varepsilon_r / d$). W and L are the width and length of channel. The curves of $I_{DS}^{1/2}$ versus V_{GS} are depicted in Figs. 3(c) and 3(f). The V_{th} of TFT containing the homojunction layer is –1.71 V, while device with uniform ZATO active layer gets a more negative V_{th} of –2.91 V. The V_{th} shifts positively due to the lower V_O concentration at the electrode interface. Moreover, devices with the homojunction layer exhibit extremely high saturation mobility of 113.8 cm^2/(V·s), compared to the TFT incorporating uniform ZATO with a μ_{sat} of 22.9 cm^2/(V·s), an order of magnitude lower than the former. In parallel device tests, as shown in Table S1, the excellent performance of homojunction TFTs can be reproduced with little fluctuations.

Generally, there are three factors dominating the field-effect mobility of AOS TFTs. The first is the magnitude of $4d^{10}5s^0$ orbitals overlap for the carrier transport, which could be improved by thermal-related processes such as annealing. The second is the concentration of carrier suppressor, such as Ga, Zr, Nb, Al, etc.[33–37]. Insufficient carrier suppressor would make V_{th} unduly negative, while excessive carrier suppressor would exacerbate the carrier scattering effect resulting in mobility decrease. Therefore, it is quite difficult to obtain mobility higher than 100 cm^2/(V·s) for TFTs with uniform AOS active layer. The third point is grain boundary concentration. For covalent semiconductors such as polysilicon, carriers need to overcome the potential barrier at the grain boundary through thermal excitation, resulting in increased charge scattering[38]. The charge scattering in covalent semiconductors intensifies as the grain boundary concentration increases, limiting mobility. However, when it comes to ionic semiconductors dominated by percolation conduction, such as ZTO and ZATO, carriers are able to bypass the barrier at the grain boundary rather than overcome it. In this case, the adverse effect of grain boundaries on mobility will be greatly reduced. The TFT devices using the homojunction active layer break this intrinsic limitation by designing micro crystallization extent and carrier suppression concentration gradient with depth, decoupling channel opening from carrier transport to achieve high field-effect mobility. It provides a new carrier transport mechanism for the channel, which is detailed below. All these make the field-effect mobility of the TFT devices with the homojunction layer improved by an order of magnitude, compared to traditional AOS TFTs[39–41].

The subthreshold swing (SS) is calculated by the Eq. (2) below[42]:

$$SS = \left[\frac{d \log (I_{DS})}{d V_{GS}} \right]^{-1}. \qquad (2)$$

The subthreshold swing (SS) is related to the interfacial trap states of the channel-insulator interface, reflecting the required voltage span of the device from off to on. The SS values of the TFT devices incorporating the homojunction layer and with a uniform ZATO active layer are 0.372 and 0.896 V/dec, respectively. The SS values suggest the homojunction layer has less trap density at the channel-SiO_2 interface than annealed uniform ZATO active layer, probably due to the lack of Al element[43]. In general, the TFT with the homojunction layer has high field-effect mobility of over 100 cm^2/(V·s), and exhibits optimized comprehensive electrical properties with lower I_{off}, higher I_{on}/I_{off} ratio, smaller absolute V_{th} value and slightly smaller SS value.

To further explain the high field-effect mobility, schematic diagrams of the conducting path of charge carriers in the uniform active layer and the homojunction layer are shown in Fig. 4. In a traditional TFT device, the shape of the "conductive channel" is influenced by the gate voltage. With the increase of a positive V_{GS} applied on the gate terminal, the majority of carriers begin to accumulate at the interface between the active layer and gate insulator. Meanwhile, the channel resistance from source to drain decreases, until carriers could flow easily. The conducting path of carriers during saturation mode are illustrated in Fig. 4(a). Therefore, saturation mobility (μ_{sat}) is affected by two processes, not only the carrier velocity conducting in the channel but also the rate of majority carrier accumulation. The carriers conducting path in

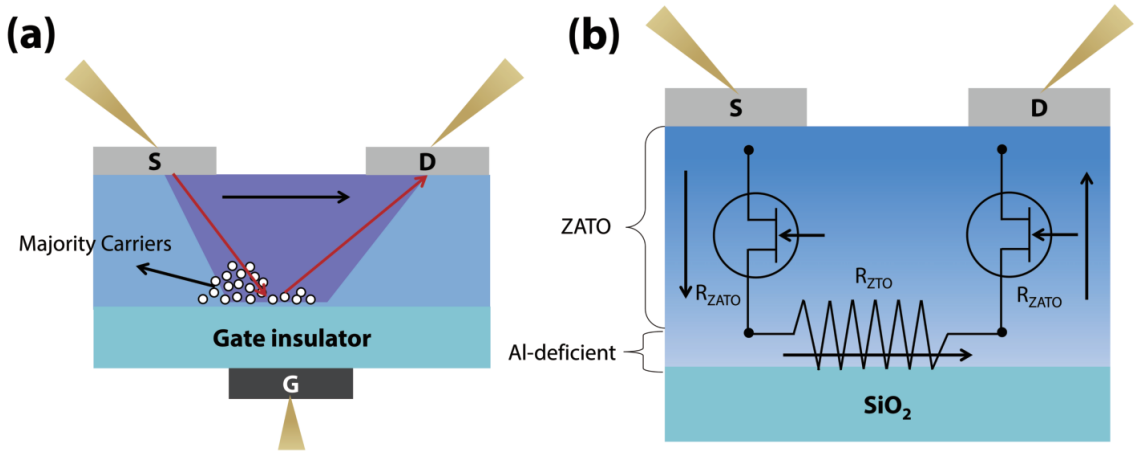

Fig. 4. (Color online) Conduction mechanism through the homojunction layer. (a) Schematic diagram of the carrier conducting path of a traditional TFT with uniform active layer during saturation mode. (b) Carrier transport model of homojunction structured amorphous oxide TFT.

the homojunction layer differs from the uniform active layer, due to the low resistivity of the Al-deficient bottom layer contacted with the gate insulator.

We established an applicable model, as shown in Fig. 4(b). The carriers conducting path of the homojunction layer could be summarized as "unannealed ZATO"–"Al-deficient region"–"unannealed ZATO", which improves the mobility of carriers greatly. According to the existence of micro crystallization and carrier suppression concentration gradient distribution in the homojunction layer, there is a gradient distribution of carrier concentration, which makes it easier and faster for the majority of carriers to accumulate at the gate interface than the device with the uniform active layer. Once the carriers gather, there is unnecessary to form a channel for transmission since carriers would be transported away through the low-resistance Al-deficient region under drain-to-source voltage. It is the main reason for drastically increasing μ_{sat} by an order of magnitude than the control device. Additionally, the thickness of the active layer has to be limited to a certain range, according to Thomas–Fermi screening[43]. As the thickness of the unannealed ZATO increases, the effects of trapped charges become shielded, which reduces carrier scattering and therefore increases field-effect mobility. However, further increasing the thickness will increase the resistance[44]. The charge injection mainly happens in the unannealed ZATO region so that field-effect mobility will be limited by the carrier vertical transport from the electrode interface to the gate interface. The field-effect mobility begins to decrease when further increasing the thickness of the active layer[45]. Therefore, to maintain high field-effect mobility, the thickness of the homojunction layer has to be suitable.

To verify the above analysis, the overall thickness of the homojunction layer is increased by controlling the sputtering time of unannealed ZATO (0, 5, 7.5, and 10 min). The overall active layer thickness of samples corresponding to 7.5 and 10 min has increased by 13.9% and 27.8% compared to the 5 min sample. The transfer characteristics of the corresponding TFTs at V_{DS} = 20 V are shown in Fig. S4 of the Supporting Information. With the increase in thickness, the μ_{sat} decreases to 80.8 cm^2/(V·s) (7.5 min) and 10.9 cm^2/(V·s) (10 min), which reveals that the overall thickness of the homojunction layer should not exceed a certain limit. This model could be used to explain the mechanism of some other reported TFTs with high field-effect mobility[46] and provide theoretical support for further improving TFT performance.

4. Conclusion

In summary, we designed amorphous oxide thin-film transistors with the homojunction structure to obtain high field-effect mobility of more than 100 cm^2/(V·s). The homojunction active layer is manufactured in the following order: 3 nm ZTO annealed at 900 °C, 10 nm ZATO annealed at 500 °C, and 5 nm ZATO unannealed. It is worth emphasizing that a gradient of the micro-crystallization extent and carrier suppressor concentration is formed in the homojunction layer with depth, which causes the carrier concentration to gradually increase from the electrode interface to the gate interface. Therefore, the device with the homojunction layer demonstrates optimized comprehensive electrical properties with a low I_{off} of about 1.5 × 10^{-11} A, a high I_{on}/I_{off} ratio of approximately 8.53 × 10^7, a V_{th} of –1.71 V, a high μ_{sat} of 113.8 cm^2/(V·s) and a small SS of 0.372 V/dec. The lower carrier concentration near the electrode interface could reduce off-state current effectively and shift the V_{th} positively. Moreover, the accumulated carriers could be transported away immediately at V_{DS} through the low-resistance Al-deficient layer without traditional channel formation resulting in high mobility. Notably, the homojunction active layer opens new opportunities for AOS TFTs with excellent device performance, especially high field-effect mobility.

Acknowledgements

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Appendix A. Supplementary materials

Supplementary materials to this article can be found online at https://doi.org/10.1088/1674-4926/44/052101.

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