RESEARCH HIGHLIGHTS

Journal of Semiconductors
(2023) 44, 050205
doi: 10.1088/1674-4926/44/5/050205

CMOS phase-locked loops in ISSCC 2023

Zhao Zhang[1, 2, †]

[1]State Key Laboratory of Superlattices and Microstructures, Institute of Semiconductors, Chinese Academy of Sciences, Beijing 100083, China
[2]Center of Materials Science and Optoelectronics Engineering, University of Chinese Academy of Sciences, Beijing 100049, China

Citation: Z Zhang, CMOS phase-locked loops in ISSCC 2023[J]. *J. Semicond.*, 2023, 44(5), 050205. https://doi.org/10.1088/1674-4926/44/5/050205

High-performance phase-locked loops (PLL) are widely used in modern system-on chips (SoC) including the ultra-high-speed wireless/wireline communication (e.g. 5G/6G transceivers, over-100-Gbps SerDes transceivers), high resolution mm-wave radars, ultra-low power internet-of-thing (IoT), and high-sampling-rate data converters. In the 2023 IEEE International Solid-State Circuits Conference (ISSCC 2023), 7 PLLs[1–7] have been reported, which refresh prior state-of-the-art PLLs' performances in terms of integrated jitter, spur, covered frequency range, and lowest supply voltage. According to these works, several design trend can be obtained as follows.

Design trend I: PLLs with digital-intensive calibration

In ISSCC 2023, it is becoming a significant trend that the performances improvements of the PLL, including the analog charge-pump based PLL (CPPLL)[1], sub-sampling PLL(SSPLL)[2] and all-digital PLL (ADPLL)[3–5], rely more and more on the digital calibration algorithms. Based on the LMS algorithm with several dedicated circuits design, the fractional spur of low-jitter ADPLL can be reduced, the nonlinearity of the VCO in a PLL-based FMCW frequency synthesizer can be overcome to improve modulation bandwidth[1], the quantization noise of the fractional-*N* PLL can be significantly reduced[2–5], and the equivalent reference frequency of the PLL can be multiplied by more than 100 times to enable the adoptation of a 32-kHz low-frequency reference clock without significant performance degradation[4].

Since the analog circuit performance is limited by the nonidealities more with advanced CMOS process, such as sub-10-nm FinFET process, developing new digital calibration algorithm with low circuit power is significant to further break the performance limitation of the PLL in the future.

Design trend II: Cascaded PLL architecture

A PLL achieving wide frequency tuning range (FTR), low jitter and low power concurrently is essential for multi-band wireless communication or multi-standard wireline communication. Conventionally, a wideband PLL with low jitter performance is usually implemented in a PLL with multiple LC voltage-controlled oscillators (VCO) or a LC-VCO with complicated resonance network, leading to large area, high power and design complexity. Although ring VCO (RVCO) based PLL can easily achieves wide FTR with compact area and low power, its jitter is usually worse than the LC counterpart. Hence, to break this trade-off, a wideband frequency synthesizer, which consists of two cascaded PLLs, has been reported in ISSCC 2023[2]. In such work, the first stage is a fractional-NLC-based SSPLL with narrow FTR to generate a GHz reference clock for the second stage PLL with low-jitter and high frequency resolution, and the second stage is a ring PLL, which can easily cover wide frequency range with low power. Since the reference frequency of the ring PLL is sufficiently high (> 1 GHz), an ultra-wide loop bandwidth can be selected to significantly suppress jitter of the RVCO, thus achieving low clock jitter with low power and wide FTR concurrently.

As observed, cascaded phase-locked loops can combine the advantages of several kinds of single-loop PLLs; thus, it has more optimization dimensions compared with the conventional single-loop PLL. Therefore, it can be an important trend to further improve other performances of the PLL by fully utilizing this feature.

Design trend III: Reference clock frequency multiplication

Low frequency reference f_{REF} clock source, such as a 32-kHz crystal oscillator, is highly desirable for the PLL design with low cost. However, the maximum allowable loop bandwidths of most of the PLLs are around 1/10 of the reference frequency, thus severely degrades the PLL performances in terms of clock jitter, spur level and settling time. Hence, the oversampling PLL (OSPLL) architecture has been proposed to address this issue[4]. In the OSPLL, the phase detection is performed by sampling the voltage of the low-frequency input clock with sampling frequency M times of f_{REF} (M is 256 in Ref. [4]) first, and then comparing the sampled voltage with a look-up table. Thus, the equivalent reference frequency can be boosted to gain a performance comparable to other high-f_{REF} PLLs.

Besides the PLL with low-f_{REF}, reference frequency multiplication technique is also demonstrated in an over-100-GHz PLL[6] with an ultra-low jitter of sub-50 fs_{rms}, in which an ultra-wide loop bandwidth of ~50 MHz can be achieved to sufficiently suppress the output jitter of the VCO.

Since the PLL performance relies much on the f_{REF}, the low-cost and low-jitter f_{REF} multiplying technique is significant for different types of PLL, especially at the case of low f_{REF}.

Design trend IV: Ultra-low voltage high-performance PLL

Ultra-low-voltage (ULV) PLL design is highly desirable for internet-of-thing (IoT) applications, especially for the system powered by the harvested energy, because the output voltage of the energy harvester is usually below 0.4 V, and reducing supply voltage is an effective way to lower down the power of digital-centric SoCs. Since prior sub-0.5-V ULVPLL mainly focus on the low-power design techniques, the rms jitters of these PLLs are higher than 500 fs, thus preventing them from being adopted in an IoT communication SoC such

Correspondence to: Z Zhang, zhangzhao11@semi.ac.cn
Received 26 APRIL 2023.

as blue tooth RF transceiver.

In ISSCC 2023, a sub-0.4-V PLL achieving a low jitter of 236.6 fs and a low power of 0.74 mW has been reported[7]. The triple-path SSPLL architecture was reported to maintain sufficient frequency tuning range. Several circuit techniques were devised to reduce the stacked number of MOSFETs. Hence, the operation statues of these ULV circuit blocks can be similar to the conventional circuits operating at regular supply (around 1 V) to achieve low-jitter performance.

As observed, multi-path PLL, instead of the single-path PLL, can be popular because its design parameters can be decoupled with each other and can be optimized more flexibly. Thus, high-performance PLL design becomes possible at sub-0.4-V voltage, and the supply voltage can be shrunk further with high possibility.

Summary

As discussed previously, PLLs reported in ISSCC 2023 shows several design trends, including design digit- al-intensive calibration, cascading several stage PLLs with dif- ferent architectures, performance improvement with refer- ence frequency multiplication, and high-performance design with lower supply voltage using multi-path architectures. Hence, in summary, the PLL future performance improve- ments rely more and more on the architecture and circuit in- novation rather than new process.

Acknowledgments

This work was supported by the National Natural Science Foundation of China (Grant Nos. 62222409 and 62174153), and Beijing Municipal Science and Technology Project (Grant No. Z211100007921019).

References

[1] Renukaswamy P T, Vaesen K, Markulic N, et al. A 16GHz, 41kHz$_{rms}$ frequency error, background-calibrated, duty-cycled FMCW charge-pump PLL. IEEE International Solid-State Circuit Conference, 2023, 68

[2] Jo Y, Kim J, Shin Y, et al. A 135fs$_{rms}$-jitter 0.6-to-7.7GHz LO generator using a single LC-VCO-based subsampling PLL and a ring-oscillator-based sub-integer-*N* frequency multiplier. IEEE International Solid-State Circuit Conference, 2023, 71

[3] Dartizio1 S M, Tesolin F, Castoro1 G, et al. A 76.7fs-integrated-jitter and -71.9dBc in-band fractional-spur bang-bang digital PLL based on an inverse-constant-slope DTC and FCW subtractive dithering. IEEE International Solid-State Circuit Conference, 2023, 74

[4] Qiu J, Wang W, Sun Z, et al. A 32kHz-reference 2.4GHz fractional-*N* nonuniform oversampling PLL with gain-boosted PD and loop-gain calibration. IEEE International Solid-State Circuit Conference, 2023, 77

[5] Castoro G, Dartizio S M, Tesolin F, et al. A 9.25GHz digital PLL with fractional-spur cancellation based on a multi-DTC topology. IEEE International Solid-State Circuit Conference, 2023, 80

[6] Bang J, Kim J, Jung S, et al. A 47fs$_{rms}$-jitter and 26.6mW 103.5GHz PLL with power-gating injection-locked frequency-multiplier-based phase detector and extended loop bandwidth. IEEE International Solid-State Circuit Conference, 2023, 83

[7] Zhang Z, Shen X, Zhang Z, et al. A 0.4V-V_{DD} 2.25-to-2.75GHz ULV-SS-PLL achieving 236.6fs$_{rms}$ jitter, -253.8dB jitter-power FoM, and -76.1dBc reference spur. IEEE International Solid-State Circuit Conference, 2023, 86

Zhao Zhang received the B.S. degree from Beijing University of Posts and Telecommunications, Beijing, China, in 2011, and the Ph.D. degree from Institute of Semiconductors, Chinese Academy of Sciences (IOSCAS), Beijing, China, in 2016. Since 2020, he joined in the IOSCAS, Beijing, where he is currently a Full Professor. He has gained National Science Fund for Excellent Young Scholars from NSFC in 2022, and he is the associated editor of IET Electronics Letters. His research interests include the design of wireline transceivers, low-jitter and low-power PLLs, and ultra-low voltage ICs for bio/energy-harvesting applications.