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RESEARCH HIGHLIGHTS

Emerging trends of integrated-mixed-signal chips in ISSCC 2023

Jinbo Chen, Jie Yang†, and Mohamad Sawan†

CenBRAIN Neurotech, School of Engineering, Westlake University, Hangzhou 310024, China

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In February 2023, the annual 'Olympic' of the chip industry, ISSCC, returned to in-person meetings in San Francisco. As shown in Fig. 1, from the ISSCC 2023, we can see that the trend in IC design has shifted from pure digital to mixed-signal design, particularly in areas such as AI accelerator chips and quantum computing. Chips have also evolved from integrated circuits to integrated chips through module-level, function-level, and chip-level fusion, with compute-in-memory being the best embodiment of module-level and function-level fusion. Moreover, quantum computing was one of the major focuses of this ISSCC edition, with a separate paper session dedicated to cryo-CMOS for quantum computing. This emphasis on quantum computing may indicate that quantum chips are poised to make a big impact and could potentially spark a paper revolution like the compute-in-memory topic. To address the gap between academia and industry, ISSCC 2023 also introduces a new lecture session for innovations outside the traditional focus on solid-state circuits.

Trend I: Walk in the middle of analog and digital

Digitalization has been the main theme of IC development in the past 70 years[2]. However, with the slowing down of Moore's Law, the technology roadmap of continuously scaling the chip performance through process has gradually become unsustainable. In recent years, the trend of chip design, especially in computing chips, has gradually shifted from pure digital to mixed-signal design, particularly in areas such as AI accelerator chips and quantum computing chips. What is the underlying logic of this change in development trend?

Bell's Law, proposed by Gordon Bell in 1972, states that every ten years, a new generation of computers (new programming platforms, new network connections, new user interfaces, and new usage patterns) will emerge, forming a new industry. The new generation of computers has new computing power characteristics, which pose new demands on chips and promote continuous innovation in bottom-level hardware chips. The computing power characteristics and demands of different eras determine the continuous evolution of chip product development modes, which is reflected in Makimoto's Wave. In 1987, Tsugio Makimoto, former chief engineer of Hitachi, proposed that the development of semiconductor products always alternates between standardization and customization, fluctuating about every ten years. The underlying balance between performance/power consumption and development efficiency behind Makimoto's Law is more of a rule refined through the product development cycle of the industry.

Correspondence to: J Yang, yangjie@westlake.edu.cn; M Sawan, sawan@westlake.edu.cn

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Based on Bell's Law and Makimoto's Wave, designers explore the fundamental rules for the advancement of chips. The evaluation of chips mainly depends on the 'PPA' indicators: power, performance, and area. In the era of general-purpose computing dominated by CPUs, low power consumption and high performance (high precision) are difficult to achieve at the same time, with high performance (high precision) taking priority. Looking to the future, AI computing and quantum computing are becoming favorable supplements to CPU general-purpose computing. One major characteristic of AI computing and quantum computing is the reduced demand for data precision, which makes low-power computing based on relatively low-precision analog and mixed-signal chips possible and unifies low-power consumption and high performance in new-generation chips. Under this new underlying logic, a wave of innovative papers is emerging, with representative papers including JSSC 2019[3], IEEE Solid-State Circuits Magazine 2021[4], ISSCC 2023[5], and more.

Looking to the future, as one of the ISSCC 2023 plenary talk speakers, Prof. Akira Matsuzawa said, "In the future, it will be important to develop computers such as AI processors and quantum computers whose operations are essentially analog, so mixed-signal technology is expected to develop even further."

Trend II: From integrated-circuits to integrated-chips

Based on the fundamental rules for the advancement of chips mentioned earlier, chips have evolved from integrated circuits to integrated chips, characterized by module-level fusion, function-level fusion, and chip-level fusion. The three levels fusion support each other and form a combined force to drive the innovation and development of the next generation chips.

Module-level fusion is driven by demand in different scenarios. It integrates the functions of different circuit modules traditionally implemented into a single circuit module to achieve function fusion and performance breakthroughs. The recent development of the analog front-end signal processing SoC exemplifies this technology trend.

For example, in wireless communication scenarios, one of the latest technology trends is to integrate the functionality of the traditional receiver mixer into the ADC. Through a high-performance ADC, the A/D sampling and RF received signal demodulation can be achieved simultaneously. One representative reference paper is JSSC 2020[6].

Module-level fusion is also reflected in the low-power front-end acquisition of biological signals, where a high dynamic range and low-noise delta-sigma ADC breaks the traditional architecture about amplifier connected with ADC, enabling low-power, small area, and high-precision biological signal acquisition[7]. Representative reference papers in ISSCC 2023 are Ref. [8–10].

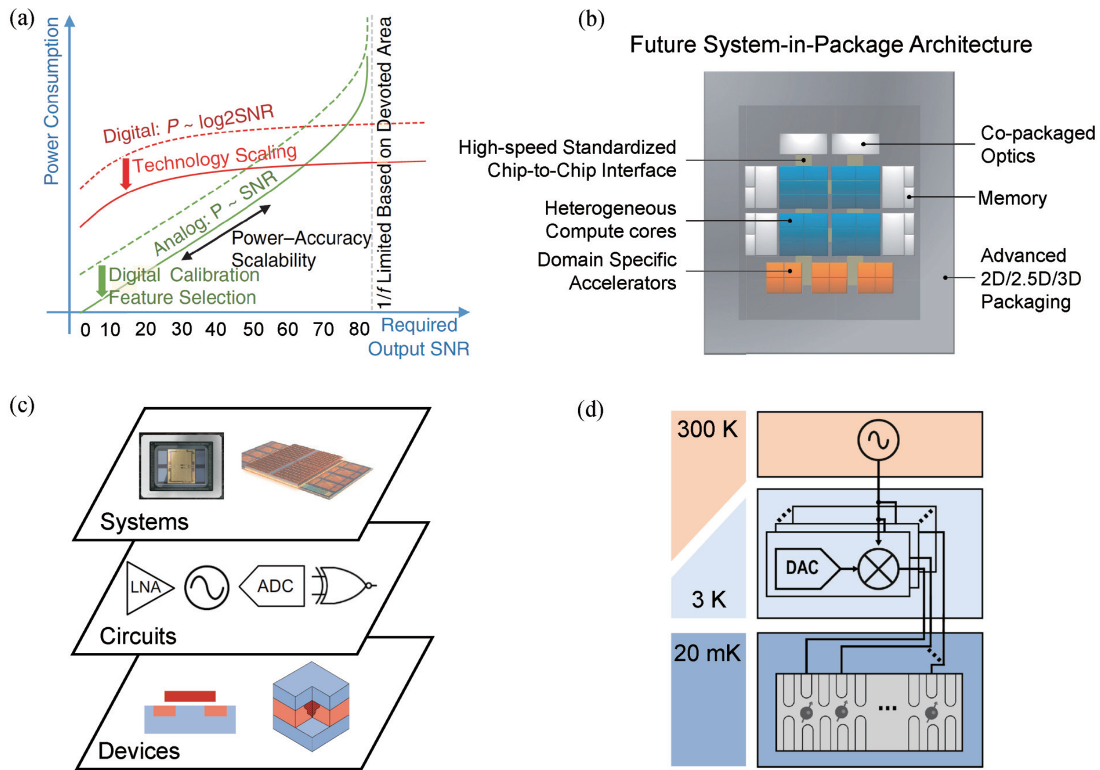

Fig. 1. (Color online) Emerging trends of integrated-mixed-signal chips in ISSCC 2023: (a) Walk in the middle of analog and digital[1]; (b) From integrated-circuits to integrated-chips; (c) Cross-layer innovation of devices, circuits, and systems; (d) Quantum computing chips become the spotlight.

The analog signal processing chip for quantum computing also reflects the trend of module-level fusion. Specifically, this trend is manifested by bringing qubits and control electronics closer together, integrating switch capacitor circuits and qubits, and packaging analog signal processing chips and qubit chips together on a PCB.

Compute-in-memory is one of the best embodiments of module-level fusion and function-level fusion, with the number of papers published each year at ISSCC continuing to break records. Compute-in-memory integrates the independent modules of computation and storage that are separated in the traditional von Neumann architecture, reducing the power consumption and time overhead caused by data movement during computation and achieving low-power, high-performance computing. In ISSCC 2023, two sessions (Session 7, Session 16) are dedicated solely to compute-in-memory and both are long sessions, which demonstrates a high level of research interest[11].

For the fusion of a chip level, it is mainly manifested by chiplet and advanced packaging technologies. ISSCC 2023 presents chiplet development in AMD (Advanced Micro Devices, Inc.) 5-nm microprocessor[12], Samsung Electronics 23-Gb/s transceiver in 4-nm CMOS[13], Tsinghua University 28-nm TensorCIM processor with chiplet multichip module (MCM)[14]. Chiplet technology is also emphasized by Lisa Su in her plenary talk this year: "It is increasingly attractive to use modular chiplet architectures where the most advanced nodes are only used for the most compute-heavy IP which get the most gains from using the latest technology, and less advanced nodes are used for the IO and other functions that do not benefit as much from the most-advanced node. To continue advancing chiplet architectures over the next decade, innovation around the die-to-die interconnect is critical". Through chiplet, integrated chips that break through computing and functional limits can be achieved.

Trend III: Cross-layer innovation of devices, circuits, and systems

ISSCC 2023 introduced a new paper session 27 for the first time: Innovations from outside the (ISSCC) box, which breaks away from the traditional focus on solid-state circuits at ISSCC and covers topics such as molecular programmers, 2D materials, and photonic quantum computing.

Despite the constant emergence of new chip products, the slowing of Moore's Law has become a major trend. Against this backdrop, innovation at only chip-level may be more about engineering optimization rather than revolutionary new principles, technologies, or architectures. The industry has abundant resources and is suitable for engineering optimization, constantly launching new products to meet market demand. In contrast, academia to ensure innovation often only has one Ph.D. student working on a single chip, with far less engineering investment than a team in a large company. This creates a gap between academia and industry in IC design.

The ISSCC organizing committee may have recognized this growing problem and attempted to introduce an "outside ISSCC box new session" that breaks people's traditional perceptions of ISSCC paper styles. Regarding this issue, the International Technical-Program Chair for ISSCC 2023 mentioned in the conference proceedings foreword: "ISSCC is, despite of its age, looking to the future, seeking innovative designs more than ever. This goes hand in hand with perform-

ance advances of state of the art. The conference emphasizes this with two highlighted sessions of invited papers, one with out-of-the-box ideas and one with chip releases from industry."

Trend IV: Quantum computing chips become the spotlight

Quantum computing is the theme of this year's ISSCC short course, and compared to 2022, a separate quantum computing session (Session 34: Cryo-CMOS for quantum computing) has been added to the paper sessions, which is sufficient to demonstrate the organizing committee's emphasis on quantum computing.

At ISSCC 2020 and 2021, quantum computing had its own regular paper session. However, at last year's ISSCC 2022, quantum computing only had an invited paper session: Highlighted chip releases: Systems and quantum computing, and there was no regular paper session. This year, the content related to quantum computing has increased significantly, which may indicate that quantum chips are poised to make a big impact and could potentially spark a paper surge like that of compute-in-memory.

In conclusion, from ISSCC 2023, the development of computing chips has shifted from pure digital to mixed-signal circuit design alternative, particularly in areas such as AI and quantum computing chips. AI and quantum computing paves the way to low-power computing based on relatively low-precision analog and mixed-signal circuit chips, making it possible to unify low-power consumption and high performance in the new-generation chips. Moreover, Chips have evolved from integrated circuits to integrated chips, characterized by module-level fusion, function-level fusion, and chip-level fusion, which drive the innovation and development of the next generation chips. Additionally, the new innovations from outside the (ISSCC) box session at ISSCC 2023 firstly covers topics such as molecular programmers, 2D materials, and photonic quantum computing. Quantum computing is also in the spotlight at ISSCC 2023, with a short course and a separate paper session. The emphasis on quantum computing may indicate that quantum chips are poised to make a big impact and could potentially induce a paper rise like compute-in-memory.

Acknowledgments

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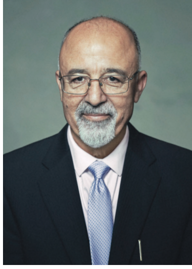
Jinbo Chen received the B.S. degree in Electronic Information Engineering from Beihang University, Beijing, China in 2020. In August 2020, he joined the Center of Excellence in Biomedical Research on Advanced Integrated-on-chips Neurotechnologies (CenBRAIN Neurotech), Westlake University, where he is currently pursuing the Ph.D. degree. His research interests include closed-loop brain-machine interface SoC and emerging neuromorphic systems.

Jie Yang is a research associate professor at Westlake University School of Engineering. He received his B.S. degree from Tianjin University in 2010 and his Ph.D. degree from the Chinese Academy of Sciences in 2015. He worked as a post-doctoral fellow at the University of Calgary from 2015 to 2019 and joined CenBRAIN Neurotech at Westlake University in 2019. His current research interests include novel SoC for intelligent biomedical applications, brain-machine interface, energy-efficient AI algorithms and VLSI architecture. He has designed different types of image, video signal processing chips and image sensors chips under advanced technologies.



Mohamad Sawan Fellow of the Canadian Academy of Engineering, Fellow of the Engineering Institute of Canada, Fellow of the Royal Society of Sciences of Canada, Fellow of the IEEE, is an internationally renowned scientist in the field of smart medical devices. He has made significant contributions in implantable and wearable medical devices based on smart microsystems. Professor Sawan got a Ph.D. in Electrical Engineering from University of Sherbrooke in 1990, was a postdoc fellow in Biomedical Engineering in McGill University in 1991, and was assistant professor, associate professor and full professor from 1991 to 2018 in Polytechnique, the Engineering School of University of Montreal. He joined the School of Engineering of Westlake University as a Chair Professor in 2018, he is the Founder and Principle Investigator in the Center of Excellence in Biomedical Research on Advances-in-Chips Neurotechnologies (CenBRAIN Neurotech) in Westlake University.