RESEARCH HIGHLIGHTS

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Digital-intensive RFIC design techniques for transmitters in ISSCC 2023

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Sub-6 GHz multi-standard wireless communication and millimeter-wave (mm-wave) wireless transmission provide users with multi-functionality and unprecedented wireless connectivity. With CMOS process scaling down, system-on-chip (SoC) implementation of wireless systems along with RFIC functionality is highly desirable for low cost and small form-factor. The digital transceiver architecture aligns with Moore's law to provide compact die area, better interface to digital backend and higher efficiency due to the faster switching nature of core devices[1–28].

The digital PA (DPA) plays a dominant role in digital transmitters (DTXs), which performs digital-to-analog conversion, frequency up-conversion and power amplification all-in-one. Since modern wireless standards widely adopt orthogonal frequency division multiplexing (OFDM) and high-order quadrature amplitude modulation (QAM) to increase throughput and spectral utilization, it requires the DPA to achieve high output power (e.g., >30 dBm), high linearity and high efficiency especially at back-off power levels.

Relevant intensive researches at sub-6 GHz have been directed toward class-D based switched-capacitor PAs, which are more amenable to CMOS scaling and have good linearity and efficiency due to fast low-loss switches and precise capacitor matching. In ISSCC 2023, two works on sub-6 GHz DTX/DPA came from Fudan University[5, 7]. In Ref. [5], a single-channel quadrature DTX supporting multi-mode multi-band NB-IoT/BLE applications is proposed. It introduces a sliding digital-IF quadrature architecture to replace the fractional upsampling module and achieve pure output spectrum. Besides, a compact wideband Doherty DPA with IQ cell-sharing is implemented to enhance output power and back-off efficiency. This multi-mode NB-IoT/BLE DTX chip achieves Watt-level peak power with >40% system efficiency while occupying only 0.79 mm^2 core area, which is well-fitting low-cost IoT applications.

In Ref. [7], a 4.1 W quadrature DPA with 33.6% peak PAE in 28 nm bulk CMOS is presented. It introduces the cascode and 8-way differential power-combining techniques to enhance output power by 16 times. Besides, the IQ cell-sharing and transformer-based Doherty techniques are introduced to further enhance output power by 2 times and achieve 12 efficiency peaks in the complex domain. Powered by 1.1 V/2.2 V supply voltages and packaged in an QFN format, this DPA chip achieves 4.1 W peak power and close-to-Watt-level average power with competitive efficiency performance even compared with polar DPAs, which is very attractive for compact and fast system integration in 5G applications.

mm-wave wireless transmission with multi-Gb/s data rate also demands wideband signal processing, high system efficiency and high output power for large coverage. In ISSCC 2023, a 71–89 GHz DPA came from University of Electronic Science and Technology of China[26]. In Ref. [26], the double-edge-triggered technique is proposed to double the signal bandwidth with limited sampling clock. Besides, the LO leakage suppression and balance-compensated power-combining techniques are introduced to enhance linearity and efficiency. Implemented in 40 nm CMOS, this mm-wave DPA obtains 12 Gb/s high-speed data rate, 20.5 dBm peak output power and 20.4% system efficiency, which is quite competitive for E-band wireless applications.

Moreover, two DTX works are implemented for FMCW chirps from Infineon Technologies[27] and low-power cryogenic controller IC design from Tsinghua University[28]. In Ref. [27], accurate frequency modulation of a direct digital frequency synthesizer is combined with the RFDAC to generate precise wide-bandwidth frequency ramps, which achieves 4 GHz modulation bandwidth with <3 dB power variation. In Ref. [28], a polar architecture with DPA-based amplitude modulation and injection-locking LO based phase modulation is proposed. Its power consumption is 13.7 mW per qubit under active control and the average chip area per channel is only 0.9 mm^2.

In Table 1, various DTX/DPAs operating from sub-6 GHz to mm-wave bands with multi-mode multi-band, output power, good efficiency, linearity and bandwidth have been summarized. With these advanced metrics, the digital RF front-end will be a good candidate for modern and further wireless applications.

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Table 1. Performance metrics of DTX/DPAs at sub-6 GHz and mm-wave bands (2019–2023).

Performance metric	System effect	Architecture/design technique
Multi-mode Multi-band	Flexibility and low cost	Quadrature/polar dual-mode reconfigurable[2]; wideband DTC/DPC-based phase modulation[3, 4]; sliding digital-IF quadrature DTX[5]
Output power	Communication range	Power combining with stacked device[6, 7]; multiphase beamforming[8]; IQ cell-sharing[9]
Power efficiency	Battery life	Time-interleaving Doherty class-G[10]; switched transformer[11]; multi-subharmonic switching[12]; class-G[13, 14]; Doherty[15]; complex-domain Doherty [9]; hybrid Doherty and impedance boosting[16, 17]; class-G Doherty[18]
Linearity	Data error rate and modulation type	Phase nonlinearity compensation[15]; switch impedance linearization and code mapping[19]; ADC background correction[20]; tri-phasing modulation[21]
Signal bandwidth	Data rate and license cost	Dual-band matching[22, 23]; edge combining class-D[24]; mm-wave power-DAC [25]; doubled-edge- triggered RFDAC[26]

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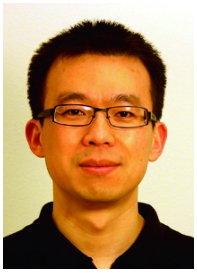

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