## **RESEARCH HIGHLIGHTS**

# CMOS image sensors in ISSCC 2023

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In IEEE International Solid-State Circuits Conference (IS-SCC) 2023, CMOS process is still the dominating fabrication technology for image sensors, and three-dimensional (3D) wafer-stacked process with Cu–Cu pixel-level connection has been adopted to achieve small pixel size and high integration level. The development of CMOS image sensors (CIS) is still focusing on the trends of high performance and more functionalities, such as hybrid event-based vision sensor (EVS) and terahertz (THz)/X-ray image sensor.

### (a) Hybrid event-based vision sensors

EVS can output pixel-level information if a temporal contrast change beyond threshold is detected, together with the feature of data-compression. It enables high-speed, lowlatency and low-power operation, and is efficient for capturing motion information. The pixel of EVS usually comprises amplifier, sampler, comparator, and logic circuitry, which leads to a complex pixel structure and large pixel pitch. For this reason, three-dimensional wafer-stacked process with Cu–Cu pixel-level connection has been used to reduce the pixel pitch and improve its performance.

In Ref. [1], the hybrid EVS/CIS macro pixels realized in top wafer are connected to the EVS readout circuit and time-to-digital converter (TDC) on the middle wafer, and the analog-todigital converter (ADC), event signal processor (ESP), image signal processor (ISP), MIPI interface on the bottom wafer. This sensor with 15M CIS pixels and 1M EVS pixels reaches a readout speed of 4.6G events/s and 8.8  $\mu$ m EVS pixel pitch. Ref. [2] also proposed an image sensor with 35.6M CIS pixels and 2.08M EVS pixels which achieves 10K event frame rate with 4.56G events/s by adaptive control method on event sparsity. Its EVS pixel pitch is 4.88  $\mu$ m. Another hybrid EVS sensor achieves 1.41G events/s with 2.97  $\mu$ m pixel pitch and resolution of  $640 \times 640$  by shared pixel front-end circuitry<sup>[3]</sup>. All of those three sensors have been realized with either three or dual wafer-stacked back-illuminated process. Compared with the EVS only sensor reported in ISSCC 2020, which achieved 1.066G events/s with pixel pitch of 4.86  $\mu$ m and resolution of  $1280 \times 720^{[4]}$ , these hybrid EVS sensors output either intensity frames or event frames<sup>[1-3]</sup>, achieve higher EVS resolution<sup>[1, 2]</sup> or smaller pixel size<sup>[3]</sup>, and improve the event readout speed greatly [1-3].

## (b) Terahertz (THz)/X-ray image sensors

The existing atmosphere absorption notches in the 3-

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4 THz frequency band provides promising applications owing to its nondestructive features. In Ref. [5], a 16.4k pixel THz image sensor with 73 dB dynamic range has been realized. This sensor adopts column-parallel readout architecture with oversampling and chopping to balance speed and noise. In this sensor, a 2T pixel with step-covered patch antenna and defected ground structure have been proposed to achieve a sensitivity of 753 V/W at 3.4 THz with a frequency span of 0.78 THz. Compared with the THz image sensor reported in ISSCC 2021, which achieved 1024 pixel, 0.46–0.75 THz frequency bandwidth and 25 fps, this sensor realized a wider frequency band in high frequency regime and a higher resolution with much higher frame rate<sup>[6]</sup>.

Hard X-rays detector has been widely used in industrial and medical equipment. X-ray detector with the features of high-frame-rate and high-dynamic-range can be more adaptive to motion objects with lower radiation dose. Although SPAD detectors have been realized to obtain 3D images<sup>[4]</sup>, this year, a 400 × 200 resolution 600 fps 117.7 dB dynamic range SPAD X-ray detector with seamless global shutter and time-encoded extrapolation counter is proposed to obtain high-quality X-ray images<sup>[7]</sup>. In this sensor, the number of control signals is minimized and the counter cells recycle when they overflow, which achieves 18-bit outputs only using 10bit hardware.

Table 1 compares the different types of image sensors in ISSCC 2023. In summary, although advanced wafer-stacked back-illuminated process has been adopted in hybrid event-based vision sensors to improve the resolution and maximum event rate, the resolution of event-detection mode, which is much lower than that of the intensity-acquisition mode, still needs to be improved. For the THz/X-ray image sensors, the resolution may be further improved by advanced wafer-stacked back-illuminated process in the future.

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Table 1.	Performance	comparison	of different	types image sensor.
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Ref.	[1]	[2]	[3]	[5]	[7]
Sensor type	CIS + EVS	CIS + EVS	CIS + EVS	THz CIS	X-ray SPAD
Technology	40 nm BSI CIS + 65 nm CMOS + 3DMIM + 40 nm CMOS	90 nm Bl CIS + 22 nm CMOS	90 nm BI CIS + 22 nm CMOS	180 nm CMOS	65 nm CMOS
Resolution (pixel)	1032 × 928(EVS)/ 4096 × 3680(CIS)	2.08M(EVS)/ 35.6M(CIS)	640 × 640	128 × 128	400 × 200
Pixel pitch ( <i>µ</i> m)	8.8(EVS)/2.2(CIS)	4.88(EVS)/1.22(CIS)	2.97	60	49.5
Frame rate (fps)	18(CIS)	59(CIS)	60(CIS)	130	600
Dynamic range (dB)	-	67.8	72.2	73	117.7
Random noise (e-)	2.2	1.57	2.6	-	-
Maximum event rate (Eps)	4.6G	4.56G	1.41G	_	_

brid event-based vision sensor with  $4.88\mu$ m-pitch event pixels and up to 10K event frame rate by adaptive control on event sparsity. IEEE International Solid-State Circuits Conference, 2023, 92

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