ARTICLES

Journal of Semiconductors
(2023) 44, 124101
doi: 10.1088/1674-4926/44/12/124101

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Multiple SiGe/Si layers epitaxy and SiGe selective etching for vertically stacked DRAM

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Abstract: Fifteen periods of Si/$Si_{0.7}Ge_{0.3}$ multilayers (MLs) with various SiGe thicknesses are grown on a 200 mm Si substrate using reduced pressure chemical vapor deposition (RPCVD). Several methods were utilized to characterize and analyze the ML structures. The high resolution transmission electron microscopy (HRTEM) results show that the ML structure with 20 nm $Si_{0.7}Ge_{0.3}$ features the best crystal quality and no defects are observed. Stacked $Si_{0.7}Ge_{0.3}$ ML structures etched by three different methods were carried out and compared, and the results show that they have different selectivities and morphologies. In this work, the fabrication process influences on Si/SiGe MLs are studied and there are no significant effects on the Si layers, which are the channels in lateral gate all around field effect transistor (L-GAAFET) devices. For vertically-stacked dynamic random access memory (VS-DRAM), it is necessary to consider the dislocation caused by strain accumulation and stress release after the number of stacked layers exceeds the critical thickness. These results pave the way for the manufacture of high-performance multivertical-stacked Si nanowires, nanosheet L-GAAFETs, and DRAM devices.

Key words: RPCVD; epitaxy; SiGe/Si multilayers; L-GAAFETs; VS-DRAM

Citation: Z Z Kong, H X Lin, H L Wang, Y P Song, J J Li, X M Liu, A Y Du, Y H Miao, Y W Zhang, Y H Ren, C Li, J H Yu, J B Liu, J X Liu, Q Z Zhang, J F Gao, H H Li, X S Wang, J F Li, H H Radamson, C Zhao, T C Ye, and G L Wang, Multiple SiGe/Si layers epitaxy and SiGe selective etching for vertically stacked DRAM[J]. *J. Semicond.*, 2023, 44(12), 124101. https://doi.org/10.1088/1674-4926/44/12/124101

1. Introduction

With the development of 5G and artificial intelligence, the demand for high-speed, massive data transmission, and big data storage capacity is increasing[1, 2]. The shrinking device size has entered deep nanoscale nodes. From 22 to 7 nm nodes, FinFETs face increasing problems, such as the short channel effect (SCE) and patterning challenges[3–7]. Stacked gate-all-around (GAA) channels with nanowires (NWs)[8–10] or nanosheets (NSs)[11] are promising structures to meet the roadmap requirements for electrostatic control, density, and performance[12, 13]. A GAAFET structure allows for the design of channel width to satisfy current diversification for devices on a single wafer with a low area cost. In addition, the evolution of horizontal $4F^2$ 3D DRAM based on silicon-based nanowire gate-all-around transistors is an important research approach for future DRAM technology. Transistors and capacitors are stacked in the vertical direction, so multilayer Si/SiGe epitaxy and ultrahigh selective ratio release technology are the key technologies to realize the development of these structures. A VS (vertically stacked) CAT (cell array transistor) is a prospective candidate that has the potential to improve the performance and power efficiency of electronic devices[14]. In 2023, a 3D stackable 1T1C DRAM structure based on vertically stacked SiGe/Si heterojunctions was reported at IMW[15] and VLSI[16]. Fig. 1 shows the three most critical process steps in vertically-stacked 3D-DRAM: (a) Si/SiGe epitaxy; (b) SiGe full release; and (c) high-*k* and top electrode deposition. The memory array structure is similar to a 90-degree rotated $4F^2$ DRAM. Retention time is a critical factor in the operation of DRAM, and the quality of the stacked Si multilayer channels is crucial in ensuring that transistors function effectively. The number of stacked Si/SiGe multilayers can be tuned by epitaxy film cycles, and more channels can increase the storage density and electrostatic performance[17–19]. Achieving multilayer film epitaxy with high crystal quality is essential in ensuring the reliability and functionality of the device. Additionally, removing the SiGe sacrificial layer without damaging the Si channel is a complex process that requires precise control and optimization[20, 21]. Due to the lattice mismatch between Si and Ge, when the SiGe thickness exceeds the critical thickness, dislocations will occur and

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Received 7 JULY 2023; Revised 5 AUGUST 2023.
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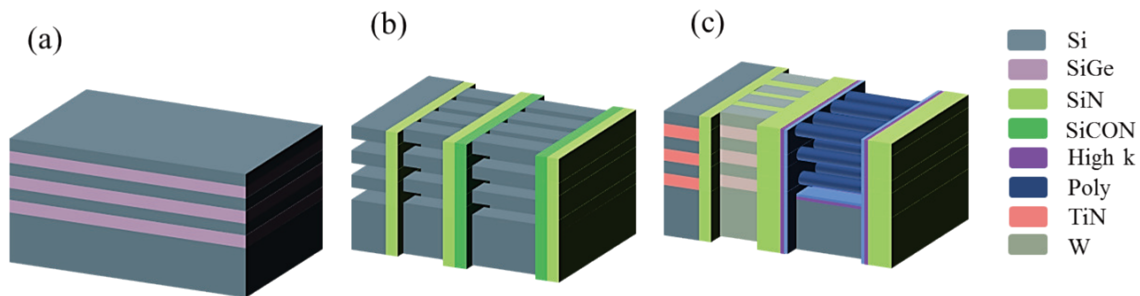


Fig. 1. (Color online) (a) Si/SiGe epitaxy; (b) SiGe full release; (c) high-*k* and top electrode deposition.

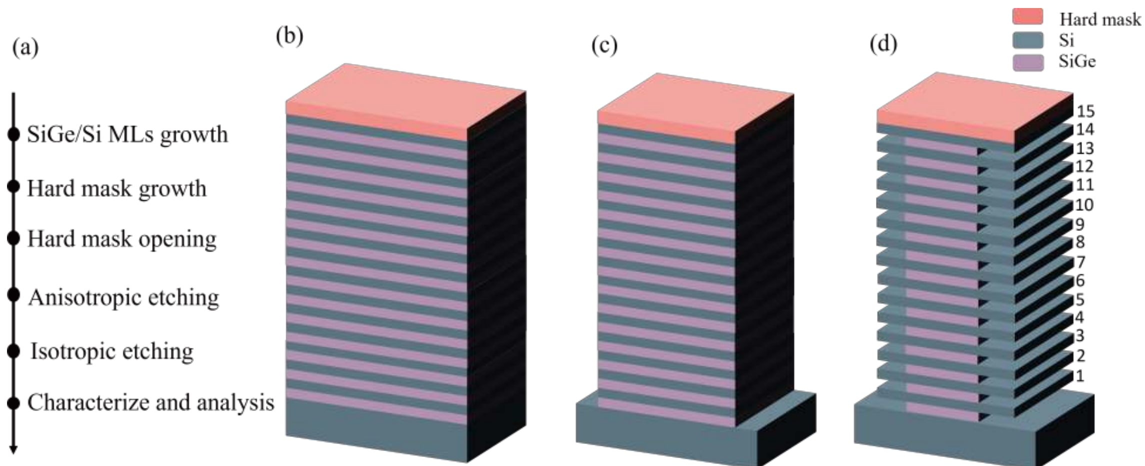


Fig. 2. (Color online) (a) Process flow. Schematic diagram of (b) hard mask growth, (c) anisotropic vertical etching of SiGe/Si MLs, and (d) isotropic selective lateral etching of SiGe.

propagate along the growth direction, which will reduce the Si channel quality[22–24]. Currently, Si channels are typically etched using selective corrosion of SiGe with various etching agents and methods, such as vapor HCl[25], plasma techniques[26–29], and wet methods[25, 30, 31]. However, if the selection ratio and etching accuracy are inadequate, then this can lead to changes in channel thickness, which may cause variations in V_{th} and I_{on} over a wafer[32, 33].

In this work, we investigated the two core process steps of vertically-stacked 3D DRAM: (a) Si/SiGe epitaxy; (b) SiGe full release. Fifteen cycles of SiGe/Si ML structures with different SiGe thicknesses and high crystal quality were grown by reduced pressure chemical vapor deposition (RPCVD). Then, three different lateral etching methods were used to etch the SiGe sacrificial layers, and these methods were compared by various methods. Finally, the film qualities during the different process stages were analyzed by HRTEM, SEM and HRXRD. After epitaxy, vertical high aspect ratio etching and lateral SiGe elective etching were analyzed to evaluate whether the Si channels were damaged. The results in this study may provide guidance for the L-GAAFET process, especially for multichannel devices.

2. Experimental details

The experiment in this work was carried out on an 8-inch Si wafer, as schematically illustrated in Fig. 2. The SiGe/Si multilayers were grown on Si (100) wafers in an RPCVD reactor at 650 °C. *In situ* prebaking was performed at 1050 °C for two mins to remove native oxide. Dichlorosilane (SiH_2Cl_2) and germane (GeH_4) (10% in H_2) were applied as Si and Ge precursors for the epitaxy of the Si/SiGe stacking film, respectively. Then, a SiO_2 film was deposited as a hard mask for the etching process. I-line lithography was utilized for patterning, and the hard mask was opened by CF_4/HBr/O_2 gases. Vertical anisotropic etching of SiGe/Si MLs is performed using HBr/O_2 as mentioned in reference[20] using ICP (Lam TCP 9400). Subsequently, SiGe layers were isotropically etched with three different methods: dry etching, continuous wet etching, and atomic layer etching (ALE). During the dry and continuous wet etching process, the films were etched by CF_4/O_2/He plasma, and by HF and HNO_3 mix solution for different times, which started at 5 s, increased by 5 s/step, and ended at 25 s. In the ALE process, the films were etched in cycles of etching and oxidation. In all the experiments, three groups were set up. In group A, the film consists of 15 pairs of SiGe/Si multilayer structures with 20 nm $Si_{0.7}Ge_{0.3}$ and 20 nm Si. In groups B and C, the thicknesses of the SiGe layers are changed to 40 and 60 nm, respectively. The cross-section images of the high resolution transmission electron microscope (HRTEM) were applied to analyze the crystal quality of the films. Secondary ion mass spectrometry (SIMS) was used for elemental composition and content analysis. The strain relaxation and defects of multilayers and the SiGe/Si interface were characterized by high-resolution X-ray diffraction (HRXRD) and reciprocal space mapping (RSM) by a Bruker JVDX configured with an analyzer crystal between the sample and detector.

3. Results and discussion

3.1. Epitaxy and profile of SiGe/Si multilayers

TEM and SIMS were used to characterize the thickness and Ge concentration of SiGe/Si MLs. As shown in Figs. 3(a)–3(e), SiGe layers and Si layers were grown periodically on Si substrates with constant thickness and content (Ge ~ 30%).

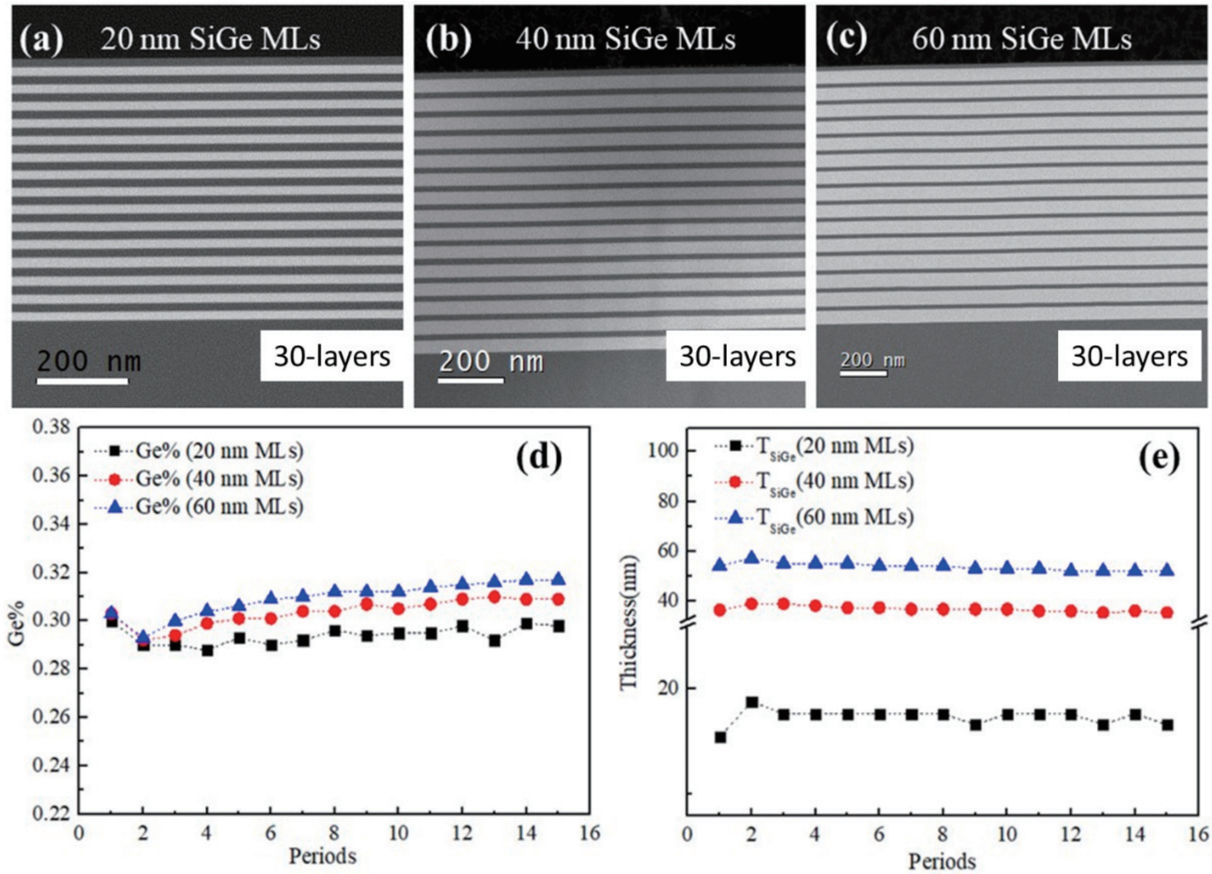


Fig. 3. (Color online) TEM images of ML structures with SiGe layers of (a) 20 nm, (b) 40 nm and (c) 60 nm. SIMS profile of (d) Ge concentration and (e) the thickness of SiGe layers in three 15-period Si/SiGe ML structures.

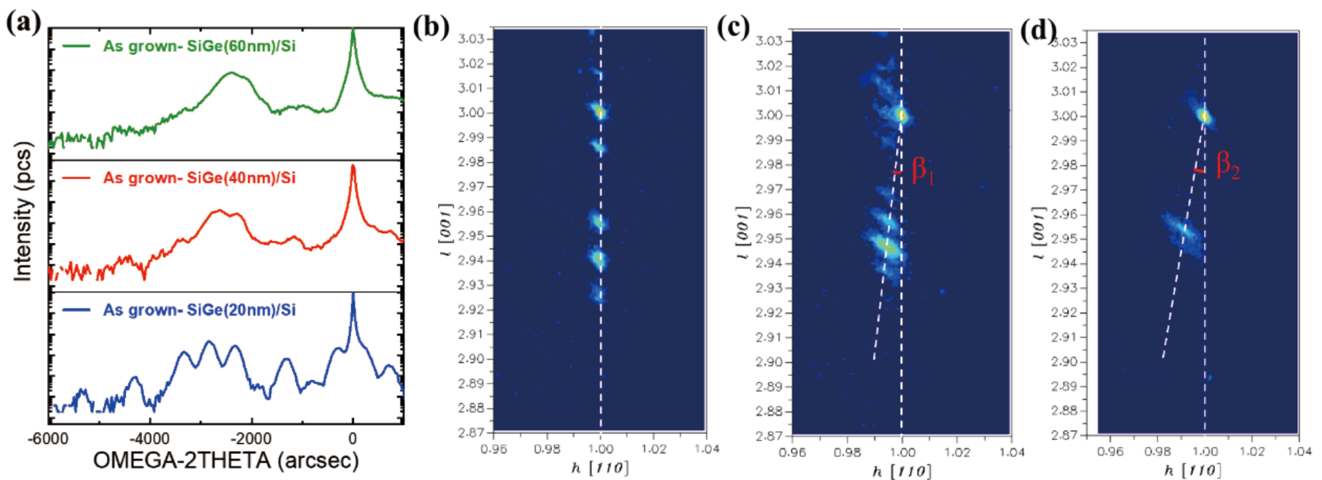


Fig. 4. (a) Rocking curves (RCs) of ML structures with different SiGe layer thicknesses. RSM images of ML structures with (b) 20 nm SiGe layers, (c) 40 nm SiGe layers and (d) 60 nm SiGe layers. $\beta_1 \approx 6.7°$, $\beta_2 \approx 10°$.

The thickness of the Si layers is kept at 20 nm in all groups, and the thicknesses of the SiGe layers in groups A, B, and C are 20, 40, and 60 nm, respectively, which is consistent with the experimental settings. Moreover, as shown in Figs. 3(d) and 3(e), there are subtle differences in the composition and thickness of the first layer and other layers. This is related to changes in the substrate surface temperature. When multiple periods of superlattice Si/SiGe are grown, the substrate temperature decreases in the first two periods, resulting in a decrease in the growth rate and an increase in the Ge concentration[34–36].

The stacking films with different SiGe thicknesses have different strains and defect states. To further investigate the effect of SiGe layer thickness on the quality of Si layers in ML structures, all three group samples were characterized by HRXRD[37]. Fig. 4(a) shows the rocking curves of three ML structures. We can see a sharp peak in the Si substrate and multiple higher-order satellite peaks due to superlattice periodicity, which are mainly to the left-hand side of the Si substrate peak. In these curves, the positions of the SiGe peaks have a right shift, and the fringes have decreased, indicating that the strain in the SiGe layers partially relaxes and that defects

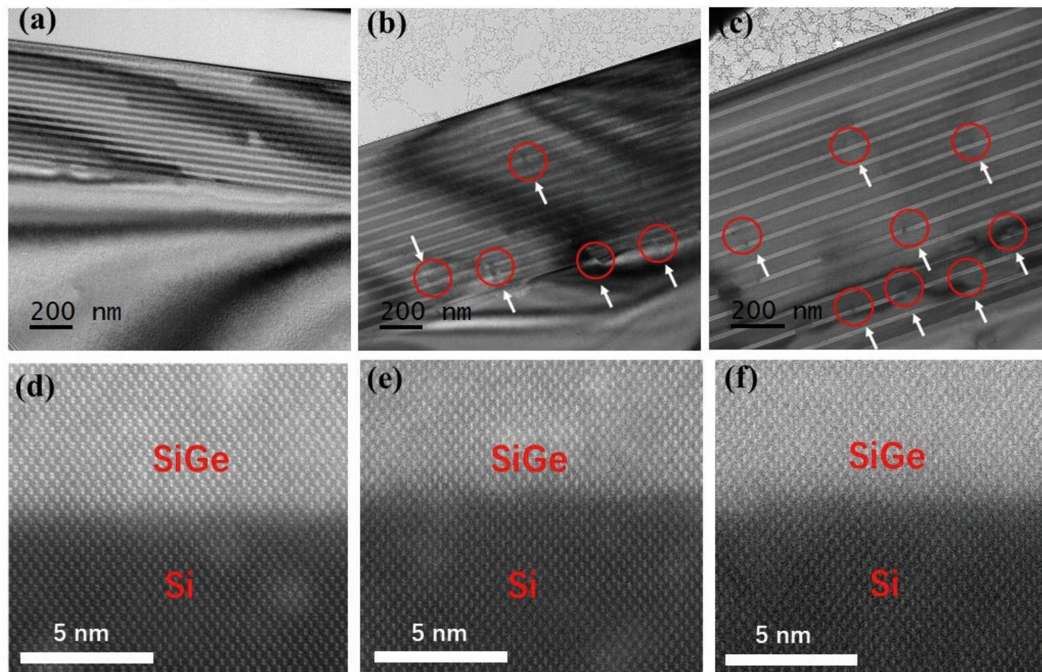


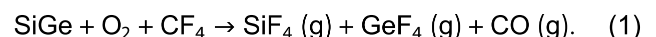
Fig. 5. (Color online) TEM images of ML structures with (a) 20 nm SiGe layers, (b) 40 nm SiGe layers and (c) 60 nm SiGe layers. HRTEM cross-sectional images of ML structures with (d) 20 nm SiGe layers, (e) 40 nm SiGe layers and (f) 60 nm SiGe layers.

appear as the thickness of SiGe increases from 20 to 60 nm. The 20 nm SiGe MLs showed well-defined multilayer fringe peaks with Kiessig stripes, indicating a high degree of crystal order and low interface roughness. For 40-nm SiGe MLs and 60-nm SiGe MLs, the Kiessig stripes begin to fade away, indicating that the material begins to relax. Correspondingly, RSM images around the (113) facet are obtained for the samples. The symmetrical RSM scan is used to determine whether the sample is tilted. To determine whether our sample is strained or relaxed, an asymmetric (113) facet scan is needed. The fully strained film layer makes its planar lattice exactly correspond to the planar lattice of the substrate, as shown in Fig. 4(b). SiGe peaks align with the Si peaks at h [110] = 1 in the SiGe (20 nm)/Si ML structure (Fig. 4(b)), whereas the SiGe peaks shift away from the Si peaks (h = 1) in the SiGe (40 nm)/Si ML structure (Fig. 4(c)) and SiGe (60 nm)/Si ML structure (Fig. 4(d)). This proves that the material begins to relax gradually. This is consistent with the HRXRD results. The peaks of SiGe (40 nm) and (60 nm) are broadened due to dislocations. These results indicate that the thinner SiGe layers have better film quality, so the quality of Si layers grown on 20 nm SiGe is the best among the three ML structures[34, 35].

TEM was used to intuitively investigate the SiGe layer thickness and the film quality. As shown in Figs. 5(a)–5(c), with increasing thickness of SiGe, the defect density in the ML structures increases from zero to more, which is consistent with the HRXRD results. In addition, HRTEM was used to characterize the Si/SiGe interfaces in the three ML structures. It can be seen from Figs. 5(d) and 5(f) that the Si/SiGe interface changes from sharp to blurred as the thickness of the SiGe layers increases from 20 to 60 nm. This also reveals that thick SiGe layers are not conducive to the high-quality growth of Si/SiGe MLs. Finally, the surface roughness of the three ML structures was characterized by AFM. The arithmetic mean deviation of the profile (Rq) increases from 0.39 to 1.40 nm when the thickness of the SiGe layers increases from 20 to 60 nm, and Rq increases more slowly from 40 to 60 nm (Figs. S1(a)–S1(c)). The characterization results indicate that the crystal quality of the 15-period $Si_{0.7}Ge_{0.3}$/Si MLs seriously degrades when the $Si_{0.7}Ge_{0.3}$ thickness is approximately 40 nm, which suggests that the L-GAAFET device should design and balance the thickness of the sacrificial layer, etch selectivity between the SiGe and Si channels and film quality.

3.2. Different sacrificial layer etching processes

We studied the SiGe layer etching methods reported in the literature and summarize them in Table 1. Most of the reports in the literature are the experimental results of a single etching process, and the same sample is not used for comprehensive comparison. In this experiment, a $CF_4 : O_2$: He gas combination was used for selective isotropic SiGe etching. The specific plasma reaction formula is as follows:



$$SiGe + O_2 + CF_4 \rightarrow SiF_4\ (g) + GeF_4\ (g) + CO\ (g). \quad (1)$$

After the introduction of O_2, the surface of SiGe and Si NS will be oxidized. Meanwhile, CO, which is easily formed into a gaseous state due to the combination of C and O, will increase the release of F free radicals from CF_4 to a certain extent. Because Ge is a more active element than Si, the oxidation of Ge is also easier to etch by F-base gas, and SiO_2 is a relatively stable material with relatively stable chemical activity, requiring a certain amount of ionic energy under F-base gas etching, so SiGe is more likely than SiO_2 to undergo F gas etching. As an inert carrier gas, He gas can make the plasma distribution more uniform, reduce the microload effect in the etching process, and reduce the roughness of the etched interface.

The wet method mainly uses a mixture of H_2O_2, HNO_3, CH_3COOH, HF, etc., which is characterized by a high selectivity ratio. The corrosion of the SiGe layer by the mixed solu-

Table 1. Selective etches of SiGe to Si.

Method	Solution	Advantages	Problem
Thermal etching	HCl[38–40] ClF_3[41]	High selectivity	React in chemical vapor deposition (CVD) tool The etching accuracy is limited Different etch rates for different crystal orientations
Dry etching	$CF_4/N_2/O_2$[27] $CF_4/O_2/He$[20] $NF_3/O_2/N_2$[42]	Easy to use in large wafer size Isotropic Fast	The etching accuracy is limited
Continuous wet etching	$HF/HNO_3/CH_3COOH$[25] $HF/HNO_3/CH_3COOH/H_2O$[31]	Excellent selectivity High etch rate Uniform etch rate in MLs etching	Etch rate depends strongly on the Ge content Residues block the tunnel in MLs etching
	$HF/H_2O_2/CH_3COOH$[43–45] $HF/H_2O_2/CH_3COOH/H_2O$[46]	High etch rate Nanoscale etching of SiGe to Si	Not suitable for small size Long aging time
Wet ALE	H_2O_2/BOEs[47] HNO_3/BOEs[48]	Controllable etch rate Atomically smooth surfaces	Long circle time Multistep processes Surface tension and capillary effect

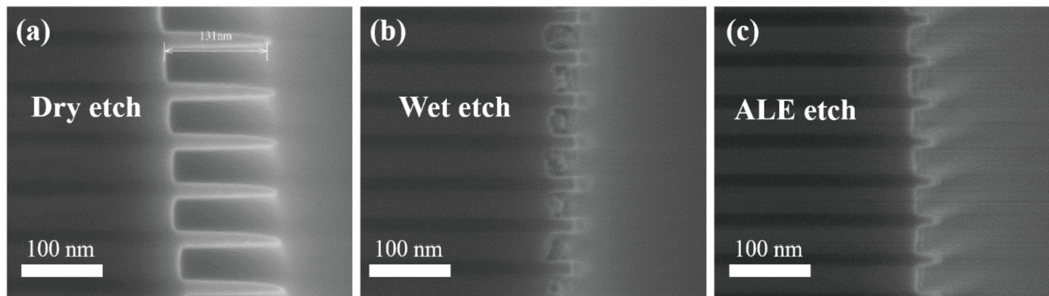


Fig. 6. SEM cross-sectional images of (a) 25 s dry etch, (b) 25 s continuous wet etch and (c) 40 cycles of ALE for the ML structure with 40 nm SiGe layers.

tion of HF, H_2O_2 and CH_3COOH mainly has two stages. Because Ge atoms in the SiGe layer are more active, the solution mainly reacts with Ge, and the oxidant in the solution oxidizes Ge in SiGe, which is relatively easily oxidized to form Ge oxides. The oxide of Ge then reacts with the acid to form a liquid soluble compound. In the SiGe layer, the Ge and Si atoms are roughly evenly arranged, and after the Ge atoms form a water-soluble substance, the Si atoms will fall off and enter the solution due to the lack of effective support. However, due to the characteristics of the solution reaction, there are some problems, such as the capillary effect and the "round" shape of the etched profile. This happens because the SiGe etch rate near the SiGe/Si interface is lower than that of the center because the Ge composition near the interface is lower than that of the center. This etch rate difference causes rounding on the sidewall of the SiGe layers. The Ge-containing layer before isotropic etching is one of the main causes of rounding formation after isotropic SiGe etching[28]. Crystalline orientation-dependent etching mechanisms also need to be considered.

In these works, different SiGe etch methods were investigated. Here, we selected three kinds of etching methods in the reported articles, dry etching, continuous wet etching, and ALE, to compare the lateral etching effects of different etching processes on the Si/SiGe ML structures. Fig. 6 shows SEM cross-sectional images of the SiGe (40 nm)/Si ML structure after lateral etching using three etching processes. (i) For dry etching, the etched cross section is neat, and the etching is highly selective and uniform from top to bottom in the ML structures (Fig. 6(a)). However, the tips of the silicon layers become sharp with time, which indicates damage to the silicon (Fig. S2). The "round" shape of the etched profile also needs to be optimized. (ii) For continuous wet etching, hydrofluoric acid (HF) and nitric acid (HNO_3) were used as etching solutions. It can be seen from Fig. 6(b) that the etched area is not clean due to some SiGe remaining in the etch tunnel. This is a common phenomenon in continuous wet etching, especially during the etching processes of small structures. In addition, the etching is uneven due to insufficient oxidation. (iii) For ALE, HNO_3 and buffered oxide etch (BOE) were utilized for oxidation and etching. As shown in Fig. 6(c), the ALE method produces a more complete etching and a clear interface, and there are no residues in the etch tunnel. Furthermore, the etch rate of dry etching is approximately 5–6 nm/s, and is independent of film thickness (Fig. S3). The etch rate of ALE is approximately 0.56 nm/cycle, which is much slower than that of dry etching. Overall, dry etching and ALE can achieve better profiles and accuracy than continuous wet etching, and drying etch has the fastest etch rate.

3.3. Quality of ML structures in different processing steps

The linearity and resolution of the delay line has a great effect on the transmitter's performance. To overcome the bottleneck of low linearity and low resolution, an improved delay line structure is proposed with a calibration algorithm to conquer PVT variations for this all-digital design. The measurement results show that the proposed structure with the calibration algorithm can evidently improve the linearity and resolution of the delay line.

HRXRD RCs can provide intuitive quality analysis, and RSM images can be used to analyze the strain state of the film without any damage. Fig. 7 shows the RCs and RSMs of the SiGe (20 nm)/Si ML structure at different steps of the pro-

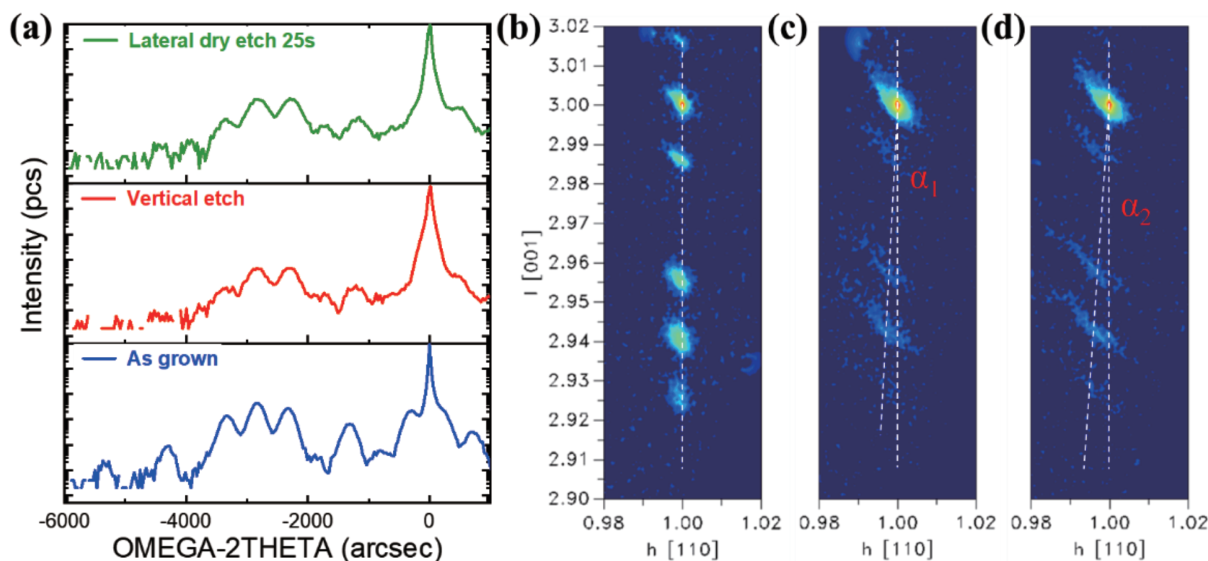


Fig. 7. (Color online) (a) Rocking curves of SiGe (20 nm)/Si ML structures at different steps of processing. RSMs in the vicinity of the asymmetric (113) Bragg reflection acquired on SiGe (20 nm)/Si ML structures: (b) as-grown, (c) after vertical anisotropy etching and (d) after lateral isotropic SiGe selectivity dry etching $\alpha_1 \approx 3°$, $\alpha_2 \approx 4°$.

cess. From the RCs curve (Fig. 7(a)), the satellite peaks of the interlayer interference can be seen clearly, meaning that the film still has a good quality and sharp interface during the three processes, which is indispensable for fabricating the L-GAAFET. The SiGe peaks are vertically aligned with the Si peak, which means that the SiGe epitaxy film is totally strained with the Si substrate (Fig. 7(b)). After vertical anisotropy etching and lateral isotropy etching, some fringes disappear and the SiGe signal decreases because SiGe is selectively etched away. Moreover, the SiGe peaks shift from the Si peaks in the h [100] = 1 direction, indicating strain relaxation in the SiGe films. The shift angles form $\alpha_1 \approx 3°$ and $\alpha_2 \approx 4°$, which means that the SiGe sacrificial layer is released and strain relaxation occurs in the residual SiGe layers. In RSMs, Si peaks appear as diffused scattering after vertical etching and lateral etching (Figs. 7(c) and 7(d)), which indicates that there are some defects occurring in Si layers. This may happen because during the process of changing from compressive strain to a free state, partial lattice deformation occurs, causing defects to increase in the epitaxial Si films.

4. Conclusion

In this study, 15 periods of SiGe/Si MLs are grown, etched, and characterized. First, the principle that there will be fewer defects in the film when the SiGe film is thinner still holds. In addition to comparing three different 15 periods of SiGe/Si MLs, we find that the ML crystal quality seriously degrades when the $Si_{0.7}Ge_{0.3}$ thickness is approximately 40 nm, which can provide an epitaxy reference for multistacking Si/SiGe films. Second, the same Si/SiGe MLs were isotropy etched by three different reported methods to compare the selectivity and rate, showing that all the etching methods have good selectivity and that the sample after dry etching and ALE still has good morphology. Third, we utilize RCs and RSM to characterize the different process effects on the MLs and find that the interface and quality are basically unaffected and that the strain is partially relaxed. In this study, a stable process for preparing 15 periods of vertically stacked Si layers from high-quality growth to high selectivity and uniform etching is realized, which is a precursor study for multi-stacking L-GAAFET and VS-CAT DRAM devices.

Acknowledgments

This work is supported in part by the Strategic Priority Research Program of the Chinese Academy of Sciences (Project ID. XDA0330300), in part by Innovation Program for Quantum Science and Technology (Project ID. 2021ZD0302301), and in part by the Youth Innovation Promotion Association of CAS (Project ID. 2020037). And Beijing Superstring Academy of Memory Technology has given strong technical and testing support.

Appendix A. Supplementary material

Supplementary materials to this article can be found online at https://doi.org/10.1088/1674-4926/44/12/124101.

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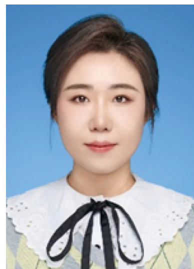

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