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Demonstration of a manufacturable SOT-MRAM multiplexer array towards industrial applications

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Abstract: We have successfully demonstrated a 1 Kb spin-orbit torque (SOT) magnetic random-access memory (MRAM) multiplexer (MUX) array with remarkable performance. The 1 Kb MUX array exhibits an in-die function yield of over 99.6%. Additionally, it provides a sufficient readout window, with a TMR/R_P_sigma% value of 21.4. Moreover, the SOT magnetic tunnel junctions (MTJs) in the array show write error rates as low as 10^{-6} without any ballooning effects or back-hopping behaviors, ensuring the write stability and reliability. This array achieves write operations in 20 ns and 1.2 V for an industrial-level temperature range from −40 to 125 °C. Overall, the demonstrated array shows competitive specifications compared to the state-of-the-art works. Our work paves the way for the industrial-scale production of SOT-MRAM, moving this technology beyond R&D and towards widespread adoption.

Key words: spin-orbit torque; MRAM; multiplexer array; 200 mm-wafer platform; stability; reliability

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1. Introduction

Magnetic random-access memory (MRAM), especially spin-transfer torque (STT) MRAM has already emerged into the consumer market. It is considered as a promising candidate for "edge" applications such as AI, IoT, and etc.[1–3]. Major semiconductor foundries like TSMC[4–6], GlobalFoundries[7–10], Samsung[11–13], one after another announced mass production of the embedded STT-MRAM, replacing embedded NOR flash (eFlash) below the 28 nm complementary metal oxide semiconductor (CMOS) technology node. The overall performances of the embedded STT-MRAM, including operation voltages, write/read speeds, endurance, feature sizes etc. surpass those of the eFlash[14]. Additionally, great efforts are being made in the MRAM industry to develop STT-MRAM as a working memory[15–17]. IBM, for instance, introduced a 14 nm FinFET-based STT-MRAM macro in 2020 for last level cache (LLC) applications[17]. Although the write speed can be reduced to 4 ns, the endurance of the STT-MRAM still falls short of meeting the requirements for the SRAM replacement in LLC application, where write speed must be under 2 ns and endurance should exceed 10^{17} cycles[18].

To overcome the challenges faced by the STT-MRAM, spin-orbit torque (SOT) MRAM has emerged as a promising alternative[19–24]. This is because SOT-MRAMs feature high endurance and fast switching speed, thanks to the separation of read/write current paths[25–29] and less incubation time during the write operations[30], distinguishing them from the STT-MRAM[31]. Researchers and industry players have made significant progress in realizing SOT-MRAM technology[32–43]. For instance, Beihang University first implemented the interplay of STT and SOT in the write operations, addressing the field-free issue for "type-Z" devices[32]. IMEC first demonstrated field-free perpendicular MTJs (referred to as "type-Z" device) in a 300 mm wafer, utilizing an additional magnetic hard mask layer[34]. Tohoku University showcased a 4 KB SOT-MRAM using canted in-plane MTJs[37]. TSMC, in collaboration with ITRI, also successfully delivered an 8 Kb SOT-MRAM array ("type-Y" devices)[38, 39]. However, it is important to note that the SOT-MRAM is still in the research and development (R&D) phase worldwide. This is because various challenges persist, such as integration process, switching efficiency, field-free switching, and more, requiring substantial efforts for resolutions[44, 45].

In our previous work, we successfully integration isolated SOT-MTJs in a 200 mm-wafer R&D platform, achieving uniform electrical and magnetic performance across the wafer[46]. In addition, high endurance of up to 10^{12} cycles was achieved for the fabricated isolated SOT-MTJs[28, 46]. Building upon this achievement, we further integrated the SOT-MTJs into an array in conjunction with CMOS in the 200 mm wafer. We finally succeed in demonstrating of the 1 Kb SOT-MRAM multiplexer (MUX) array, with competitive specifications over all the reported works. For the 1 Kb SOT-MRAM MUX array, several aspects should be considered simultaneously: (1) excellent fabrication process to ensure devices with good morphology and stable performance[47]; (2) tight distribution of high and low resistance within the array[39]; (3) a large TMR value

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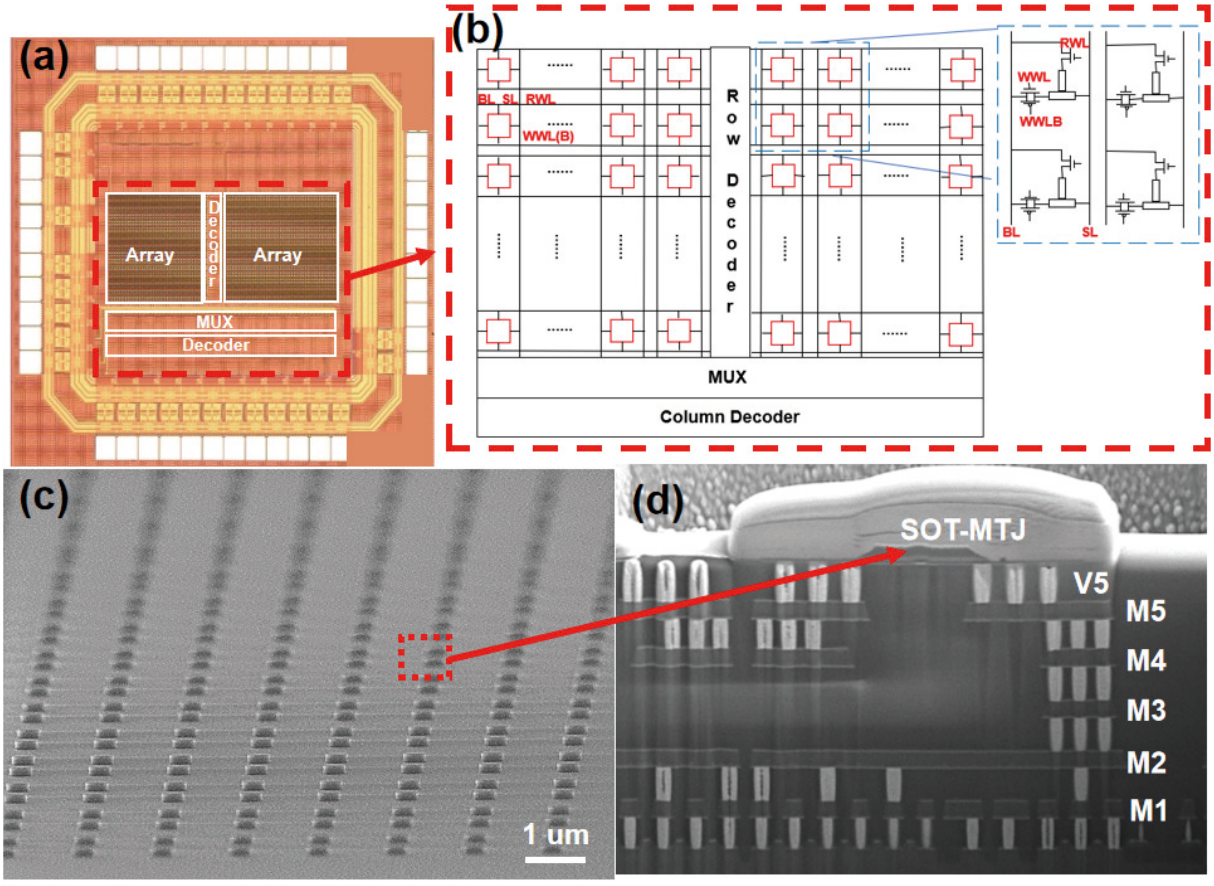

Fig. 1. (Color online) (a) A top view of 1 Kb SOT MRAM MUX array observed by an optical microscope. The size of the MUX array is about 1 × 1 mm^2. (b) The 1 Kb SOT-MRAM MUX array includes a row address decoder, a column address decoder, SOT arrays, and a MUX circuit. (c) A zoom-in SEM image of the MUX array after the MTJ etch process. Each pillar in the SEM image represents an elliptical shape MTJ with CD of 300, 1050 nm for short axis *a* and long axis *b*, respectively. (d) The cross-section TEM of a selected MTJ in the array from the fully processed wafer in conjunction with CMOS using common 0.18 μm CMOS process technology node. The SOT-MTJ is integrated between the "Metal 5" and the passivation layer.

to provide a sufficient reading window[8]; (4) industrial-grade operation temperature capability to meet the practical applications requirements[25, 41]. Thus, following the fabrication of the SOT-MRAM MUX array, we systematically characterized the electrical properties, with a particular focusing on the write operation capabilities under industry-grade temperatures.

2. Experiments

We will first briefly introduce the physical properties of the 1 Kb SOT-MRAM MUX array. The most critical SOT-MTJ stacks were deposited in a specialized PVD consisting of (from the bottom to the top) CMOS substrate/β-W (5)/CoFeB (1.3)/MgO (1.5)/CoFeB (1.9)/CoFe (0.8)/Ru (0.8)/CoFe (2.5)/IrMn (7.5)/Ta (3)/Ru (2)/Ta (2). The numbers in parentheses signify every layer thickness in nanometer. Each layer thickness nonuniformity (sigma%) is smaller than 2% across the wafer confirmed through the 49 points resistivity measurements. We keep monitoring the film thicknesses periodically to ensure 2% of wafer-to-wafer variations. Overall film stacks, especially for the MgO tunneling barrier/CoFeB interfaces, are well stacked with sharp interfaces confirmed by the TEM[46] thanks to the surface treatment by the chemical mechanical polishing process. Detailed information of the integration procedures and isolated device performance can be found in our-previous work[46]. Fig. 1(a) shows a top-view image of the 1 Kb MUX array taken from an optical microscope. The actual physical size of the MUX array in the picture does not exceed 1 × 1 mm^2. As shown in Fig. 1(b), the 1 Kb SOT-MRAM MUX array includes a row address decoder, a column address decoder, SOT-MTJ arrays, and a MUX circuit. Through the cooperation of the MUX circuit and the address decoders, SOT-MTJs of all addresses can be accessed and tested by external analog signals. Fig. 1(c) shows a magnified image of the MUX array after the MTJ etch process, which was captured using a scanning electron microscope (SEM). The MTJs in the SEM image are patterned into "type-Y" devices[48] having an elliptical shape. Although the "type-Y" SOT-MTJ devices have lower density and limited scalability compared to the "type-Z" devices, they do have some advantages[25], including: (1) the in-plane MTJ stacks for the "type-Y" devices are relatively easier to be deposited with sufficient pinning field as compared with those of the top-pinned perpendicular MTJ stacks for the "type-Z" devices; (2) "type-Y" devices show deterministic switching without the need for an additional bias field to break the symmetry, resulting in a less-complexity integration process. The designed critical dimensions (CD) of the MTJs in the MUX array are 300 nm for the short axis *a* and 1050 nm for the long axis *b*, with an aspect ratio (*b*/*a*) of 3.5. As can be seen from Fig. 1(c), the MTJs are well distributed-

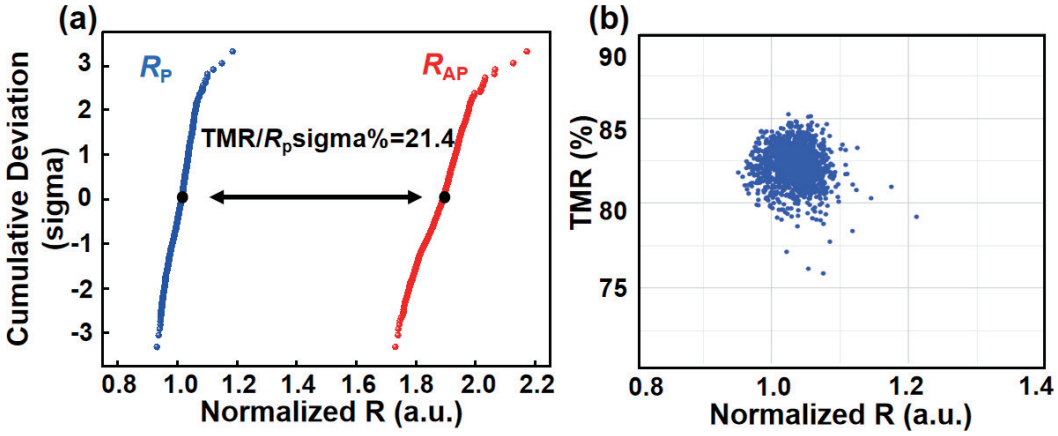

Fig. 2. (Color online) (a) The quantile plot of the R_P and R_{AP} distributions of the 1 Kb SOT-MRAM MUX array. The R_P and R_{AP} were measured after the SOT-MTJs were set to either the P or AP states under appropriate write bias voltages. The R_P and R_{AP} were normalized to the average value of the R_P in the 1 Kb MUX array. The arrows indicate the separation gap between the R_P and R_{AP} statistically. (b) The correlation between the TMR and the R_P. Each dot in the figure indicates one SOT-MTJ. The resistance in horizontal axis of (b) is normalized by the average value of the R_P.

with an excellent within-array CD sigma% (standard deviation/average value) around 1%. Fig. 1(d) shows a cross-section transmission electron microscope (TEM) image of a selected SOT-MTJ from the fully integrated 200 mm CMOS wafer. The front-end of line (FEOL) and back-end of line (BEOL) processes of the 200 mm CMOS wafer adopt a standard 180 nm CMOS technology node process from a common foundry. After completing the "Metal 5" and "Via 5", the wafer was transferred to a dedicated MRAM R&D process platform. The SOT-MTJs are integrated between the "Metal 5" and the passivation layer. The height of the SOT-MTJs (including the metal hard mask for the top electrode connection) totals approximately 100 nm. With such height, the SOT-MTJs can be potentially moved downward even to "Metal 1" in the near future, which is close to the transistors and enable faster write/read operation speeds.

Following the integration of the MUX array, the electrical properties of the 1 Kb SOT-MRAM MUX array were systematically investigated. An external bias voltage VDD of 3.3 V was applied to the chip to select each SOT-MTJ bit within the MUX array. Another tunable bias voltage was applied to drive the read/write operations of the selected SOT-MTJ. We initiated the study of the analog read tests to evaluate the magnetoresistances of the SOT-MTJs within the MUX array. The tunneling magnetoresistance (TMR) ratio is defined as $(R_{AP} - R_P)/R_P$, where R_{AP} and R_P are the tunneling resistances measured at 100 mV for both antiparallel (AP) and parallel (P) magnetization configurations between the top and bottom magnetic layers. Subsequently, we conducted statistical analysis to assess the write operation capabilities of the MUX array. This includes evaluating the write error rate (WER), and examining the write shmoo under various bias voltages and pulse widths. Furthermore, the temperature dependence of the analog read results and write capabilities were investigated over a wide temperature range from –40 to 125 °C.

3. Results and discussions

We will first introduce the analog read results obtained from the SOT-MRAM MUX array. The R_P and R_{AP} were measured after the SOT-MTJs were set to either the P or AP states under appropriate write bias voltages. Fig. 2(a) shows the quantile plot of the R_P and R_{AP} recorded for all the bits in the 1 Kb MUX array. The R_P and R_{AP} were normalized to the average value of the R_P in the 1 Kb MUX array. As illustrated in Fig. 2(a), the R_P values exhibit normal distributions with a tight R_P_sigma% of 3.9%, aligning well with the CD distributions as described above. Fig. 2(b) presents the correlation between the TMR and the R_P. No clear resistance open and/or short bits are found among the SOT-MTJs within the 1 Kb MUX array as indicated in Fig. 2(b). This finding confirms the well-controlled and robust process employed in our MRAM R&D platform. Additionally, the majority of the SOT-MTJs exhibit TMR values above 80%. Although this value is slightly lower than that of 100% film level TMR obtained by current in-plane tunneling technology (CIPT)[46], it can be attributed to potential extrinsic defects at the magnetic layer/MgO interfaces or the sidewall damage of the MTJs caused by the subsequent process. However, it is worth noting that the ratio of TMR/R_P_sigma% is 21.4. This implies that the R_P and R_{AP} are well separated with a wide gap of 21.4 R_P_sigma. Despite the 1 Kb MUX array exhibiting relatively lower TMR ratios of around 80%, such a wide gap will ensure enough read margin even if we use a middle-point sense amplifier circuit design[49]. Nevertheless, by optimizing the MTJ film stacks and integration processes in the future, it is possible to further enhance the TMR ratios to approximately 200%[45].

Next, we characterized the WER for the SOT-MTJs in the MUX array. Fig. 3(a) shows typical WER curves as a function of bias voltages for a write pulse width of 100 ns, where positive bias voltage corresponds to the write AP direction and negative bias voltage corresponds to the write P direction. Each data point in Fig. 3(a) represents the write failure rate for a selected device tested over 1 million cycles under a constant bias voltage. Every cycle consists of a sequence of reset-read-write-read operations. The bias voltages were normalized to the median switching voltage of 1.25 V at WER = 10^{-4}. As observed in Fig. 3(a), the WER curves exhibit a smooth and sharp decrease, successfully achieving relatively symmetrical WER level of 10^{-6} for both the write P and AP directions. In addition, the bias voltages at WER = 10^{-6} are only about 10% higher than those at WER = 10^{-4}. Due to the test time limitations, we only collected WER curves down to 10^{-4} level for over 70 devices from the MUX array, as displayed in Fig. 3(b). Similar to Fig. 3(a), all WER curves show reliable switching

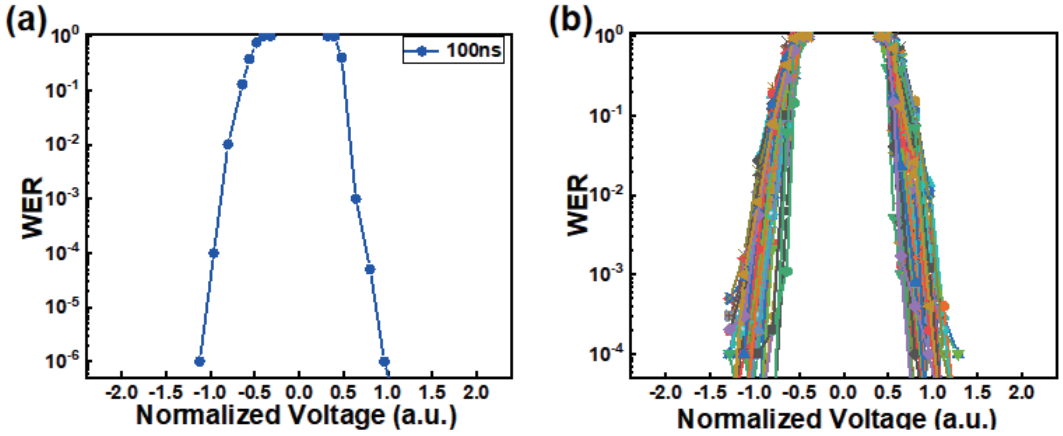

Fig. 3. (Color online) (a) Typical WER curves down to 10^{-6} level measured under 100 ns write pulse widths; (b) WER curves down to 10^{-4} level were collected from over 70 SOT-MTJs under 100 ns write pulse widths. The positive and negative bias voltages in (a) and (b) correspond to the write AP and P directions respectively. Each point in (a) and (b) represents the write failure rate for devices tested over 1 million cycles under each constant bias voltage.

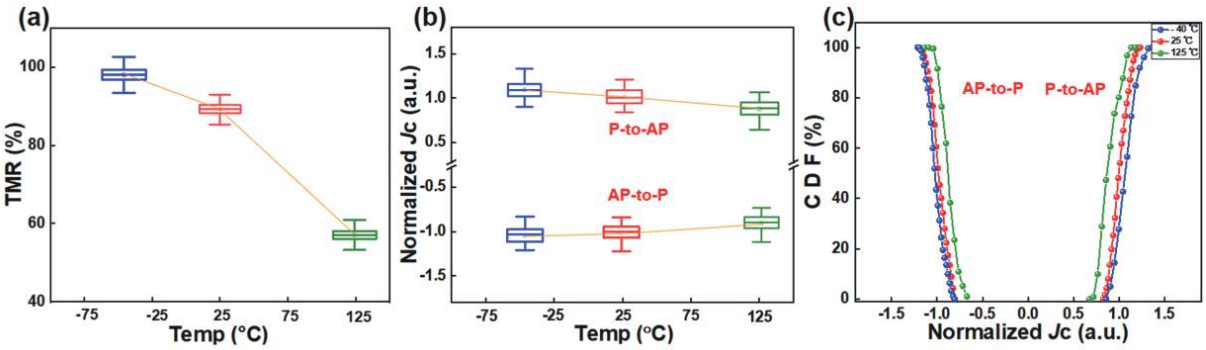

Fig. 4. (Color online) The temperature dependence of (a) the TMR ratios and (b) switching critical switching densities. (c) The CDF plot of the critical current densities from the data in (b). Blue, red and green box plots/dots represent the values at –40, 25, and 125 °C, respectively. The current densities in (b) and (c) are normalized to the median value of 19 MA/cm^2 at 25 °C.

down to 10^{-4} level at a write pulse width of 100 ns. Most importantly, we do not observe ballooning effects[50] or back-hopping behaviors[50, 51] in the obtained WER curves for both write directions across all the measured devices. This suggests that the SOT-MTJs feature robust and reliable switching behaviors when tested under a 100 ns pulse width. Moreover, the sigma of the bias voltage at WER = 10^{-4} is 0.16 V with sigma% of 12.8% for the bias voltage distribution. This distribution is reasonably favorable for a small density array, such as Kb-level array. However, it would be relatively large for a larger Mb-level array. This arises from the fact that, in order to have sub-parts-per-million (ppm) level bit error rate (BER) for a Mb array, an operation voltage $V_{OP} = V_{median} + 5\ V_{\_sigma}$ is necessary to be applied. Here V_{OP} is the operation voltage, V_{median} and $V_{\_sigma}$ are the median voltage and the sigma of the voltage at sub-ppm-level WER, respectively. If the $V_{\_sigma}$ is large, the value of the V_{OP} would be large and exceed the operation margin, even if the V_{median} are the same. There are several factors that would contribute to these relatively large distributions. First, we observe that the sigma% of the bias voltages are much larger than those of the CD and magnetic free layer thickness of the SOT-MTJs within the MUX array. This suggests that the CD and magnetic free layer thickness are not the main root causes. Then, it is likely that these distributions could be attributed to (1) the extrinsic defects inside of the magnetic free layer, and/or (2) non-uniform spin current generated from the SOT heavy metal layer or injected into the ferromagnetic layer due to the imperfect quality of the interfaces between the heavy metal and magnetic free layer. To address these issues, further engineering of the integration process is necessary, including optimizing the quality of the SOT material and the magnetic free layer, and implementing damage-free MTJ etching techniques in the future studies.

Then, we checked the temperature dependence of the aforementioned electrical parameters of the MUX array across an industry-grade temperature range from −40 to 125 °C. We measured the R_{AP} and R_P distributions of the array devices at different temperatures and calculated the TMR. Fig. 4(a) illustrates the TMR ratios as a function of the temperature. The median values of the TMR ratios decrease from 96% at –40 °C to 59% at 125 °C, which shows a consistent trend with previous works[49, 52]. Although the TMR drops by nearly half, it would remain sufficient for automotive applications when employing differential-reference or self-reference sense amplifier circuit designs. However, it is still necessary to achieve as high TMR ratios over 100% as possible at high temperatures such as 160 °C to meet low read errors and fast read speed[53, 54] and to reduce the overhead of circuit design. The TMR ratios could be improved through careful

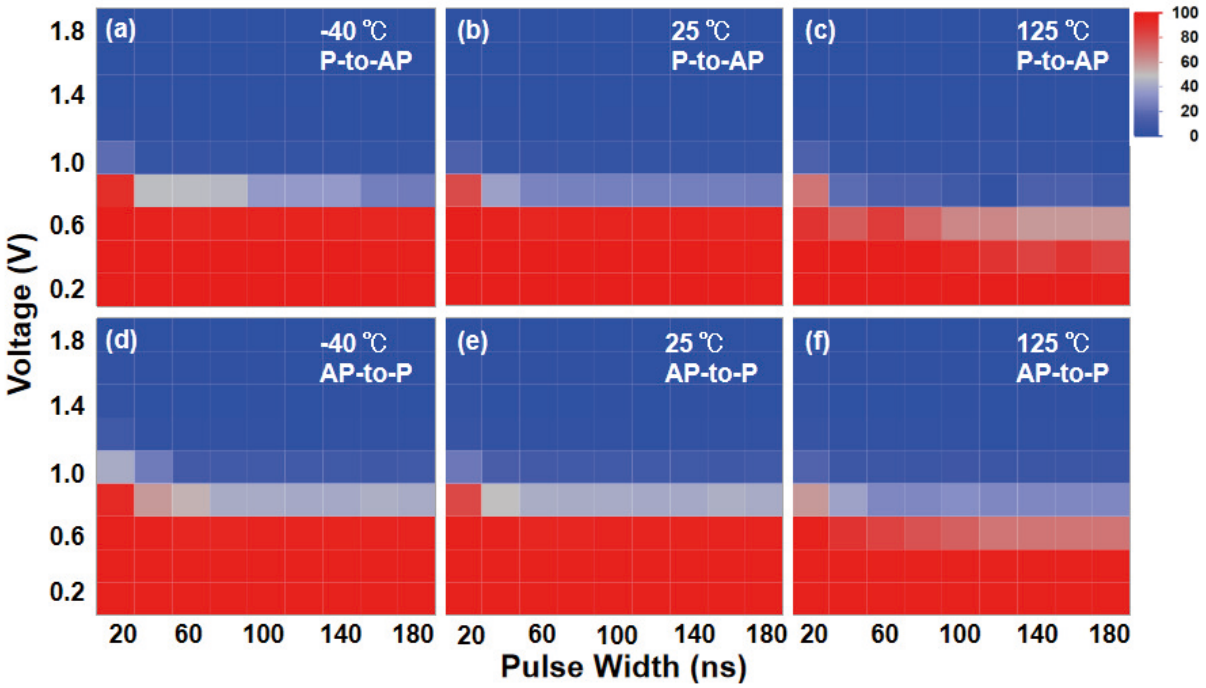

Fig. 5. (Color online) Write shmoo plots of the 1 Kb MUX array at different temperatures from −40, 25, and 125 °C, respectively. (a)–(c) are for the P-to-AP direction, and (d)–(f) are for the AP-to-P direction. The shmoo plots show the write failure rates of 1 Kb in the MUX array at each write speed (*x*-axis) and each write bias voltage (*y*-axis). The pulse widths vary from 20 to 200 ns and the bias voltages range from 0.2 to 1.8 V, respectively. The write failure rates are presented in color gradient with the scale bar shown on the right: red represents 100% fail and blue represents zero fail.

design of the film stack and optimization of the PVD deposition conditions, such as gas, power, chamber configurations, etc.

Figs. 4(b) and 4(c) summarize the critical switching current densities of the MUX array as a function of the temperature from different perspectives. The critical current densities are defined as the values at the 50% switching probabilities for AP-to-P and P-to-AP directions, obtained from *R*–*V* measurements under 100 ns pulse width for all the SOT-MTJs in the MUX array. The values in both Figs. 4(b) and 4(c) are normalized to the median critical current density J_C = 19 MA/cm^2 at 25 °C. As illustrated in Fig. 4(b), the current densities slightly increase by 5% at −40 °C as compared to that at 25 °C. Fig. 4(c) presents the cumulative distribution function (CDF) of the critical switching current densities calculated from the data in Fig. 4(b). The current densities at each temperature follow normal distributions and are tightly distributed with sigma% values of 9.1%, 9.0%, and 10.8% for −40, 25, and 125 °C, respectively. The sigma% values are similar between −40 and 25 °C and are lower than that of the 125 °C. This suggests that the magnetic properties at −40 and 25 °C are similar, resulting in only minor changes of switching current density. However, at 125 °C, the thermally induced fluctuations contributed to an overall reduction in the switching current density while enlarging the sigma% value.

Based on the above results, we then examined the write capability of the MUX array through the write shmoo tests. Figs. 5(a)–5(c) are the write shmoo plots at different temperatures for the P-to-AP direction, while Figs. 5(d)–5(f) are the corresponding ones for the AP-to-P direction. These shmoo plots show the write failure rates of 1 Kb in the MUX array at various write speeds (*x*-axis) and write bias voltages (*y*-axis). The pulse widths range from 20 to 200 ns and the bias voltages vary from 0.2 to 1.8 V. The write failure rates are presented using a color gradient, with the scale bar shown on the right: red indicates a 100% fail rate, while blue represents zero fail. From Figs. 5(b) and 5(e), it is evident that the write failure rates tested at 25 °C exhibit a distinct horizontal boundary between the red and the blue regions around write bias voltage of approximate 1 V. This suggests that the write failure rates are primarily influenced by the write bias voltages rather than the pulse widths within the measured range of 20 up to 200 ns. If the pulse widths were to be below 20 ns or in the sub-ns range, it is likely that the pulse width would play a more dominant role in the switching behaviors. However, due to the tester limitations used in this work, the write pulse width cannot be further reduced below 20 ns. Nevertheless, the MUX array demonstrates successful write operations without failures across a wide pulse width range down to 20 ns, coupled with appropriate bias voltages. Furthermore, the failure rates (red color) tend to slightly increase with decreasing the pulse width under the same bias voltage. The behaviors of write shmoo plots for −40 °C (Figs. 5(a) and 5(d)) and 125 °C (Figs. 5(c) and 5(f)) are basically the same as those of 25 °C, suggesting an excellent write capability for the MUX array across a broad temperature range.

Finally, we compare the 1 Kb MUX array with other published ones. Please note that there are very limited array-level data available for the SOT-MRAM worldwide so far[37–39]. As summarized in Table 1, despite the larger CDs of the SOT-MTJs in our work due to process limitations compared to other work, we still achieved a high yield of 99.6% for the 1 Kb SOT-MRAM MUX array, with TMR ratios exceeding 80%, WER reaching a level of 10^{-6}, which proves the good manufacturing process.

Table 1. Performance comparison of SOT-MRAM.

Items	This work	Ref. [34]	Ref. [35]	Ref. [38]	Ref. [39]	Ref. [40]	Ref. [41]	Ref. [42]
SOT channel	β-W	W	β-W	W	W	Pt	Pt	β-W
Device type	IMA	PMA	IMA	IMA	IMA	PMA	IMA	PMA
MTJ CD (nm)	300 × 1050	60	88 × 315	240 × 840	75 × 230	50	700	60
TMR (%)	>80	110	167	85	140	90/125	101	105
WER	$<10^{-6}$	10^{-5}	N/A	N/A	10^{-4}	N/A	N/A	N/A
Jc (MA/cm^2)	28 @20 ns	126 @1 ns	23.6 @0.35 ns	81	61 @1 ns	110 @1 ns	170 @10 ns	57 @1 ns
Function yield	99.6%	N/A	N/A	N/A	98%	N/A	N/A	N/A

4. Conclusion

We demonstrated a 1 Kb SOT-MRAM MUX array with competitive performance compared with others as shown in Table 1. Moreover, we also showed sufficient write operation window without failures at a write pulse width of 20 ns or greater and above 1.2 V bias voltages, covering a wide temperature range from −40 to 125 °C. Following this first demonstration, we will focus on scaling down the MTJs' CD and SOT channel lengths/widths to compete with other works[32–40]. Based on the CD dependence of the switching current density observed in our study[46], we would anticipate achieving sub-100 μA write current by reducing the MTJ CD to around 100 nm. We will also evaluate the array-level reliability, particularly the endurance performance. The SOT-MTJ CD/aspect ratio, SOT channel size and temperature dependence of the endurance will be systematically studied, which is not the scope of this paper and will be published elsewhere. This advancement would make SOT-MRAM highly promising as a replacement for slow SRAM in last-level cache applications.

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References

[1] Clarke P. TSMC embedded MRAM is key to Gyrfalcon AI chip. Technology News, 2018, [2018-9-22]. https://www.eenews-europe.com/

[2] Choe J. TSMC 22ULL eMRAM Die removed from Ambiq Apollo-4, Another Disruptive Technology on Embedded Memory. TechInsights TechStream Blog_Emerging Memory, 2021 [2021-8-13]. https://www.techinsights.com/

[3] Choe J. Recent technology insights on STT-MRAM: Structure, materials, and process integration. 2023 IEEE International Memory Workshop (IMW), Monterey, 2023, 1

[4] Chiang H L, Wang J F, Chen T C, et al. Cold MRAM as a density booster for embedded NVM in advanced technology. 2021 Symposium on VLSI Technology, 2021, 1

[5] Chen C H, Chang C Y, Weng C H, et al. Reliability and magnetic immunity of reflow-capable embedded STT-MRAM in 16nm FinFET CMOS process. 2021 Symposium on VLSI Technology, 2021, 1

[6] Wang C Y, Shih M C, Weng C H, et al. Reliability demonstration of reflow qualified 22nm STT-MRAM for embedded memory applications. 2020 IEEE Symposium on VLSI Technology, 2020, 1

[7] Lee K, Yamane K, Noh S, et al. 22-nm FD-SOI embedded MRAM with full solder reflow compatibility and enhanced magnetic immunity. 2018 IEEE Symposium on VLSI Technology, 2018, 183

[8] Naik V B, Lee K, Yamane K, et al. Manufacturable 22nm FD-SOI embedded MRAM technology for industrial-grade MCU and IOT applications. 2019 IEEE International Electron Devices Meeting (IEDM), 2019, 2.3.1

[9] Naik V B, Yamane K, Kwon J, et al. STT-MRAM: A robust embedded non-volatile memory with superior reliability and immunity to external magnetic field and RF sources. Proceedings of 2021 IEEE Symposium on VLSI Technology, 2021, 1

[10] Naik V B, Yamane K, Lee T Y, et al. JEDEC-qualified highly reliable 22nm FD-SOI embedded MRAM for low-power industrial-grade, and extended performance towards automotive-grade-1 applications. 2020 IEEE International Electron Devices Meeting (IEDM), 2021, 11.3.1

[11] Lee K, Bak J H, Kim Y J, et al. 1Gbit high density embedded STT-MRAM in 28nm FDSOI technology. 2019 IEEE International Electron Devices Meeting (IEDM), 2019, 2.2.1

[12] Lee K, Kim D S, Bak J H, et al. 28nm CIS-compatible embedded STT-MRAM for frame buffer memory. 2021 IEEE International Electron Devices Meeting (IEDM), 2021, 2.1.1

[13] Suh K, Lee J H, Shin H M, et al. 12.5 Mb/mm^2 embedded MRAM for high density non-volatile RAM applications. 2021 Symposium on VLSI Technology, 2021, 1

[14] Endoh T, Honjo H, Nishioka K, et al. Recent progresses in STT-MRAM and SOT-MRAM for next generation MRAM. 2020 IEEE Symposium on VLSI Technology, 2020, 1

[15] Rao S, Kim W, van Beek S, et al. STT-MRAM array performance improvement through optimization of Ion beam etch and MTJ for last-level cache application. 2021 IEEE International Memory Workshop (IMW), 2021, 1

[16] Wu H, Katragadda V, Evarts E, et al. First experimental demonstration of MRAM data scrubbing: 80 Mb MRAM with 40 nm junctions for last level cache applications. 2021 IEEE International Electron Devices Meeting (IEDM), 2021, 2.3.1

[17] Edelstein D, Rizzolo M, Sil D, et al. A 14 nm embedded STT-MRAM CMOS technology. 2020 IEEE International Electron Devices Meeting (IEDM), 2020, 11.5.1

[18] Worledge D C. Spin-transfer-torque MRAM: The next revolution in memory. 2022 IEEE International Memory Workshop (IMW), 2022, 1

[19] Mihai Miron I, Gaudin G, Auffret S, et al. Current-driven spin torque induced by the Rashba effect in a ferromagnetic metal layer. Nat Mater, 2010, 9, 230

[20] Miron I M, Garello K, Gaudin G, et al. Perpendicular switching of a single ferromagnetic layer induced by in-plane current injection. Nature, 2011, 476, 189

[21] Cubukcu M, Boulle O, Drouard M, et al. Spin-orbit torque magnetization switching of a three-terminal perpendicular magnetic tunnel junction. Appl Phys Lett, 2014, 104, 042406

[22] Liu L Q, Lee O J, Gudmundsen T J, et al. Current-induced switching of perpendicularly magnetized magnetic layers using spin torque from the spin Hall effect. Phys Rev Lett, 2012, 109, 096602

[23] Liu L Q, Pai C F, Li Y, et al. Spin-torque switching with the giant spin Hall effect of tantalum. Science, 2012, 336, 555

[24] Pai C F, Liu L Q, Li Y, et al. Spin transfer torque devices utilizing

the giant spin Hall effect of tungsten. Appl Phys Lett, 2012, 101, 122404
[25] Shao Q M, Li P, Liu L Q, et al. Roadmap of spin–orbit torques. IEEE Trans Magn, 2021, 57, 1
[26] Guo Z X, Yin J L, Bai Y, et al. Spintronics for energy- efficient computing: An overview and outlook. Proc IEEE, 2021, 109, 1398
[27] Van Beek S, Cai K M, Fan K Q, et al. MTJ degradation in multi-pillar SOT-MRAM with selective writing. 2023 IEEE International Reliability Physics Symposium (IRPS), 2023, 1
[28] Xu X Y, Zhang H C, Jiang C P, et al. Full reliability characterization of three-terminal SOT-MTJ devices and corresponding arrays. 2023 IEEE International Reliability Physics Symposium (IRPS), 2023, 1
[29] Sverdlov V, Makarov A, Selberherr S. Two-pulse sub-ns switching scheme for advanced spin-orbit torque MRAM. Solid State Electron, 2019, 155, 49
[30] Lee K S, Lee S W, Min B C, et al. Threshold current for switching of a perpendicular magnetic layer induced by spin Hall effect. Appl Phys Lett, 2013, 102, 112410
[31] Liu H, Bedau D, Sun J Z, et al. Dynamics of spin torque switching in all-perpendicular spin valve nanopillars. J Magn Magn Mater, 2014, 358, 233
[32] Wang M X, Cai W L, Zhu D Q, et al. Field-free switching of a perpendicular magnetic tunnel junction through the interplay of spin-orbit and spin-transfer torques. Nat Electron, 2018, 1, 582
[33] Garello K, Yasin F, Couet S, et al. SOT-MRAM 300MM integration for low power and ultrafast embedded memories. 2018 IEEE Symposium on VLSI Circuits, 2018, 81
[34] Garello K, Yasin F, Hody H, et al. Manufacturable 300mm platform solution for field-free switching SOT-MRAM. 2019 Symposium on VLSI Circuits, 2019, T194
[35] Honjo H, Nguyen T V A, Watanabe T, et al. First demonstration of field-free SOT-MRAM with 0.35 ns write speed and 70 thermal stability under 400°C thermal tolerance by canted SOT structure and its advanced patterning/SOT channel technology. 2019 IEEE International Electron Devices Meeting (IEDM), 2020, 28.5.1
[36] Wu Y C, Kim W, Garello K, et al. Deterministic and field-free voltage-controlled MRAM for high performance and low power applications. 2020 IEEE Symposium on VLSI Technology, 2020, 1
[37] Natsui M, Tamakoshi A, Honjo H, et al. Dual-port SOT-MRAM achieving 90-MHz read and 60-MHz write operations under field-assistance-free condition. IEEE J Solid-State Circuits, 2021, 56, 1116
[38] Chen G L, Wang I J, Yeh P S, et al. An 8kb spin-orbit-torque magnetic random-access memory. 2021 International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA), 2021, 1
[39] Song M Y, Lee C M, Yang S Y, et al. High speed (1ns) and low voltage (1.5V) demonstration of 8Kb SOT-MRAM array. 2022 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits), 2022, 377
[40] Couet S, Rao S, Van Beek S, et al. BEOL compatible high retention perpendicular SOT-MRAM device for SRAM replacement and machine learning. 2021 Symposium on VLSI Technology, 2021, 1
[41] Zhu D Q, Guo Z X, Du A, et al. First demonstration of three terminal MRAM devices with immunity to magnetic fields and 10 ns field free switching by electrical manipulation of exchange bias. 2021 IEEE International Electron Devices Meeting (IEDM), 2022, 17.5.1
[42] Cai K, Talmelli G, Fan K, et al. First demonstration of field-free perpendicular SOT-MRAM for ultrafast and high-density embedded memories. 2022 International Electron Devices Meeting (IEDM), 2023, 36.2.1
[43] Rahaman S Z, Chang Y J, Hsin Y C, et al. Development of highly manufacturable, reliable, and energy-efficient spin-orbit torque magnetic random access memory (SOT-MRAM). 2022 International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA), 2022, 1
[44] Krizakova V, Perumkunnil M, Couet S, et al. Spin-orbit torque switching of magnetic tunnel junctions for memory applications. J Magn Magn Mater, 2022, 562, 169692
[45] Lin S J, Huang Y L, Song M, et al. Challenges toward low-power SOT-MRAM. 2021 IEEE International Reliability Physics Symposium (IRPS), 2021, 1
[46] Zhang H C, Ma X Y, Jiang C P, et al. Integration of high-performance spin-orbit torque MRAM devices by 200-mm-wafer manufacturing platform. J Semicond, 2022, 43, 102501
[47] Park J H, Lee J, Jeong J, et al. A novel integration of STT-MRAM for on-chip hybrid memory by utilizing non-volatility modulation. 2019 IEEE International Electron Devices Meeting (IEDM), 2020, 2.5.1
[48] Fukami S, Anekawa T, Zhang C, et al. A spin-orbit torque switching scheme with collinear magnetic easy axis and current configuration. Nat Nanotechnol, 2016, 11, 621
[49] Lee K, Chao R, Yamane K, et al. 22-nm FD-SOI embedded MRAM technology for low-power automotive-grade-I MCU applications. 2018 IEEE International Electron Devices Meeting (IEDM), 2019, 27.1.1
[50] Min T, Chen Q, Beach R, et al. A study of write margin of spin torque transfer magnetic random access memory technology. IEEE Trans Magn, 2010, 46, 2322
[51] Kim W, Couet S, Swerts J, et al. Experimental observation of back-hopping with reference layer flipping by high-voltage pulse in perpendicular magnetic tunnel junctions. IEEE Trans Magn, 2016, 52, 1
[52] Tan J, Lim J H, Sikder B, et al. Impact of voltage polarity on time-dependent dielectric breakdown of 1-nm MgO-based STT-MRAM with self-heating correction. IEEE Trans Electron Devices, 2022, 70, 76
[53] Zhao W S, Chappert C, Javerliac V, et al. High speed, high stability and low power sensing amplifier for MTJ/CMOS hybrid logic circuits. IEEE Trans Magn, 2009, 45, 3784
[54] Song Y J, Lee J H, Shin H C, et al. Highly functional and reliable 8Mb STT-MRAM embedded in 28nm logic. 2016 IEEE International Electron Devices Meeting (IEDM), 2017, 27.2.1

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