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Incomplete charge transfer in CMOS image sensor caused by Si/SiO_2 interface states in the TG channel

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Abstract: CMOS image sensors produced by the existing CMOS manufacturing process usually have difficulty achieving complete charge transfer owing to the introduction of potential barriers or Si/SiO_2 interface state traps in the charge transfer path, which reduces the charge transfer efficiency and image quality. Until now, scholars have only considered mechanisms that limit charge transfer from the perspectives of potential barriers and spill back effect under high illumination condition. However, the existing models have thus far ignored the charge transfer limitation due to Si/SiO_2 interface state traps in the transfer gate channel, particularly under low illumination. Therefore, this paper proposes, for the first time, an analytical model for quantifying the incomplete charge transfer caused by Si/SiO_2 interface state traps in the transfer gate channel under low illumination. This model can predict the variation rules of the number of untransferred charges and charge transfer efficiency when the trap energy level follows Gaussian distribution, exponential distribution and measured distribution. The model was verified with technology computer-aided design simulations, and the results showed that the simulation results exhibit the consistency with the proposed model.

Key words: CMOS image sensor; charge transfer; interface state traps

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1. Introduction

CMOS image sensors (CISs) with pinned photodiodes (PPDs) are widely used in various imaging fields due to their low power consumption, high integration, and high quantum efficiency[1–5]. Charge transfer efficiency (CTE) is a key performance parameter of PPD CISs[6]. Only when the photogenerated charges collected in the PPD are fully transferred through the transfer gate (TG) to the floating diffusion (FD) node can CIS read the complete signal value and achieve a high-quality imaging[7, 8]. However, existing CMOS manufacturing processes usually introduce non-idealities such as potential barriers and interface state traps into the transfer path, making it difficult for CISs to achieve complete charge transfer[9]. Therefore, research in related fields is increasingly focused on exploring the mechanism of incomplete charge transfer.

Thus far, this research can be divided into two main categories based on the factors that cause incomplete charge transfer. The first factor is the presence of potential barriers on the transfer path, which is generated by complicated doping profiles under the TG[6, 10–15]. In Ref. [6], Serena Rizzolo in France investigated the influence of pixel design on image lag by focusing on two different aspects which impact the charge transfer. In Ref. [10], Raffaele Capoccia in Switzerland proposed a physics-based compact model of the pinned photodiode combined with the transfer gate. In Ref. [11], Cui Yang in Xidian University proposed and investigated a novel CMOS image sensor pinned photodiode pixel, named as O-T pixel. In Ref. [12], Xiuyu Wang in Tianjin Univeristy proposed an analytical model for quantifying the charge transfer potential barrier in pinned photodiode CMOS image sensors. In Ref. [13], Uzma Khan in India reported the full well capacity and the pinned photodiode capacitance of four-transistor pixels in a CMOS image sensor to be dependent on the potential barrier offered by transfer gate. In Ref. [14], Lu Liu in National University of Defense Technology proposed an analytical model of the potential barrier for the pinned photodiode combined with the transfer gate. In Ref. [15], Congzhen Hu in Xi'an Jiao Tong University proposed physical-based model to characterize the whole charge behavior characteristics of the pinned photodiode when employing the thermal diffusion, self-induced drifting, and thermionic emission mechanisms together. The second factor leading to incomplete charge transfer is the spill back effect under high illumination. The physical mechanism underlying this effect was investigated in Ref. [16].

Silicon devices inevitably suffer from interface state traps[17]. In 2007, Boyd Fowler proposed a conjecture: There are two reasons for image lag, one is the potential barrier on the transfer path, and the other is the trap in the TG channel[18]. In 2012, Bonjour *et al.* accurately distinguished the incomplete charge transfer caused by potential barriers

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and traps in the TG channel, which confirmed the influence of interface state traps on charge transfer[19]. Specifically, under low illumination, the number of photogenerated electrons collected in the PPD decreases[20], and the proportion of electrons that cannot be transferred to the FD node in the total number of photogenerated electrons will increase. This leads to more obvious degradation of the imaging quality of CISs under low illumination[9].

However, Bonjour *et al*. only confirmed the effect of interface state traps in the TG channel on charge transfer, they did not provide any analytical model for CISs to quantify the incomplete charge transfer caused by interface state traps in the TG channel. The mechanism of incomplete charge transfer caused by interface state traps is still unclear. Without a quantitative model as a guide, the experimental findings remain limited to the specific experimental conditions. Therefore, it is particularly necessary to establish an accurate physical model for the incomplete charge transfer caused by interface state traps in the TG channel.

This paper proposes a physical model for quantifying the incomplete charge transfer caused by interface state traps in the TG channel. First, the value of the boundary trap energy level is determined by calculating emission time constants of different trap energy levels based on Shockley-Read-Hall (SRH) theory and comparing them with the time of the TG to the off state. Then, according to the small injection theory, the quasi-Fermi level is approximated to the Fermi level, and the relationship between the probability of electrons occupying the trap energy level and the Fermi level is established based on the Fermi-Dirac statistical distribution. Next, an explicit two-dimensional expression for the number of untransferred charges associated with the trap state density and trap energy level distribution is established, and the variation rules of the number of untransferred charges and charge transfer efficiency are given when the trap energy levels follow different distributions, particularly under low illumination. Finally, the proposed model is verified using technology computer-aided design (TCAD) simulations.

2. Mathematical model

A typical four-transistor pixel structure, including PPD, TG, and FD node, is shown in Fig. 1. After the optical integration phase in PPD is completed, the TG is switched on, and the photogenerated electrons are transferred from the PPD to the FD node through the TG. CTE is defined as the percentage of electrons in a pixel that can be successfully transferred to the FD node with respect to the total number of electrons collected in the PPD within a transfer cycle:

$$\mathrm{CTE} = \frac{N_{\mathrm{transfer}}}{N_{\mathrm{e0}}} \times 100\%, \tag{1}$$

where N_{transfer} is the number of electrons successfully transferred to the FD node, and N_{e0} is the total number of electrons collected in the PPD.

2.1. Determination of boundary trap energy level E_{t0}

To further explore the restriction mechanism of interface state traps on charge transfer, the core step is to explain the behavior of interface state traps in the TG channel during charge transfer, to capture and release carriers. Figs. 2(a)–2(e) depict the change in the TG voltage (V_{TG}) with time during

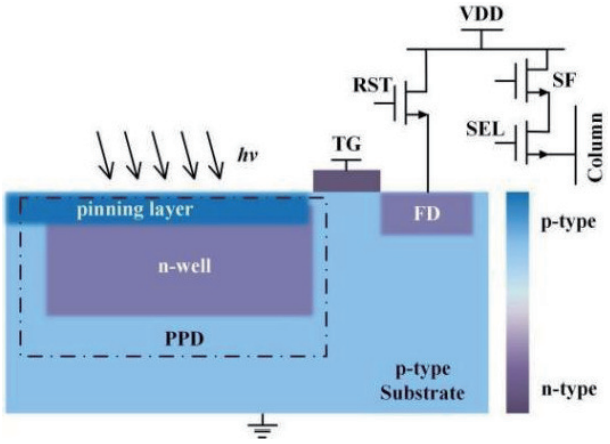

Fig. 1. (Color online) Four-transistor pixel structure of the PPD CIS.

the charge transfer, the band bending of semiconductors under the TG during charge transfer, as well as the filling of trap energy levels by electrons. In Fig. 2(a), the process by which V_{TG} increases from $V_{\mathrm{TG\text{-}Low}}$ to $V_{\mathrm{TG\text{-}High}}$ is defined as phase Ⅰ, the process by which it keep $V_{\mathrm{TG\text{-}High}}$ is defined as phase Ⅱ, and the process by which it decreases from $V_{\mathrm{TG\text{-}High}}$ to $V_{\mathrm{TG\text{-}Low}}$ at t_2 is defined as phase Ⅲ. The time required for V_{TG} to drop from $V_{\mathrm{TG\text{-}High}}$ to $V_{\mathrm{TG\text{-}Low}}$ is defined as t_{fall}. Before the pixel enters stage Ⅰ, V_{TG} is maintained at $V_{\mathrm{TG\text{-}Low}}$. The semiconductor under the TG is in equilibrium, and the surface energy band bending is shown in Fig. 2(b). When TG is turned on, the change of V_{TG} breaks the equilibrium state of the semiconductor under the TG, and the pixel enters stage Ⅰ. The filling behavior of charges on trap energy levels is shown in Fig. 2(c). Due to the rise of V_{TG}, the position of quasi-Fermi level of the electron changes from $E_{\mathrm{F\text{-}t0}}$ to $E_{\mathrm{F\text{-}t1}}$, the position of the trap energy level relative to the quasi-Fermi level decreases, the trap energy level below the quasi-Fermi level will be rapidly filled with electrons, and finally the energy band bending of the semiconductor will reach the state shown in Fig. 2(d). In stage Ⅱ, V_{TG} remains at $V_{\mathrm{TG\text{-}High}}$. Since the number of photogenerated electrons collected under low illumination is generally dozens to hundreds[20], which is much less than the concentration of most carriers (electrons) in the TG channel, the behavior of photogenerated electrons entering the TG channel can be regarded as a low level injection, and the quasi-Fermi energy level of electrons in stage Ⅱ can be approximated to the Fermi energy level of equilibrium state[21]. After completing the charge transfer, TG turns off, corresponding to stage Ⅲ. Similar to Stage Ⅰ, the change in V_{TG} breaks again the equilibrium state of the semiconductor. The position of quasi-Fermi level of the electron changes from $E_{\mathrm{F\text{-}t2}}$ to $E_{\mathrm{F\text{-}t3}}$, and the electrons captured by interface states during stage Ⅰ tend to be re-emitted into the conduction band, as shown in Fig. 2(e). This phenomenon is determined by the emission time constant of electrons. The emission time constant of electrons is the average time for the electrons emitted to conduction band from interface states and expressed as τ_{c}. The average time for the electrons captured by interface states from conduction band is capture time constant of electrons and represented as τ_{e}. The SRH theory[22] provides expressions for τ_{c} and τ_{e}:

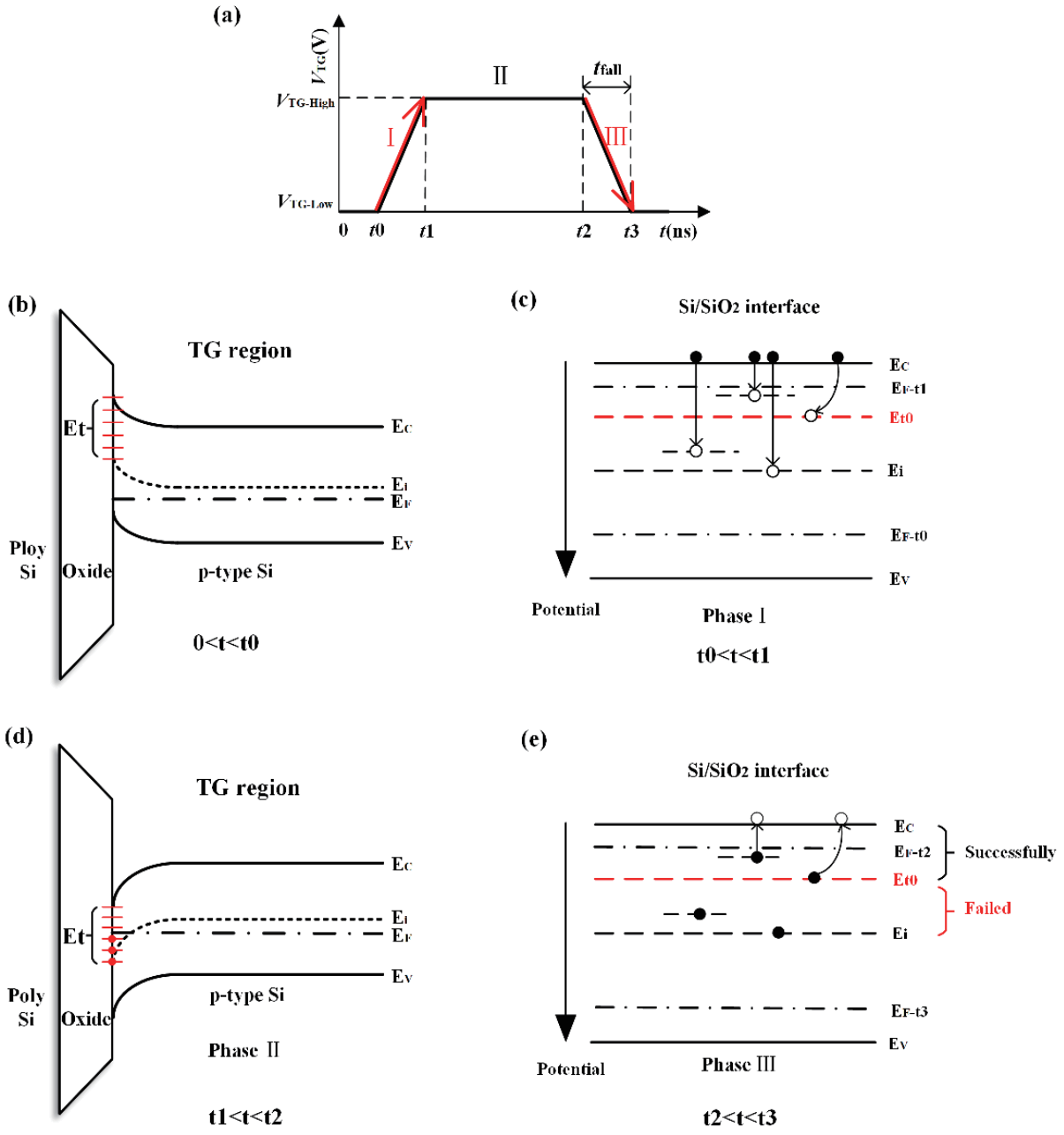

Fig. 2. (Color online) V_{TG} time sequence diagram, semiconductor energy band diagram, and charge trapping effect during charge transfer. (a) Time sequence diagram of V_{TG} during charge transfer. (b) Energy band diagram of the semiconductor in the TG region at V_{TG-Low}. (c) Process of electron capture by interface states in phase Ⅰ. (d) Energy band diagram of the semiconductor in the TG region at $V_{TG-High}$. (e) Process of electron emission by interface states in phase Ⅲ.

$$\tau_c = \frac{1}{n\sigma_n v_t}, \tag{2}$$

$$\tau_e = \frac{1}{\sigma_n N_C v_t}\exp\left(\frac{E_C - E_t}{KT}\right), \tag{3}$$

where n is the electron density of Si semiconductor, N_C is the effective state density of the conduction band, v_t is the thermal velocity, σ_n is the electron capture cross-section, E_C is the conduction band, E_t is the trap energy level, K is the Boltzmann constant, and T is the temperature. The specific values of these parameters are given in Table 1.

Eq. (3) indicates that the emission time constant of the trap energy level is related to the position of the trap energy level in the band gap. An energy level far from the conduction band, also known as the deep level trap, has a large emission time constant. Therefore, the electrons trapped by the deep level traps cannot be emitted into the conduction band during TG closure, as shown in Fig. 2(e).

During charge transfer, the semiconductor under the TG will generate an electron inversion layer to form the conductive channel. When the threshold inversion point is reached, the electron concentration in the channel is equal to the hole concentration of the p-substrate in Table 1, the capture time constant can be calculated by using this concentration according to Eq. (2), and the value is 100 ns. When electrons begin to transfer from the PPD to the TG channel, the electron concentration in the TG channel will increase compared to the electron concentration at the threshold inversion point, and

Table 1. Parameters of the mathematical model.

Parameters	Description	Value
N_A	Doping concentration of the p-type substrate	10^{15} cm^{-3}
N_D	Doping concentration of the n-well	10^{17} cm^{-3}
N_A^+	Doping concentration of the top pinning layer	10^{20} cm^{-3}
N_C	Effective state density of conduction band	2.8×10^{19} cm^{-3}
v_t	Thermal velocity	10^7 cm/s
q	Unit charge	1.6×10^{-19} C
K	Boltzmann constant	1.38×10^{-23} J/K
T	Temperature	300 K
L_{TG}	Length of the TG	0.7 μm
L_{PPD}	Length of the pinned photodiode	2 μm
A_{TG}	Area of the TG	0.7 μm^2
t_{fall}	Time required for the TG to drop from $V_{TG\text{-}High}$ to $V_{TG\text{-}Low}$	1 ns
N_{max}	The coefficient of Gaussian and exponential distribution	5×10^{10} cm^{-2}·eV^{-1}
n	Electron density of Si semiconductor	10^{15} cm^{-3}
σ_n	Electron capture cross-section	10^{-15} cm^{-2}

the capture time constant will be shorter than 100 ns. Therefore, the time for V_{TG} to rise from $V_{TG\text{-}Low}$ to $V_{TG\text{-}High}$ is set to 100 ns, that is, the time for stage Ⅰ is 100 ns. In this way, it can be assumed that interface states can complete the capture of charges during stage Ⅰ. Thus, the number of charges lost during charge transfer is the number of electrons captured when the TG is turned on but unreleased when the TG is turned off. To obtain the number of untransferred charges, it is necessary to determine the value of the boundary trap energy level E_{t0}. The emission time constant of the boundary trap energy level is set to be equal to t_{fall}, as expressed in Eq. (4). And by substituting Eq. (4) into Eq. (3), we obtain the value of E_{t0}.

$$\tau_{e0} = t_{fall}, \tag{4}$$

$$E_{t0} = E_C - KT\ln\left(t_{fall}\sigma_n N_C V_t\right). \tag{5}$$

2.2. Model for quantifying incomplete charge transfer caused by different trap energy level distribution

After the TG is turned off, the number of charges stored in interface states, with a continuous distribution from the band gap center E_i to the boundary trap energy level E_{t0}, is the number of charges lost during the transfer. The charge density of interface states is given by the Fermi–Dirac distribution, as expressed in Eq. (6):

$$n_{Trapped} = \int_{E_i}^{E_{t0}} N_t\left(1-\frac{1}{1+\frac{1}{g}\exp\left(\frac{E_F-E_t}{KT}\right)}\right)\mathrm{d}E_t, \tag{6}$$

where N_t is the trap state density, g is the degeneracy of the ground state, and E_F is the Fermi level. The area of the TG is multiplied by the density in Eq. (6) to obtain the number of untransferred charges:

$$N_{Trapped}(E_t, N_t) = A_{TG}\int_{E_i}^{E_{t0}} N_t\left(1-\frac{1}{1+\frac{1}{g}\exp\left(\frac{E_F-E_t}{KT}\right)}\right)\mathrm{d}E_t, \tag{7}$$

where A_{TG} denotes the area of the TG. Note that Eq. (7) is a two-dimensional function related to N_t and E_t, both of which are related to the trap energy level distribution.

In this way, based on the relationship between $N_{transfer}$ and $N_{Trapped}$:

$$N_{transfer} = N_{e0} - N_{Trapped}(E_t, N_t). \tag{8}$$

Eq. (1) can be further written as Eq. (9). Thus, the CTE fluctuates with changes in E_t and N_t.

$$\mathrm{CTE} = \frac{N_{e0} - N_{Trapped}(E_t, N_t)}{N_{e0}}\times 100\%. \tag{9}$$

In the actual manufacturing process, owing to fluctuations in CMOS technology, for the same pixel design, the position of the trap energy level is not always a single constant[23, 24]. In addition, it is demonstrated in Ref. [25], that the common trap energy level distribution includes Gaussian (as shown in Eqs. (10) and (11)) and exponential distributions (as shown in Eqs. (12) and (13)).

$$\mathrm{Gaussian} \sim \begin{cases} E_t \neq E_i \\ N_t = N_{max}\exp\left(-\left(\dfrac{E_t-E_0}{\sqrt{2}E_S}\right)^2\right), \end{cases} \tag{10}$$

$$N_{Trapped\text{-}Gaussian}(E_t, N_t) = A_{TG}\int_{E_i}^{E_{t0}} N_{max}\exp\left(-\left(\frac{E_t-E_0}{\sqrt{2}E_S}\right)^2\right)\times\left(1-\frac{1}{1+\frac{1}{g}\exp\left(\frac{E_F-E_t}{KT}\right)}\right)\mathrm{d}E. \tag{11}$$

In the Gaussian distribution, the trap energy level is not equal to the intrinsic Fermi level and is continuously distributed in the silicon band gap. Moreover, the center of the trap energy level deviates from the center of the silicon band gap, as indicated in Eq. (10). E_0 is the average value of the Gaussian distribution, and it ranges from 0 to 1.12 eV.

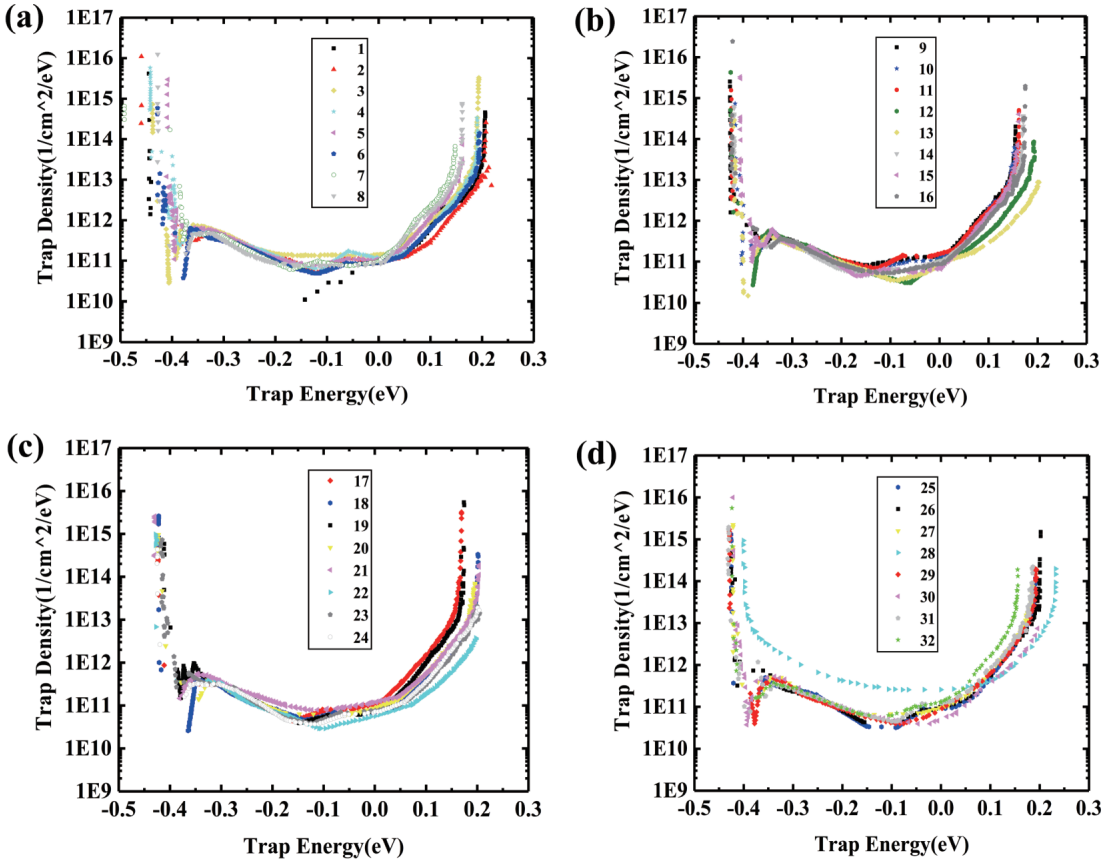

Fig. 3. (Color online) Different trap energy level distributions. (a) 1–8 sets of measured distribution data of Si/SiO_2 interface state. (b) 9–16 sets of measured distribution data of Si/SiO_2 interface state. (c) 17–24 sets of measured distribution data of Si/SiO_2 interface state. (d) 25–32 sets of measured distribution data of Si/SiO_2 interface state.

E_S is the variance of the Gaussian distribution, and it is slightly smaller than this band gap width. When Eq. (10) is inserted into Eq. (7), $N_{Trapped}$ exhibiting a Gaussian distribution of the trap energy level can be further expressed as $N_{Trapped\text{-}Gaussian}(E_t, N_t)$ in Eq. (11).

$$\text{Exponential} \sim \begin{cases} E_t \neq E_i \\ N_t = N_{max}\exp\left(-\left|\dfrac{E_t - E_0}{E_S}\right|\right) \end{cases}, \tag{12}$$

$$N_{Trapped\text{-}Exponential}(E_t, N_t) = A_{TG}\int_{E_i}^{E_{t0}} N_{max}\exp\left(-\left|\frac{E_t - E_0}{E_S}\right|\right)\times \left(1 - \frac{1}{1 + \frac{1}{g}\exp\left(\frac{E_F - E_t}{KT}\right)}\right)\mathrm{d}E. \tag{13}$$

In the exponential distribution, the trap energy level is not equal to the intrinsic Fermi energy level. The center of the trap energy level also deviates from the center of the silicon band gap, as indicated in Eq. (12). By substituting Eq. (12) into Eq. (7), $N_{Trapped}$ exhibiting an exponential distribution of the trap energy level can be further expressed as $N_{Trapped\text{-}Exponential}(E_t, N_t)$ in Eq. (13).

3. Simulation results

This study verifies the model in detail by using Gaussian trap energy level distribution, exponential trap energy level distribution and 32 sets of measured trap energy level distributions, which are supplied by Chongqing Optoelectronics Research Institute, the relationship between trap energy level E_t and trap state density N_t as shown in Figs. 3(a)–3(d). The Si/SiO_2 system is composed of 60 nm dry oxygen grown on P-type monocrystalline silicon, the interface state distribution of Si/SiO_2 system was measured by MOS-C-V method with Keithley 82win C-V tester.

To verify the mathematical model proposed in this paper, simulations were conducted on the Synopsys Sentaurus TCAD 2018. First, process simulation design was carried out in the Sprocess module in TCAD with reference to the advanced CMOS process flow. This step acquired process simulation files with doping, material and boundaries information, etc. After that, the files were imported into the Sdevice module in TCAD for physical characteristics simulation. By adding lighting models, trap models, and pixel timing spice models, the 4T pixel model is equipped with various physical characteristics. Finally, we used the 4T pixel model to simulate the number of untransferred charges when the duration of the TG falling edge is equal to the emission time constant of electrons.

The CIS PPD 4T pixels are simulated by a 0.18 μm CIS technology, and the structural parameters of the simulation are listed in Table 1. The temperature and electron capture cross-section were set to 300 K and 1×10^{-15} cm^{-2}, according to Ref. [24], respectively. In addition, at low light intensity levels (less than 1 $\mu W/cm^2$), the illumination intensity and time were set to 1.46×10^{-7} W/cm^2 and 100 μs, according to the literature[20].

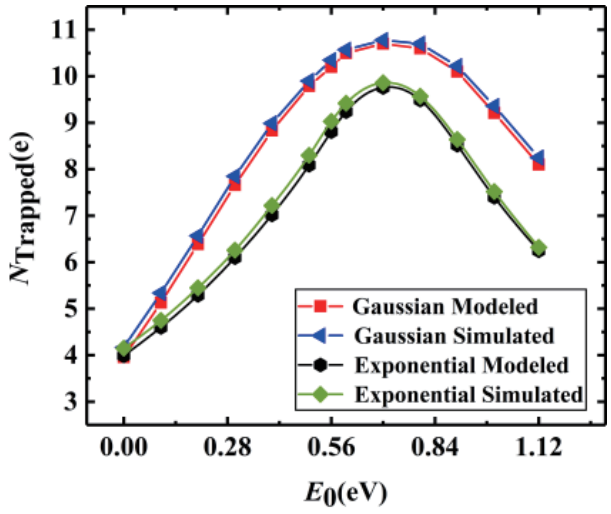

Fig. 4. (Color online) Variations in $N_{Trapped}$ with the mean value E_0 under Gaussian and exponential distributions.

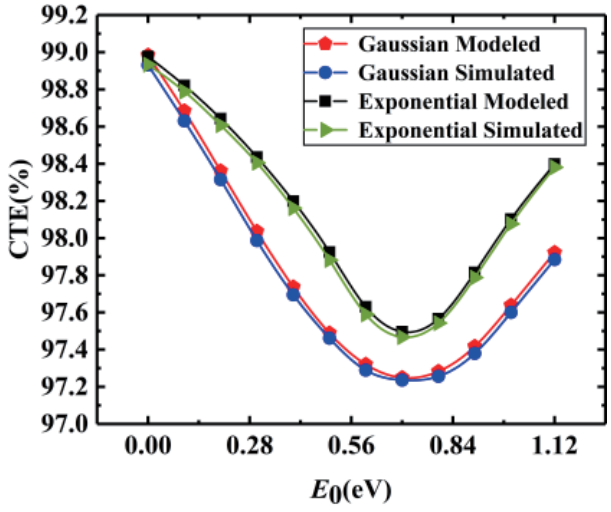

Fig. 5. (Color online) Variations in CTE with the mean value E_0 under Gaussian and exponential distributions.

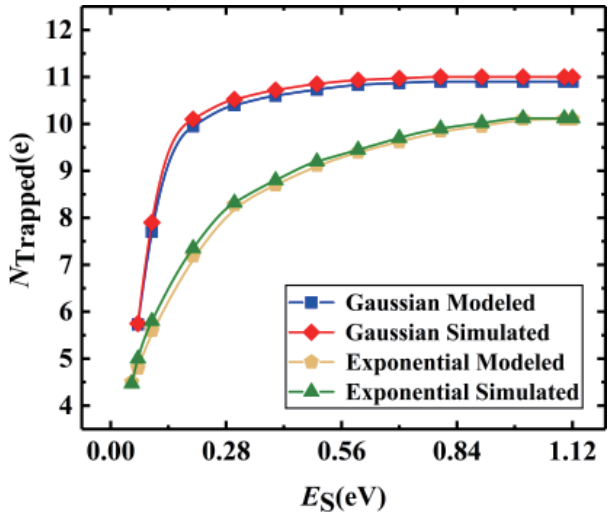

Fig. 6. (Color online) Variations in $N_{Trapped}$ with different variances E_S under Gaussian and exponential distributions.

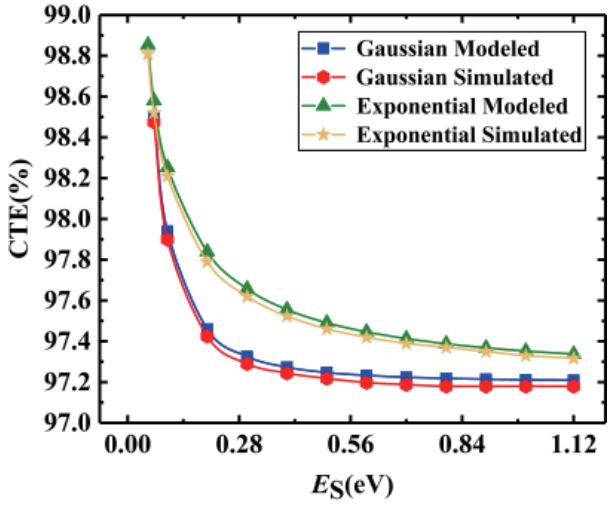

Fig. 7. (Color online) Variations in CTE with different variances E_S under Gaussian and exponential distributions.

3.1. Specific curve results of $N_{Trapped}$ and CTE changing with E_0 under Gaussian and exponential distributions

Fig. 4 and Fig. 5 show the variations in $N_{Trapped}$ and CTE, respectively, with the mean value E_0 for both the mathematical model and simulation when the interface state trap energy level follows Gaussian and exponential distributions. In Fig. 4 and Fig. 5, the model results and simulation results not only exhibit the same variation trend but also possess similar values. Specifically, when E_0 changes from 0 to 0.7 eV, and then from 0.7 to 1.12 eV, regardless of whether the energy level follows Gaussian or exponential distribution, the $N_{Trapped}$ value from the simulation results and model results increases first and then decreases. Meanwhile, the change trend of the CTE with E_0 is opposite to that of $N_{Trapped}$.

3.2. Specific curve results of $N_{Trapped}$ and CTE changing with E_s under Gaussian and exponential distributions

Fig. 6 and Fig. 7 display the variations in $N_{Trapped}$ and CTE with the variance E_S for both the mathematical model and simulation when the interface state trap energy level follows the Gaussian and exponential distributions. Specifically, as E_S increases to 1.12 eV, regardless of whether the energy level follows Gaussian distribution or exponential distribution, in both the modeling and simulation results, the value of $N_{Trapped}$ increases, and the value of CTE decreases.

3.3. Specific curve results of $N_{Trapped}$ and CTE changing under measured trap energy level distributions

In order to reflect the relationship between $N_{Trapped}$ and trap energy level distributions, trap charge density is calculated as Eq. (14), when the measured trap energy level distributions in Fig. 3 and Eq. (7) are used to verify the proposed model.

$$N_{it} = \int_{E_i}^{E_{t0}} N_t(E_t)\,\mathrm{d}E_t\,. \tag{14}$$

Fig. 8 and Fig. 9 show the variations in $N_{Trapped}$ and CTE, respectively, with trap charge density N_{it} for both the mathematical model and simulation when the interface state trap energy level follows different distributions in Fig. 3. It can be

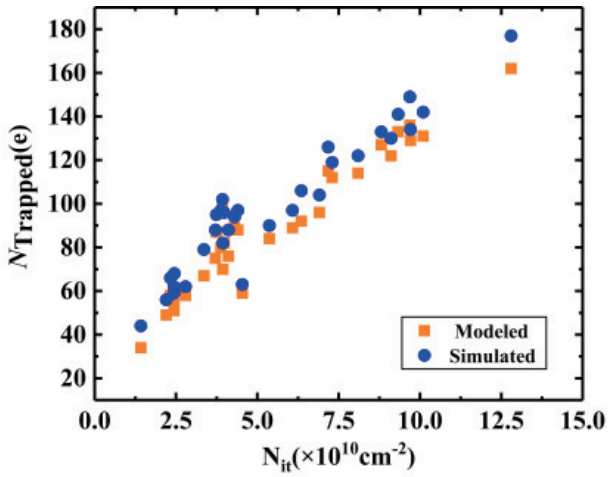

Fig. 8. (Color online) The variations in $N_{Trapped}$ with trap charge density N_{it}.

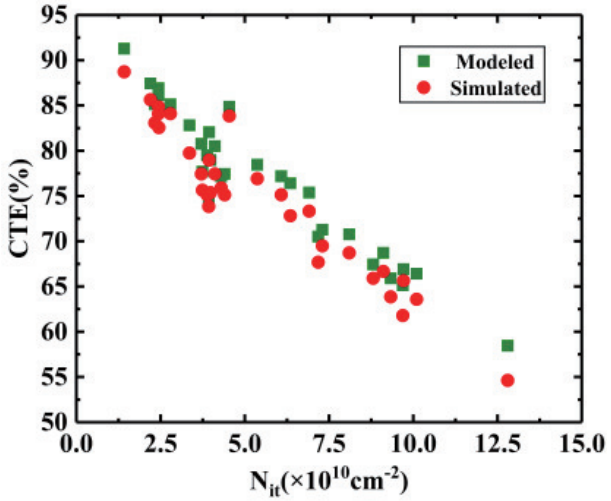

Fig. 9. (Color online) The variations in CTE with trap charge density N_{it}.

seen that the model results and simulation results not only exhibit the same variation trend but also possess similar values. Specifically, the $N_{Trapped}$ value from the simulation results and model results increases with the increases of trap charge density. Meanwhile, the change trend of the CTE with N_{it} is opposite to that of $N_{Trapped}$.

4. Conclusions

In summary, an analytical model for quantifying the incomplete charge transfer caused by Si/SiO_2 interface state traps in the TG channel under low illumination has been established for the first time. This model can predict the variation rules of the number of untransferred charges and charge transfer efficiency when the trap energy level follows different distributions. The model has been verified with TCAD simulations, and the consistency between model and simulation results proves the accuracy of the proposed model in this paper. The proposed model provides beneficial theoretical guidance for the circuit design and analysis of CISs.

Acknowledgments

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