ARTICLES

Journal of Semiconductors
(2023) 44, 114103
doi: 10.1088/1674-4926/44/11/114103

Performance optimization of tri-gate junctionless FinFET using channel stack engineering for digital and analog/RF design

Devenderpal Singh†, Shalini Chaudhary, Basudha Dewan, and Menka Yadav

Department of Electronics and Communication Engineering, Malaviya National Institute of Technology, Jaipur, Rajasthan-302017, India

Abstract: This manuscript explores the behavior of a junctionless tri-gate FinFET at the nano-scale region using SiGe material for the channel. For the analysis, three different channel structures are used: (a) tri-layer stack channel (TLSC) (Si–SiGe–Si), (b) double layer stack channel (DLSC) (SiGe–Si), (c) single layer channel (SLC) (Si). The *I*–*V* characteristics, subthreshold swing (SS), drain-induced barrier lowering (DIBL), threshold voltage (V_t), drain current (I_{ON}), OFF current (I_{OFF}), and ON-OFF current ratio (I_{ON}/I_{OFF}) are observed for the structures at a 20 nm gate length. It is seen that TLSC provides 21.3% and 14.3% more ON current than DLSC and SLC, respectively. The paper also explores the analog and RF factors such as input transconductance (g_m), output transconductance (g_{ds}), gain (g_m/g_{ds}), transconductance generation factor (TGF), cut-off frequency (f_T), maximum oscillation frequency (f_{max}), gain frequency product (GFP) and linearity performance parameters such as second and third-order harmonics (g_{m2}, g_{m3}), voltage intercept points (VIP_2, VIP_3) and 1-dB compression points for the three structures. The results show that the TLSC has a high analog performance due to more g_m and provides 16.3%, 48.4% more gain than SLC and DLSC, respectively and it also provides better linearity. All the results are obtained using the VisualTCAD tool.

Key words: short channel effects (SCEs); junctionless FinFET; analog and RF parameters; SiGe

Citation: D Singh, S Chaudhary, B Dewan, and M Yadav, Performance optimization of tri-gate junctionless FinFET using channel stack engineering for digital and analog/RF design[J]. *J. Semicond.*, 2023, 44(11), 114103. https://doi.org/10.1088/1674-4926/44/11/114103

1. Introduction

The scaling of conventional MOSFET introduces various short channel effects in the nanoscale that needs to be addressed to assure the optimum performance of any device[1, 2]. The FinFET device has recently attracted attention due to superior electrical properties at sub-22 nm technology nodes. It has better channel control than the conventional MOSFET structure[3]. Various novel devices have been investigated to diminish the short channel effects, such as double gate TFET[4], double gate and tri-gate FinFET[5], omega FinFET[6], and junctionless FinFET[7]. A junctionless transistor (JLT) is an emerging concept with simple fabrication steps compared to conventional MOSFETs because, in the junctionless FinFET, the source, channel, and drain have constant concentrations. The other difference between a junctionless FinFET and a conventional MOSFET is that the drain current flows through the bulk of the semiconductor in a junctionless FinFET and flows through the channel in a conventional MOSFET[8, 9].

Another solution to minimize the short channel effects is to employ beyond silicon materials, for example**,** Ge, SiGe, GaAs, and group $\mathrm{III}-\mathrm{V}$ materials. W T Chang *et al*.[10] presented the threshold voltage shifting and transconductance with the strained SiGe channel dimension variation. R Das *et al*.[11] proposed the structure of the tri-gate heterojunction FinFET with various configurations of the gate dielectric and metal stacks. It was found that the junction formed between Ge and Si produces a lower leakage current than conventional MOSFETs, but it had more subthreshold swing (SS). M J Kumar *et al*.[12] reported the strain effect on the threshold voltage (V_t) of strained Si/SiGe MOSFETs using the mathematical model. It also discussed the effect of germanium content on V_t of the bulk MOSFET. T V Singh *et al*.[13] presented the impact of Ge content in the SiGe channel in a cylindrical MOSFET.

V. Venkkataraman *et al*.[14] derived the expression of threshold voltage considering the Si strain effect on the SiGe channel. Fei Ding *et al*.[15] proposed a p-channel FinFET with a heterogeneous channel region ($Si\text{-}Si_{0.9}Ge_{0.1}$) and compared it with a conventional p-channel FinFET. It was observed that the hetero-channel structure provides more ON current than the conventional one, and a low Ge mole fraction can enhance performance.

The objective of this manuscript is to analyze the performance of the device with a channel stack using a compound semiconductor material. Various studies have been presented in the literature to analyze the digital, analog/RF and linear characteristics of FinFET and junctionless devices[16, 17]. However, according to our research, the performance evaluation of tri-gate junctionless FinFET with a SiGe based stack channel, is required to analyze the analog/RF and linearity parameters. Since modern communication systems operate in the gigahertz frequency range and require low intermodulation linear operation for detecting the weak signal, the linearity parameters play a vital role in high frequency domain.

Key contributions in the proposed work: In the manuscript, the following objectives are setups for the tri-gate junctionless FinFET device:

(1) Channel stack engineering in the SOI junctionless tri-gate FinFET.

Correspondence to: D Singh, 2020rec9502@mnit.ac.in
Received 11 FEBRUARY 2023; Revised 3 MARCH 2023.

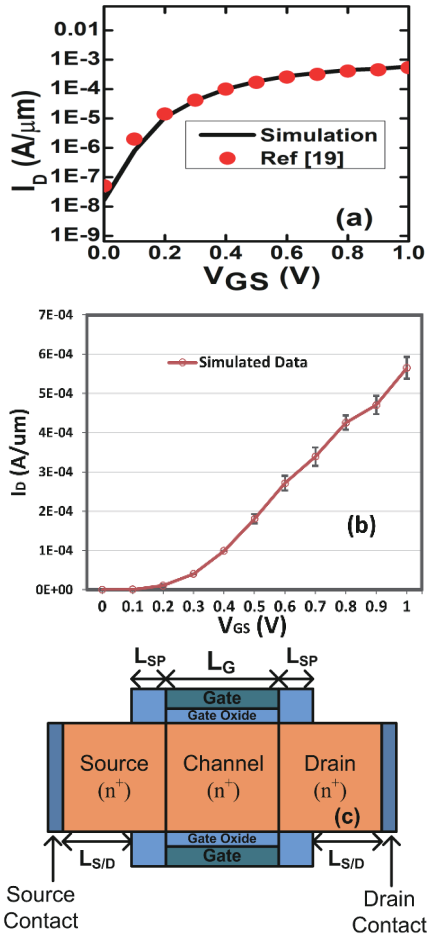

Fig. 1. (Color online) (a) Calibration of the tool against the experimental data presented in Ref. [19]. (b) Simulated *I*–*V* curve with error bars. (c) Cross-sectional representation of the junctionless FinFET device.

(2) Analysis of digital parameters for different channel stacks of the device.

(3) Analysis of RF/analog and linearity parameters.

(4) The comparison with the existing devices presented in the literature.

The other sections in the manuscript are categorized as follows: Section 2 narrates the simulation setup, the device structure is presented in Section 3, Section 4 represents the general fabrication flow of the device, and Section 5 is the results and discussion that include the analysis of the proposed structure for digital, analog applications and linearity performance. Finally, Section 6 concludes the manuscript.

2. Calibration setup and simulation flow

Cogenda Genius VisualTCAD software is utilized for structure simulation[18]. Since the device is heavily doped, the Lombardi and Philips mobility models are considered for the simulation of Si and SiGe materials, respectively. Eq. (1) represents the Lombardi surface model mobility equation[18]:

$$\frac{1}{\mu_t} = \frac{1}{\mu_b} + \frac{1}{\mu_{ac}} + \frac{1}{\mu_{sr}}, \tag{1}$$

where μ_t is the total mobility, μ_b is the doping-dependent bulk mobility that occurs due to ionized impurity scattering, μ_{ac} is the mobility degradation resulting from acoustic phonon scattering, and μ_{sr} represents the mobility degradation due to surface roughness scattering.

The Philips mobility model for the SiGe material given as Eq. (2)[18].

$$\frac{1}{\mu_{0,n}} = \frac{1}{\mu_{Lattice,n}} + \frac{1}{\mu_{D+A+p}}, \tag{2}$$

where $\mu_{0,n}$ is the electron mobility, $\mu_{Lattice,n}$ is the electron mobility due to lattice scattering, and μ_{D+A+p} is the mobility due to donor (D), acceptor (A), screening (p).

The hot carrier model is considered to assess the effect of hot carriers. The Schokley-Read-Hall (SRH) model is used to incorporate carrier generation and recombination. The parameters, for example, the Drift-Diffusion model, and Poisson equation solver, are also defined for the simulation. The Drift-Diffusion model solves the Genius code of the device for constant lattice temperature. Its main function is to solve the partial differential equation, known as the Poisson equation, along with the continuity equation of charge carriers[18]. The VisualTCAD Genius tool uses the following Poisson's equation to solve the partial differential Eq. (3) of the device[18],

$$\nabla \cdot (\varepsilon \nabla \psi) = -q(p - n + N_D^+ - N_A^-), \tag{3}$$

where ψ represents the electrostatic potential of the vacuum level, p and n are the hole and electron concentrations, respectively, N_D^+, N_A^- are the impurity concentrations, and q is the charge of the electron.

The tool is calibrated as per the data presented in Ref. [19]. The physical specifications such as electron mobility (μ_1), exponent of the bulk term of the Lombardi surface mobility model (α), and doping parameter (CSN.LSM) are carefully modified to match the experimental data reported in Ref. [19]. These parameters are taken as: EXN1.LSM (α) = 0.8, MUN1.LSM (μ_1) = 50 $cm^2/(V{\cdot}s)$, CSN.LSM = 3.4×10^{20} cm^{-3}. For SiGe material, Philips model is used to simulate the device.

Fig. 1(a) represents the simulated calibration against the reported experimental data[19] at V_{DS} = 0.9 V. It depicts that the experimental data in Ref. [19] matches with the simulated data calculated using VisualTCAD Genius simulation. In the graph, the drain current is taken in the log scale and V_{GS} is varied up to 1 V. For the calibration, the gate length is taken as 26 nm, Fin height is 29 nm, Fin thickness is 10 nm and equivalent oxide thickness (EOT) for high-*k* dielectric is 1 nm, as per the experimental data presented in Ref. [19] for Si material. Fig. 1(b) depicts the percentage change in the simulation data of *I*–*V* curve with the experimental data reported in Ref. [19]. In this curve, the error bars represent the deviation of simulated data with experimental data and there is 3%–5% variation between both data. Fig. 1(c) is the general cross-sectional representation of the junctional FinFET device with different dimensions. The device consists of HfO_2 as the high-*k* gate dielectric material, spacers (HfO_2) to suppress the source/drain–gate capacitances, and metal (work function = 4.9 eV) for the gate electrode. Fig. 2 represents the simulation flow of the device in VisualTCAD. It starts with defining the parameters such as Fin height, thickness, oxide thickness, source/drain length, spacer length, gate length. The script of the device is written in the VisualTCAD text editor and meshing is defined.

3. Proposed device structure

Fig. 3(a) represents the proposed structure of the device with Tri layer Stack Channel (TLSC) used for simulation; the

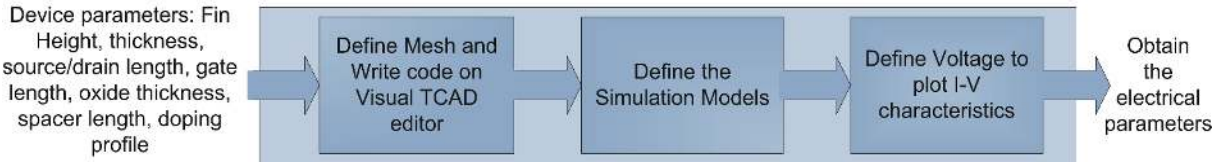

Fig. 2. (Color online) Simulation flow of the device in VisualTCAD genuis simulator.

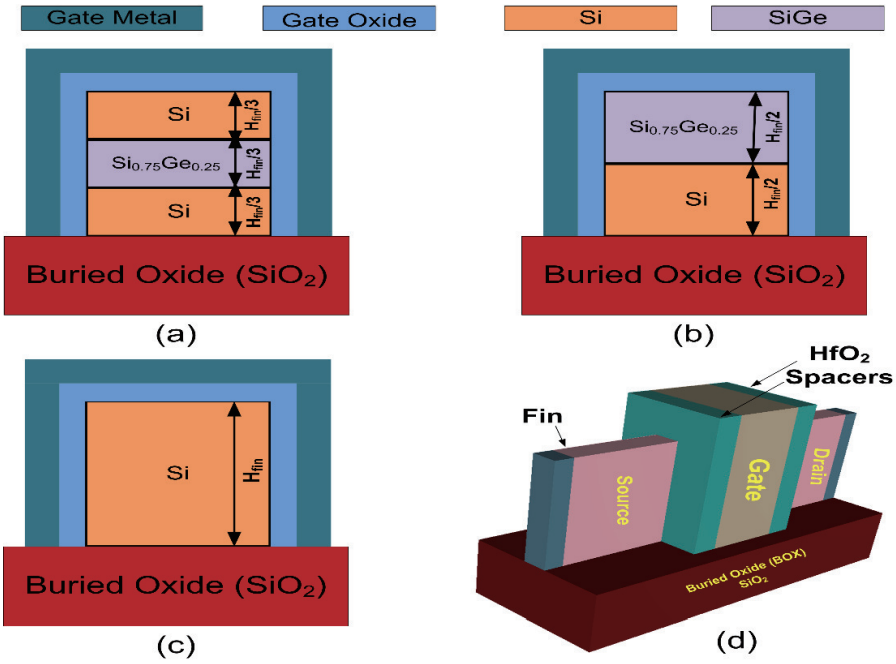

Fig. 3. (Color online) Cross sectional view of junctionless FinFET. (a) Tri layer stack channel (TLSC), (b) double layer stack channel (DLSC), (c) single layer channel (SLC), (d) 3D view of trigate FinFET.

channel is formed as the stack of Si + $Si_{0.75}Ge_{0.25}$ + Si (here, $Si_{0.75}Ge_{0.25}$ represents that the mole fractions of Si and Ge are 0.75 and 0.25 respectively), here, the SiGe layer is between the layers of Si, so the top and bottom of the Fin have same layers. Fig. 3(b) is the 2D view of the channel with double layer stack channel (represented as DLSC); in this, the channel is the combination of Si + $Si_{0.75}Ge_{0.25}$, Fig. 3(c) illustrates the 2D front view of the single layer channel (Si Channel). The height of the layers is equally divided in the DLSC and TLSC. The other parameters such as gate length, source/drain length, Fin thickness, spacer length are shown in Table 1. The doping concentration of source, drain and channel is 1×10^{19} cm^{-3}. The simulated 3D view of the proposed device is presented in Fig. 3(d). According to the width quantization rule, the effective width (W_{eff}) of the device that is given as $2H_{Fin} + T_{Fin}$ [20].

Figs. 4(a)–4(c) represent the contour plots of the valence band (VB) and conduction band (CB) energy for the structures TLSC, DLSC, and SLC, respectively, which is obtained at V_{DS} = 0.7 V. The figure shows the variation of energy VB and CB along the channel and Fin height. Since the channel stack is different for the three structures; only the energy variation in the channel is shown here. Figs. 4(a)–4(c) show that the energy increases with negative magnitude along the channel for the three structures and the lowest difference between CB energy and VB energy is obtained for the TLSC structure, which is shown graphically in Fig. 4(d). It depicts the energy-band diagram of the three structures (TLSC, DLSC, SLC), based on the contour plot and it is plotted for source, channel and drain regions. The figure shows that the band-gap for SLC, DLSC and TLSC structures in the source and drain region is approximately the same due to the same material (silicon) but it is different in the channel region due to stacking of the materials in the three structures. The band-gap for SLC is 1.1 eV, for DLSC, 0.89 eV and for TLSC, 0.85 eV, approximately. The CB in TLSC has a steeper slope than DLSC and SLC from the source–channel to the channel–drain region; this increases the electron flow from source to drain and increases the drain current.

4. Fabrication process flow of the device

Fig. 5 represents the general process flow of the device. It starts with the preparation of the Si wafer (Fig. 5(a)), after that the SiO_2 layer is deposited on the Si substrate using thermal oxidation (Fig. 5(b)). After this, the SOI layer is deposited and the Si layer is formed as shown in Figs. 5(c) and 5(d). After the formation of the Si layer, the SiGe-Si stack is fabricated (Figs. 5(e) and 5(f)). The stack of the Fin is patterned using electron beam lithography as shown in Fig. 5(g). The gate stack (HfO_2 oxide-gate material) is formed as shown in Figs. 5(h) and 5(i). After that ion implantation (n+) is done to form source and drain regions (Fig. 5(j)). Then, the HfO_2 layer is deposited on the spacer regions (Fig. 5(k)).

5. Results and analysis

This section analyses the performance of SLC, DLSC, and TLSC. The height of the Fin (H_{Fin}) is taken as 36 nm, and the

Table 1. Parameters and dimensions used for simulation.

	Device structures		
	Tri layer stack channel (TLSC)	Double layer stack channel (DLSC)	Single layer channel (SLC)
Source/Drain material	Si	Si	Si
Gate length (L_G) (nm)	20	20	20
Source/Drain length ($L_{S/D}$) (nm)	30	30	30
Channel material	Si + $Si_{0.75}Ge_{0.25}$+Si	Si + $Si_{0.75}Ge_{0.25}$	Si
Spacer material	HfO_2	HfO_2	HfO_2
Spacer length (L_{SP}) (nm)	7	7	7
Total Fin height (H_{Fin}) (nm)	36	36	36
Height of each layer (nm)	12	18	36
Fin thickness (T_{Fin}) (nm)	7	7	7

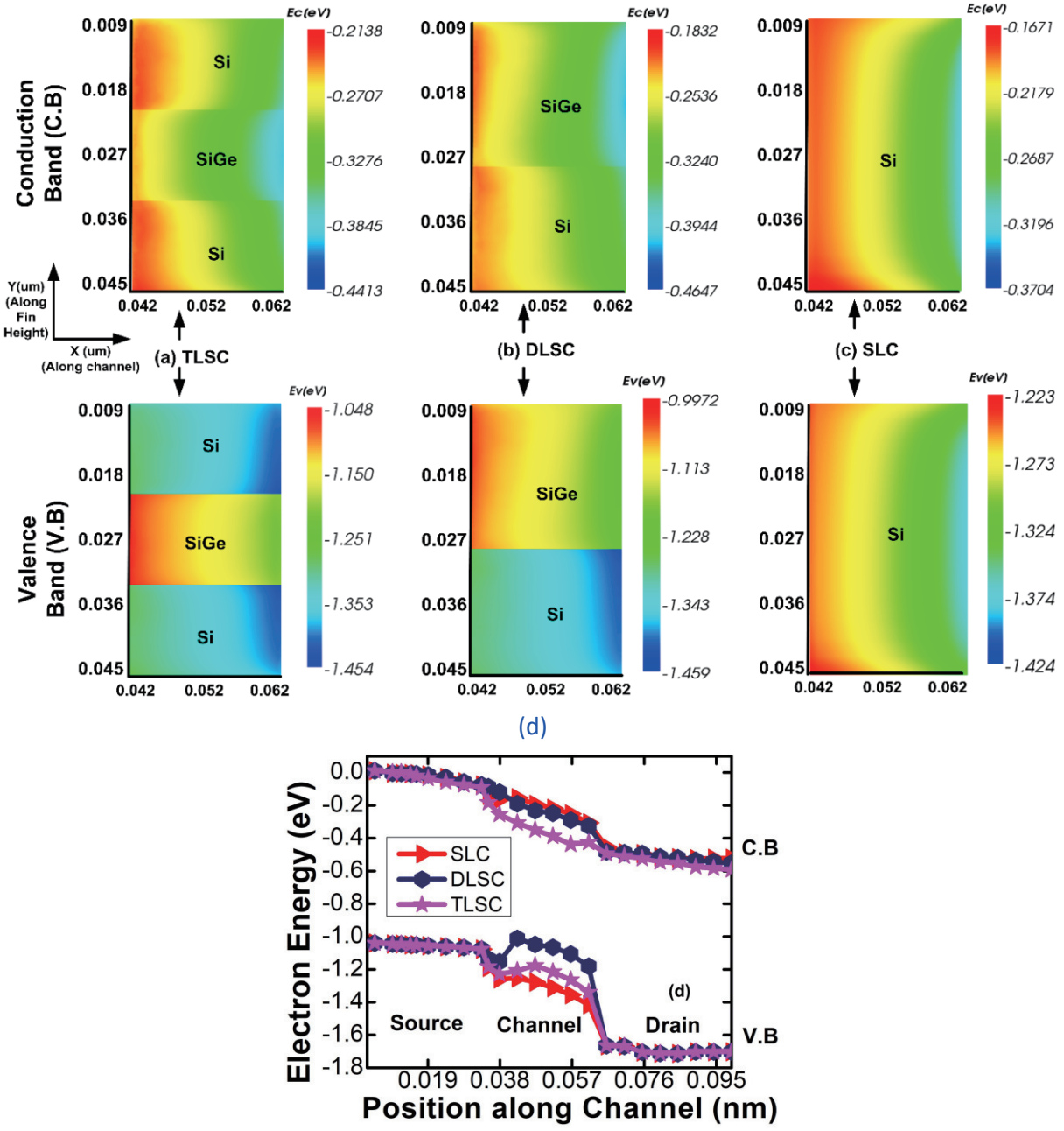

Fig. 4. (Color online) Visual TCAD simulated contour plots of valence band and conduction band energy along the channel and Fin height at V_{DS} = 0.7 V and V_{GS} = 1 V for (a) TLSC, (b) DLSC, (c) SLC. (d) Energy-band diagram of the three structures based on the contour plot.

Fin thickness (T_{Fin}) is taken as 7 nm for the three structures. The digital parameters such as SS, DIBL, I_{ON}/I_{OFF} and RF/Analog parameters: transconductance parameter (g_m), transconductance generation factor (TGF), output transconductance (g_{ds}), voltage gain (A_v), cut-off frequency, maximum oscillation frequency and linearity parameters are compared for the

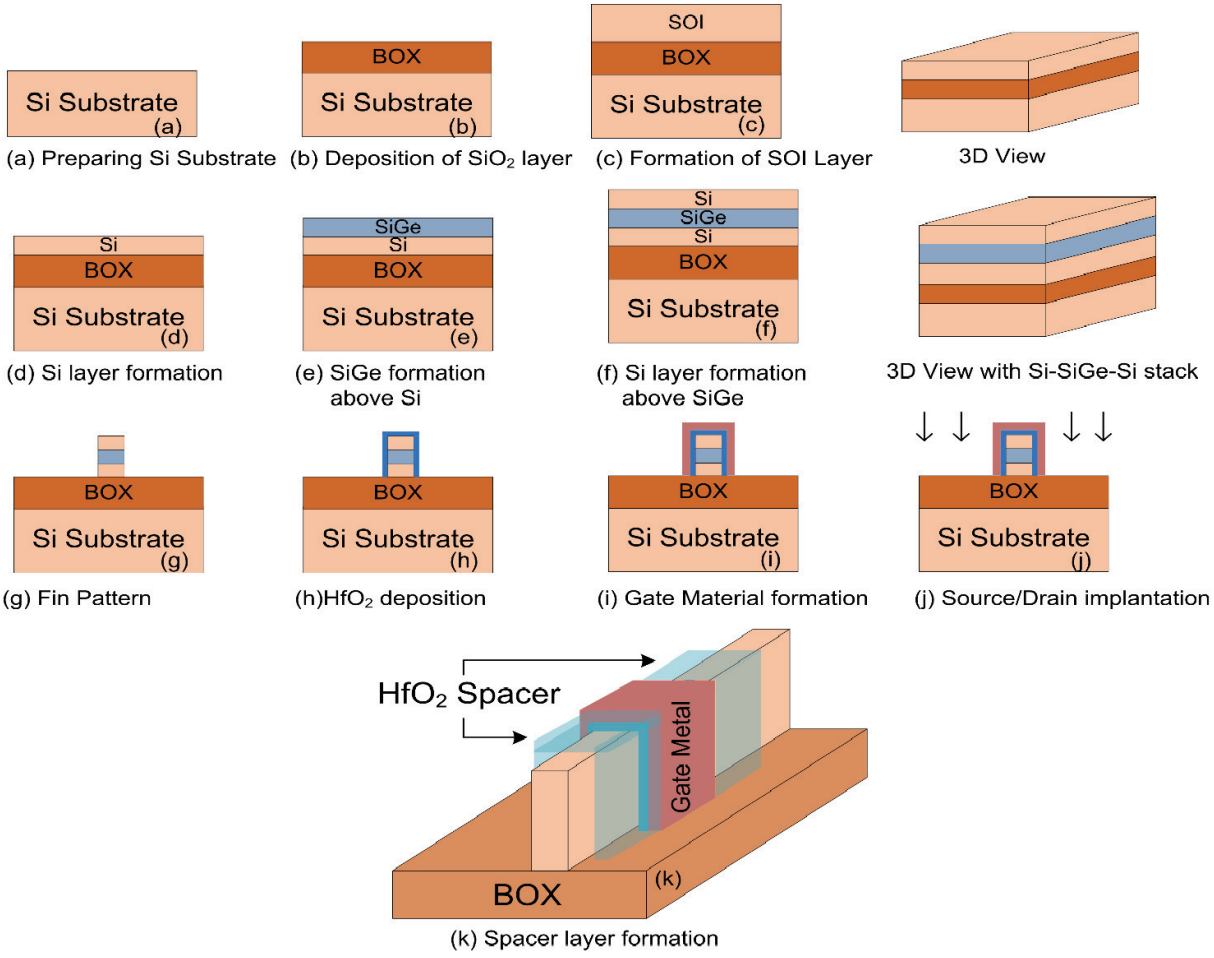

Fig. 5. (Color online) Fabrication process flow of the proposed device.

three structures at gate length (L_G) 20 nm and supply voltage 0.7 V. The parameters are taken according to the IRDS-2021 "5 nm" node-range[21].

To compare the conduction mechanism, Fig. 6 shows the electron density distribution in the three structures along the channel at the ON state (V_{GS} = 1 V) and V_{DS} is taken as 0.7 V. Fig. 6(a) represents that TLSC has two Si–SiGe junctions and its electron density is higher than the DLSC structure shown in Fig. 6(b), which has one SiGe–Si junction. Fig. 6(c) depicts the electron density distribution in the SLC structure along the channel and it is uniform throughout the height of the channel. The electron density in the SLC is lower than the DLSC and TLSC as it has only one silicon layer in the channel.

5.1. Analysis of digital performance parameters

Fig. 7(a) represents the current–voltage (I–V) characteristics of SLC, DLSC, and TLSC structures. It shows that the TLSC structure has more drain current (I_{ON}) than the other structures (DLSC and SLC) due to the hetero-layer of Si–$Si_{0.75}Ge_{0.25}$–Si. In the TLSC structure, the SiGe layer is between the two Si layers, which creates two Si–SiGe junctions and the strained lattice structure that can enhance carrier mobility. When the Si channel is strained, the spacing between the energy band is altered, as shown in Eq. (4). This can lead to the effective mass of the electrons, which can enhance their mobility. When a voltage is applied to the gate of the FinFET, an electric field is generated that controls the flow of carriers through the channel region. The higher mobility of carriers in the TLSC allows for more efficient flow of carriers though the channel, leading to a higher drive current**.** As Fig. 6(a) shows that TLSC has high electron density due to two Si–SiGe junctions, the resulting drain current is shown in Fig. 7(a).

The parameters related to SiGe such as modified band gap and density-of states, are given in Eqs. (4)–(6)[22]:

$$\Delta E_G\,(\mathrm{SiGe}) = 0.467x, \tag{4}$$

$$N_V\,(\mathrm{SiGe}) = (0.6x + 0.04\,(1-x)) \times 10^{19}\ \mathrm{cm}^{-3}, \tag{5}$$

$$\varepsilon\,(\mathrm{SiGe}) = 11.9 + 4.2x, \tag{6}$$

where ΔE_G (SiGe) represents the reduction in the SiGe band gap from Si, N_V (SiGe) is the density-of-states in valence band, ε (SiGe) is permittivity of SiGe, and x is the mole fraction of Ge. The modification in band gap of SiGe causes the increase in mobility, hence drain current increases. The drain current in TLSC is more than DLSC and SLC because it has two Si–SiGe junctions.

The value of the drain current for the TLSC is 0.342 mA/μm, for DLSC is 0.28 mA/μm and for SLC is 0.299 mA/μm. The logarithmic plot is also shown in Fig. 7(a); it represents that the SLC structure has the lowest OFF current (I_{OFF}) and DLSC, TLSC structures have an almost equal OFF current but more than SLC. This is because the SiGe layer in DLSC and TLSC induces strain in the channel region, which enhances the diffu-

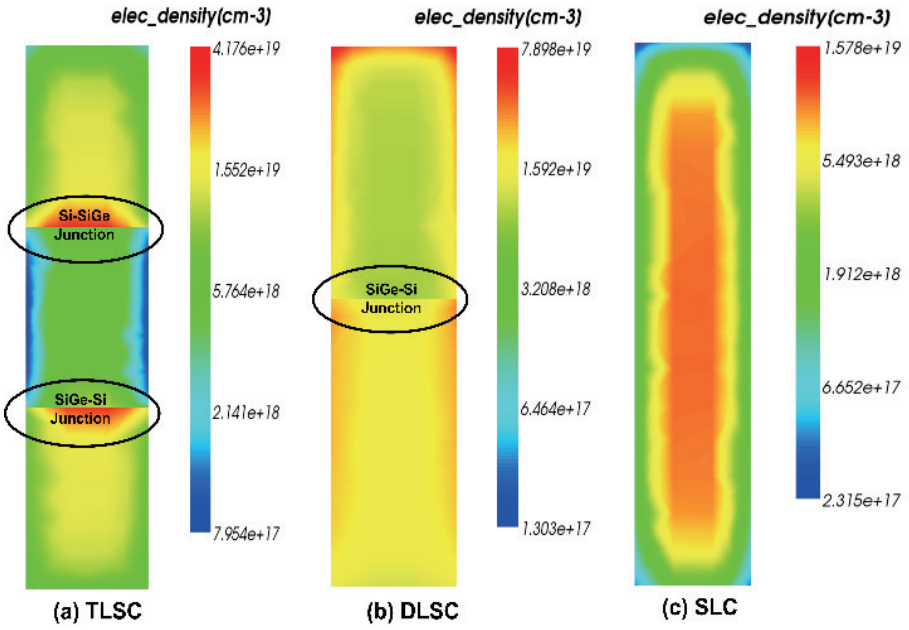

Fig. 6. (Color online) Electron density distribution in (a) TLSC structure, (b) DLSC structure, and (c) SLC structure.

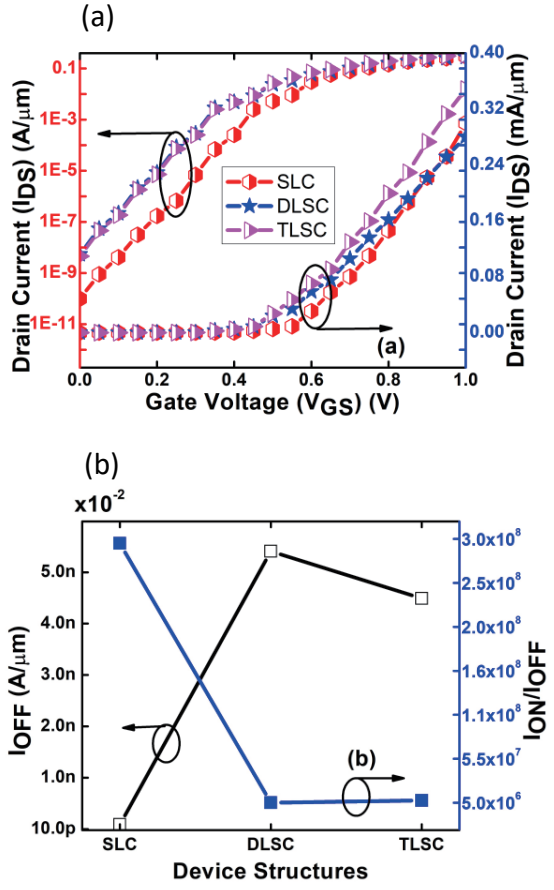

Fig. 7. (Color online) (a) *I*–*V* characteristics. (b) Comparison of I_{OFF} and I_{ON}/I_{OFF} for SLC, DLSC and TLSC structures.

sion of dopants and increases the formation of the leakage path. Additionally, TLSC and DLSC typically have higher parasitic capacitances due to additional interfaces in the channel structure, which increases the tunnelling current and contribute to the overall leakage current**.** Fig. 7(b) represents the comparison of I_{OFF} and I_{ON}/I_{OFF}, representing that SLC has less I_{OFF}, more I_{ON}/I_{OFF} than DLSC and TLSC, but these structures have I_{ON}/I_{OFF} more than 10^6, which is required for better performance of a device according to IRDS-2021[21]. These values are obtained at V_{DS} = 0.7 V and V_{GS} is varied from 0 to 1 V.

The mathematical expression for SS is given below in Eq. (7)[5]. The SS is a current–voltage characteristics that determines the transistor's behaviour in sub-threshold region. It represents the measure of how fast a transistor can be turned ON/OFF. Its value is limited by thermal voltage (kT/q), which results in the limit of SS value at 60 mV/dec. To perform a device effectively, the SS value must be near to 60 mV/dec. In this paper, the value of SS for TLSC, DLSC and SLC are 62.29, 62.34, and 61.64 mV/dec respectively, at fixed drain bias 0.7 V. The SS values of SLC, DLSC, and TLSC structure are compared with other devices presented in the literature, as shown in Table 2.

$$\mathrm{SS} = \left[\frac{\mathrm{d}\log(I_D)}{\mathrm{d}V_{\mathrm{GS}}}\right]^{-1} = \ln(10)\,\frac{kT}{q}\left(1+\frac{C_{\mathrm{d}}}{C_{\mathrm{ox}}}\right), \tag{7}$$

where C_d is known as depletion capacitance, C_{ox} is the oxide capacitance, and $\frac{kT}{q}$ is the thermal voltage.

The DIBL is another parameter of the short channel effect which refers to threshold voltage reduction at higher drain bias. The value of the DIBL must be low for the better device operation. The DIBL is calculated by measuring the horizontal shift in sub-threshold characteristics divided by the change in drain voltage. The equation for the DIBL is given in Eq. (8)[5]. The values of the DIBL obtained by simulation for the three structures are given in Table 2 and these values are 29.6, 32.2, and 28.07 mV/V for the TLSC, DLSC and SLC structures, respectively.

$$\mathrm{DIBL} = \frac{|V_{\mathrm{th,lin}} - V_{\mathrm{th,sat}}|}{V_{\mathrm{DS,sat}} - V_{\mathrm{DS,lin}}}, \tag{8}$$

where $V_{th,lin}$, $V_{DS,lin}$ are threshold voltage and drain–source voltage in linear region, respectively, and $V_{th,sat}$, $V_{DS,sat}$ are threshold voltage and drain–source voltage in the saturation region, respectively.

Table 2. Summary of parameters of three junctionless structures in terms of I_{ON}, I_{OFF}, I_{ON}/I_{OFF}, SS, DIBL and V_t.

Parameters	TLSC (This work)	DLSC (This work)	SLC (This work)	Junctionless accumulation mode FinFET[23]	Junctionless FinFET[24]	Junctionless bulk FinFET[25]
Gate length (L_G) (nm)	20	20	20	20	20	20
Fin height (H_{Fin}) (nm)	36	36	36	10	10	20
Channel doping (cm^{-3})	1×10^{19}	1×10^{19}	1×10^{19}	5×10^{17}	2.7×10^{19}	1×10^{18}
I_{ON} (mA/μm)	0.342	0.280	0.299	0.1	0.39	0.18
I_{OFF}(A/μm) ($\times 10^{-2}$)	4.5×10^{-9}	5.42×10^{-9}	9.88×10^{-11}	1×10^{-10}	–	1.45×10^{-10}
I_{ON}/I_{OFF}	7.6×10^{6}	5×10^{6}	3×10^{8}	1×10^{6}	–	1.2×10^{6}
SS (mV/dec) (V_{DS} = 0.05 V)	62.67	62.76	61.94	–	–	–
SS (mV/dec) (V_{DS} = 0.7 V)	62.29	62.34	61.64	66	67.3	78
DIBL (mV/V)	29.6	32.2	28.07	–	56	42
V_t (V) (V_{DS} = 0.05 V)	0.334	0.332	0.433			
V_t (V) (V_{DS} = 0.7 V)	0.315	0.317	0.413	0.25	0.3	0.15

The performance analysis of the three structures is given in Table 2 and compared with other reported papers. The table compares the ON current (I_{ON}), OFF current (I_{OFF}), I_{ON}/I_{OFF}, SS, DIBL and V_t of the different structures. For comparison, the gate length is taken as 20 nm for TLSC, DLSC and SLC structures. The Table 2 shows that SiGe material stack channel has more ON current, more I_{ON}/I_{OFF}, less SS and DIBL than the reported papers. Hence, SiGe material-based stack channel improves the short channel effects.

The impact of channel structures on SS, DIBL, and threshold voltage (V_t) is shown as a bar graph in Fig. 8. It illustrates that TLSC has less V_t than the SLC but almost the same as the DLSC, because the SiGe layer in the channel, effectively increases the carrier mobility due to the strain effect; as a result, the ON current is higher and resulting in less V_t. In Fig. 8, the values are taken for V_{DS} = 0.7 V.

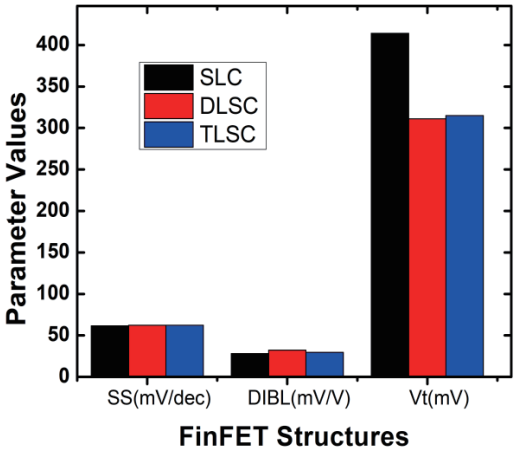

Fig. 8. (Color online) Comparative analysis of SLC, DLSC, TLSC in terms of SS, DIBL and V_t at V_{DS} = 0.7 V.

5.2. Analysis of analog/RF parameters

In this subsection, RF and analog parameters such as g_m, g_{ds}, TGF, f_T, f_{max}, gain, gain-frequency product (GFP) are evaluated and compared for the three structures. Eqs. (9) and (10) represent g_m and TGF, respectively[26]. Transconductance plays an essential role in the analysis of a circuit, and represents the change in drain current (I_D) with gate voltage (V_{GS}) at fixed drain bias. TGF demonstrates how effectively the current can attain the g_m value.

$$g_m = \frac{\partial I_D}{\partial V_{GS}}, \tag{9}$$

$$\mathrm{TGF} = \frac{g_m}{I_D}. \tag{10}$$

The variation of g_m and TGF for the three structures are shown in Fig. 9. The transconductance is a measure of how effectively the device can amplify an input signal. It is related to the carrier mobility or drain current. Since the TLSC structure provides more drain current due to higher mobility; the electron can move more easily through the channel and respond more quickly to changes in the gate voltage, and it leads to higher g_m. From Fig. 9, it is observed that the TLSC has the highest value of g_m due to the Si–SiGe–Si stack channel. Here, the maximum value of g_m is obtained in a moderate-to-strong inversion region, where the channel resistance changes rapidly with the V_{GS}. In this region, small changes in V_{GS} can result in large changes in drain current, which means the device can provide high g_m. Fig. 9 also represents the TGF value for the three structures with respect to the gate voltage. It shows that the TGF has almost the same value in the strong inversion region, it only changes in-subthreshold region. The value of g_m in the DLSC structure starts decreasing than SLC structures at a higher gate voltage, because the device is tri-gate and the gate is controlling the tri-layer stack channel (TLSC) equally in three directions (the top and bottom have the same layers), but in the DLSC, the top, and bottom of the FinFET have different layers; this asymmetric structure reduces the current in the double-layer stack channel, resulting in a decrease in g_m. Eq. (11) represents the output transconductance (g_{ds})[26]; it is the rate of change of drain current with drain-source voltage (V_{DS}) and determines the driving capability of a device[26]. The inverse of g_{ds} is known as output resistance (R_o). Fig. 10 shows the g_{ds} for three types of channel structures. Initially, g_{ds} is high in the linear region and starts decreasing with V_{DS}. It achieves a constant value in the saturation region. Fig. 10 also shows that the TLSC structure has a maximum value of g_{ds} at V_{DS} = 0 and decreases gradually with an increase in V_{DS}. The presence of SiGe in the channel region of the stacked channel FinFET increases the electron mobility, resulting in higher output transconductance in the TLSC and DLSC structures. This is because the electrons experience less resistance to their motion, and are able to

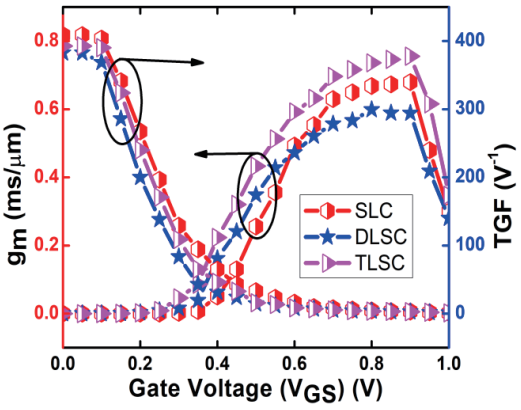

Fig. 9. (Color online) g_m and TGF comparison for SCL, DLSC and TLSC structures.

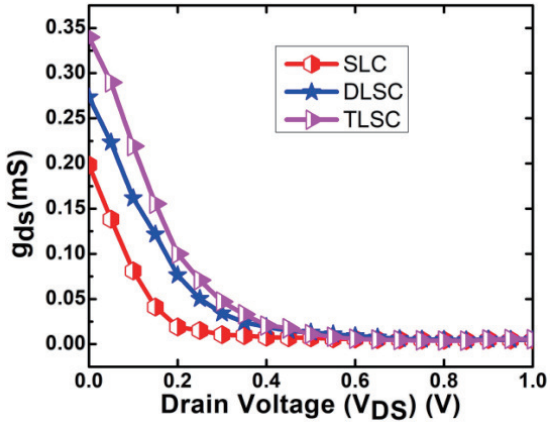

Fig. 10. (Color online) Output transconductance (g_{ds}) comparison for SLC, DLSC, TLSC with a change in drain voltage (V_{GS} = 0.6 V).

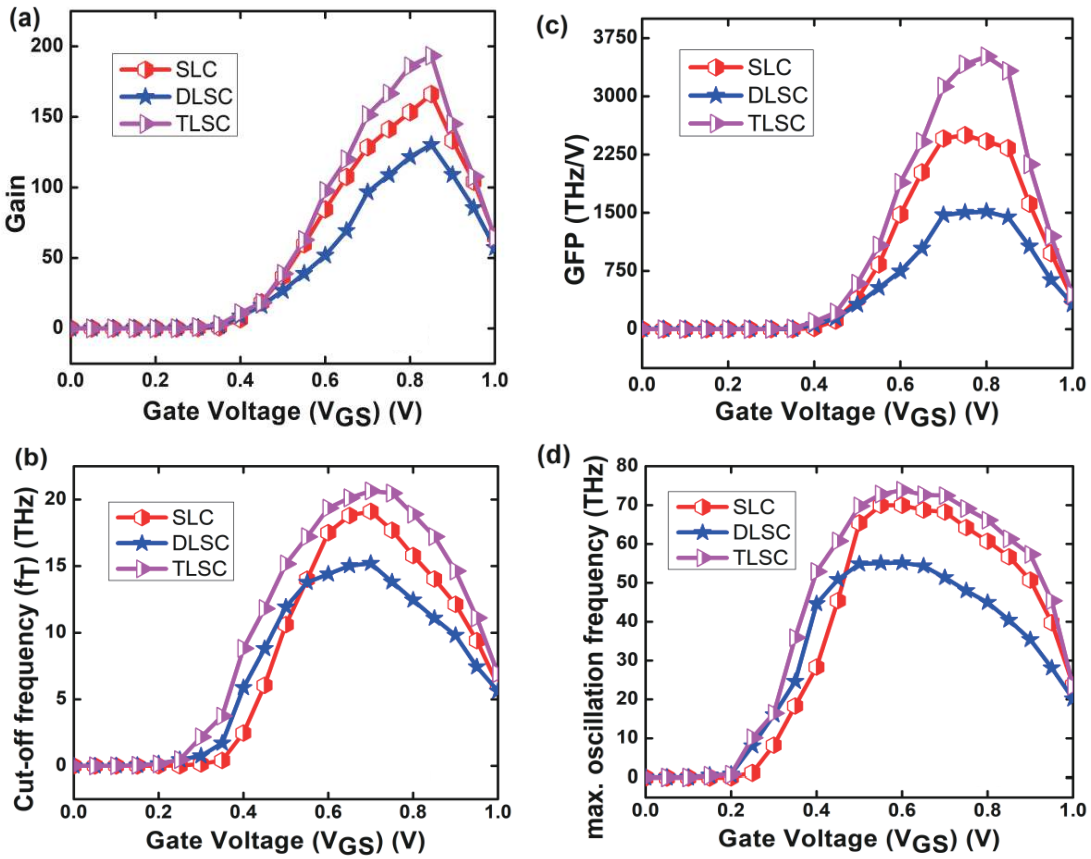

Fig. 11. (Color online) Variation of parameters in the three structures: (a) gain, (b) frequency, (c) GFP, and (d) maximum oscillation frequency.

flow more freely through the channel region. The output transconductance is obtained at a fixed gate voltage.

$$g_{ds} = \frac{\partial I_D}{\partial V_{DS}}. \tag{11}$$

The intrinsic gain (g_m/g_d) represents the amplification factor which should be high to enhance the analog performance. Eq. (12) represents the expression for intrinsic gain; it is the ratio of g_m and g_{ds}[26]. Fig. 11(a) shows variation of gain with gate voltage for the three types of channel structures. The peak value of gain is the highest for the TLSC structure because it has higher transconductance (g_m) than the other structures due to higher ON current. The DLSC structure has less gain than SLC due to less g_m. The gain value falls at a higher gate voltage, known as mobility degradation, due to the scattering of charge carriers.

$$\text{Intrinsic gain}\,(A_V) = \frac{g_m}{g_{ds}}. \tag{12}$$

The cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) are other crucial figure-of-merit characteristics for the high-frequency performance of transistors. The frequency at which short-circuit current gain becomes one is known as cut-off frequency (f_T) and it is the ratio of small signal output current to input current when the output is short-circuited. The expression of f_T is given in Eq. (13)[26], it shows that f_T is directly and inversely proportional to g_m and C_{gg}, respectively, which means the higher the g_m or lower the C_{gg},

Table 3. RF and analog parameter comparison of different structures at 20 nm gate length.

Parameter (Peak values)	TLSC (This work)	DLSC (This work)	SLC (This work)	Junctionless FinFET[27]	Junctionless verticle super-thin body FET[28]	Gaussian doped-junctionless FinFET[29]
g_m (mS)	0.75	0.58	0.67	0.062	0.067	0.25
TGF (V^{-1})	392.8	391.7	408.9	–	–	–
g_{ds} (mS)	0.339	0.273	0.198	–	–	–
f_T (THz)	20.5	15.2	19.11	0.140	0.285	9.13
f_{max} (THz)	73.82	69.93	55.16	–	–	–
Gain	193.36	130.26	166.23	–	–	–

the higher the cut-off frequency. The expression of the gain-frequency product (GFP) is given in Eq. (14)[26]. It is an essential parameter for high-frequency applications.

$$f_T = \frac{g_m}{2\pi C_{gg}}, \tag{13}$$

where C_{gg} is the total gate capacitance represented as the total of gate–source capacitance and gate–drain capacitance ($C_{gs} + C_{gd}$).

$$\text{GFP} = A_V \times f_T. \tag{14}$$

The frequency at which unilateral power gain equals unity is known as maximum oscillation frequency (f_{max}). Therefore, it is also known as the highest frequency at which a transistor can still provide power gain. It signifies the practical upper limit for the useful performance of a device. Higher f_{max} means that the device can produce oscillations at a higher frequency. The mathematical expression for f_{max} is given in Eq. (15)[27].

$$f_{max} = \frac{f_T}{\sqrt{4R_g(g_{ds} + 2\pi f_T C_{gd})}}, \tag{15}$$

where R_g is the series resistance, which is represented as (Eq. (16))[27]

$$R_g = \frac{1}{q\mu N_D^+}\frac{2L_{S/D}}{H_{Fin}W_{eff}}, \tag{16}$$

where q represents electron charge, μ is the career mobility, N_D^+ is the doping concentration, $L_{S/D}$ denotes the source/drain length, H_{Fin} is the Fin height and W_{eff} is the effective width, which is represented as $2H_{Fin} + T_{Fin}$.

The devices with $f_{max} > f_T$, provides power gain at frequencies of more than f_T and up to f_{max}, thus, these can be used as power amplifiers between frequency range f_T and f_{max}. The devices with $f_{max} > f_T$, can only achieve power gain up to f_{max} and cannot be utilized for the amplification of power between f_{max} and f_T[30].

The f_T variation with V_{GS} for the SLC, DLSC, and TLSC is shown in Fig. 11(b), indicating that the TLSC structure has high cut-off frequency than the other structures. Since the f_T depends directly on g_m; the TLSC structure provides more g_m, resulting in high f_T. The cut-off frequency in DLSC decreases at a higher gate voltage due to reduction in g_m, as shown in Fig. 9. Fig. 11(c) represents the variation of the GFP with V_{GS}; it depicts that GFP increases with an increase in the gate voltage and the TLSC structure has a maximum value of GFP due to high g_m and gain. The GFP attains its maximum value in the inversion region due to higher drain current and g_m. Fig. 11(d) represents the variation of f_{max} with gate voltage. The obtained curve is almost similar to the f_T–V_{GS} curve, except the frequency values are different. It represents that the TLSC structure has more maximum oscillation frequency, which means that it can provide more power gain than the other two structures. The comparative analysis of analog/RF parameters of the different structures is given in Table 3. It compares the analog parameters g_m, TGF, g_{ds}, f_T, f_{max} and gain of the TLSC, DLSC and SLC structures with the junctionless FinFET devices presented in the literature at 20 nm gate length.

5.3. Analysis of linear performance parameters

The analysis of linearity parameters for the stack-based channel is also done in this manuscript. The linear performance parameters deal with the non-linear distortion of the device that describes the non-linear relationship between input and output, resulting in mobility degradation that changes the transconductance performance. The major disturbances in the communication systems are higher-order transconductance parameters g_{m2} and g_{m3}, also known as harmonic distortions. The expressions for these are given in Eqs. (17) and (18); these are the second and third-order derivative of I_D with respect to V_{GS}, respectively[31].

$$g_{m2} = \frac{\partial^2 I_D}{\partial V_{GS}^2}, \tag{17}$$

$$g_{m3} = \frac{\partial^3 I_D}{\partial V_{GS}^3}. \tag{18}$$

The variation of g_{m2} and g_{m3} with V_{GS} is shown in Figs. 12(a) and 12(b). The lower peak value of g_{m2} and g_{m3} signifies that the device has better linearity or less distortions. Figs. 12(a) and 12(b) represent that the peak values of g_{m2} and g_{m3} for DLSC and TLSC structures are less than SLC, which means that DLSC and TLSC have fewer harmonic distortions than SLC, hence SiGe based hetero-structures improve the linearity of a device. This is because, higher drain current can reduce the variation of g_m by decreasing the impact of parasitic resistances. Additionally, at higher drain current, the channel becomes wider and electric field becomes more uniform. This uniform electric field leads to more uniform current density, resulting in a more linear transconductance. The values of g_{m2} and g_{m3} are high at lower gate voltage and it decreases with an increase in V_{GS}, because the g_m decreases at higher gate voltage due to higher drain current and consequently the magnitude of second and third-order harmonics decreases.

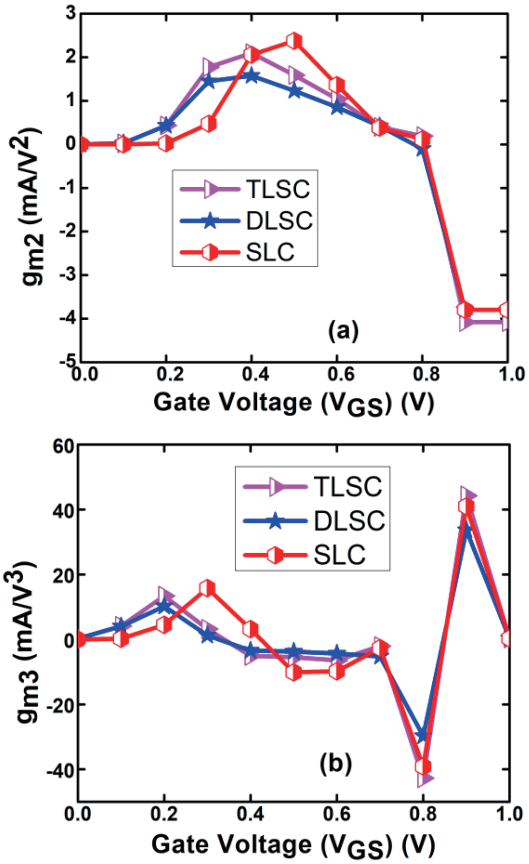

Fig. 12. (Color online) Variation of harmonic distortions (a) g_{m2} and (b) g_{m3} with V_{GS} for TLSC, DLSC and SLC structures.

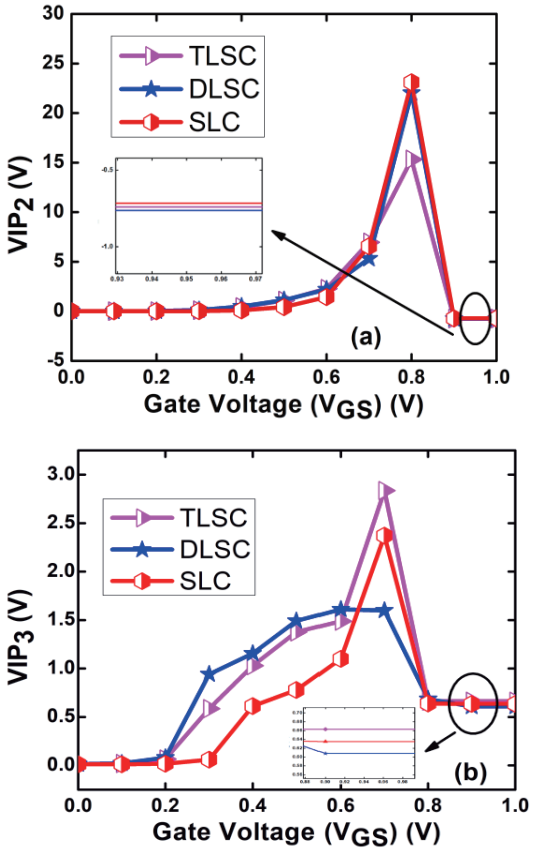

Fig. 13. (Color online) (a) Variation of VIP_2 with V_{GS}. (b) Variation of VIP_3 with V_{GS} for TLSC, DLSC and SLC.

Another parameter for linearity is the voltage intercept points (VIP_2 and VIP_3). The VIP_2 is the gate voltage representing the equal values of the fundamental harmonic and the second-order harmonic and VIP_3 is the gate voltage representing the same values of the fundamental and third-order harmonics. The expressions are given in Eqs. (19) and (20)[31]:

$$\mathrm{VIP}_2 = 4\frac{g_\mathrm{m}}{g_\mathrm{m2}}, \tag{19}$$

$$\mathrm{VIP}_3 = \sqrt{24\frac{g_\mathrm{m}}{g_\mathrm{m3}}}. \tag{20}$$

Figs. 13(a) and 13(b) illustrate the variation of VIP_2 and VIP_3 for the three structures with V_{GS}. The peak of VIP_2/VIP_3 signifies the improvement in linearity performance. Fig. 13(a) depicts that the SLC and DLSC have an almost the same peak value of VIP_2, which is more than the TLSC; Fig. 13(b) represents that TLSC has the highest value of VIP_3 and the value decreases for DLSC than SLC in the strong inversion region due to the channel asymmetry. The values of VIP_2 and VIP_3 increase at a lower gate bias and become constant for the three structures at the higher gate voltage after getting the maximum values. Fig. 13(b) also represents that TLSC shows better linear performance at third harmonic distortion (VIP_3) and DLSC, SLC shows better linearity at second harmonic distortion (VIP_2).

Another fundamental factor for linearity performance is the 1-dB compression point that determines the power level at input and output. It is the measure of the magnitude of the input power to fall the output power by 1-dB and the equation is given in Eq. (21)[31].

$$1\ \mathrm{dB\ compression\ point} = 0.22\sqrt{g_\mathrm{m}/g_\mathrm{m3}}. \tag{21}$$

It specifies the power level that results in 1-dB gain drop from a small signal value. The factor is vital for an amplifier as it provides a clear idea of the maximum power on which a device can operate at a fixed value of gain.

The peak transmitted power is kept below the 1-dB compression point to prevent inter-channel interference. Therefore, the high value of the point improves the linearity. Fig. 14 represents the comparison of peak values of 1-dB compression points for the three structures. It shows that the TLSC has the highest peak value of 1-dB compression point which means that it provides more linearity than the other structures. The value of the 1-dB compression point for the DLSC is less than the other two structures due to the lower drain current. There is a 52.8% increment in peak value for the SLC structure than the DLSC and a 21.4% increment for the TLSC than the SLC, as shown in Fig. 14.

6. Conclusion

A detailed study of the tri layer stack channel, double-layer stack channel and single layer channel is presented in this work. For the analysis, various parameters such as I_{ON}, I_{OFF}, I_{ON}/I_{OFF}, SS, DIBL, V_t are extracted using the VisualTCAD simulation. The result shows that the tri-layer stack channel has a high I_{ON} and V_t when compared with the other structures. The analog and RF parameters: g_m, g_{ds}, gain, TGF, f_T, GFP are also calculated for further study and it shows that

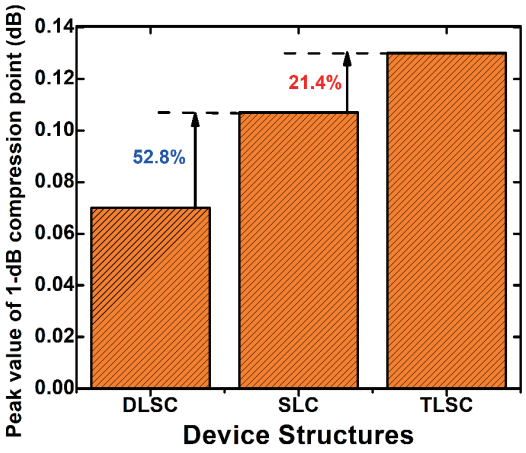

Fig. 14. (Color online) Comparison of peak values of 1-dB compression point for the three structures.

the tri layer stack channel (TLSC) is more suitable for analog applications due to its high g_m, gain, cut-off frequency and maximum oscillation frequency. The increase in peak value of g_m of TLSC is 11.9% to SLC and 29.3% to DLSC. In addition, compared to SLC and DLSC, in TLSC, the peak value of gain increases by 16.3% and 48.44%, respectively. The increase in peak value of the cut-off frequency of TLSC is 7.2% more than SLC and 34.8% more than DLSC. The linearity parameters for analysing the distortion are also discussed and the results represent that TLSC shows better linearity than the other structures due to improved transconductance.

Acknowledgement

The authors thank the Electronics and Communication Engineering Department, Malaviya National Institute of Technology, Jaipur, for providing essential support to carry out the research work.

References

[1] Hu C M. Device challenges and opportunities. Digest of Technical Papers, 2004 Symposium on VLSI Technology, 2004, 4
[2] Skotnicki T, Hutchby J A, King T J, et al. The end of CMOS scaling: Toward the introduction of new materials and structural changes to improve MOSFET performance. IEEE Circuits Devices Mag, 2005, 21, 16
[3] Bhattacharya D, Jha N K. FinFETs: From devices to architectures. Adv Electron, 2014, 2014, 1
[4] Bulusu A, Dasgupta S. Insights into channel potentials and electron quasi-Fermi potentials for DG tunnel FETs. J Semicond, 2015, 36, 014005
[5] Narendar V, Mishra R A. Analytical modeling and simulation of multigate FinFET devices and the impact of high-k dielectrics on short channel effects (SCEs). Superlattices Microstruct, 2015, 85, 357
[6] Yeh M S, Wu Y C, Hung M F, et al. Fabrication, characterization and simulation of Ω-gate twin poly-Si FinFET nonvolatile memory. Nanoscale Res Lett, 2013, 8, 331
[7] Leung G, Chui C O. Variability of inversion-mode and junctionless FinFETs due to line edge roughness. IEEE Electron Device Lett, 2011, 32, 1489
[8] Colinge J P, Lee C W, Afzalian A, et al. Nanowire transistors without junctions. Nature Nanotech, 2010, 5, 225
[9] Liu X, Wu M L, Jin X S, et al. The optimal design of 15 nm gate-length junctionless SOI FinFETs for reducing leakage current. Semicond Sci Technol, 2013, 28, 105013
[10] Chang W T, Lin Y S, Shih C T. Threshold voltage and transconductance shifting reliance on strained-SiGe channel dimension. Solid State Electron, 2015, 110, 10
[11] Das R, Goswami R, Baishya S. Tri-gate heterojunction SOI Ge-FinFETs. Superlattices Microstruct, 2016, 91, 51
[12] Kumar M J, Venkataraman V, Nawal S. Impact of strain or Ge content on the threshold voltage of nanoscale strained-Si/SiGe bulk MOSFETs. IEEE Trans Device Mater Reliab, 2007, 7, 181
[13] Singh T V, Jagadesh Kumar M. Effect of the Ge mole fraction on the formation of a conduction path in cylindrical strained-silicon-on-SiGe MOSFETs. Superlattices Microstruct, 2008, 44, 79
[14] Venkataraman V, Nawal S, Kumar M J. Compact analytical threshold-voltage model of nanoscale fully depleted strained-Si on silicon–germanium-on-insu lator (SGOI) MOSFETs. IEEE Trans Electron Devices, 2007, 54, 554
[15] Ding F, Wu Y T, Connelly D, et al. Simulation-based study of $Si/Si_{0.9}Ge_{0.1}/Si$ hetero-channel FinFET for enhanced performance in low-power applications. IEEE Electron Device Lett, 2019, 40, 363
[16] Jaisawal R K, Rathore S, Kondekar P N, et al. Assessing the analog/RF and linearity performances of FinFET using high threshold voltage techniques. Semicond Sci Technol, 2022, 37, 055010
[17] Ghosh D, Kranti Abhinav. Impact of channel doping and spacer architecture on analog/RF perfromance of lower power junctionless MOSFETs . Semicond Sci Technol, 2015, 30, 015002
[18] Genius C. A CMOS TCAD Simulation Tool, User's Guide.
[19] Rios R, Cappellani A, Armstrong M, et al. Comparison of junctionless and conventional trigate transistors with L_g down to 26 nm. IEEE Electron Device Lett, 2011, 32, 1170
[20] Colinge J P. FinFETs and other multi-gate transistors. Springer, 2008
[21] Badaroglu M. More Moore. 2021 IEEE International Roadmap for Devices and Systems Outbriefs, 2022, 1
[22] Rahimian M, Orouji A A, Aminbeidokhti A. A novel deep submicron SiGe-on-insulator (SGOI) MOSFET with modified channel band energy for electrical performance improvement. Curr Appl Phys, 2013, 13, 779
[23] Hu L D, Lou H J, Li W T, et al. Suppression of statistical variability in junctionless FinFET using accumulation-mode and charge plasma structure. IEEE Trans Electron Devices, 2021, 68, 399
[24] Seo J H, Yuan H, Kang I M. Design optimization of silicon-based junctionless fin-type field-effect transistors for low standby power technology. J Electr Eng Technol, 2013, 8, 1497
[25] Biswas K, Sarkar A, Sarkar C K. Linearity and analog performance analysis of silicon junctionless bulk FinFET considering gate electrode workfunction variability and different fin aspect ratio. Silicon, 2022, 14, 7531
[26] Srivastava N A, Priya A, Mishra R A. Analog and radio-frequency performance of nanoscale SOI MOSFET for RFIC based communication systems. Microelectron J, 2020, 98, 104731
[27] Jegadheesan V, Sivasankaran K. RF stability performance of SOI junctionless FinFET and impact of process variation. Microelectron J, 2017, 59, 15
[28] Barman K R, Baishya S. An insight into the DC and analog/RF response of a junctionless vertical super-thin body FET towards high-K gate dielectrics. Silicon, 2022, 14, 6113
[29] Manikandan S, Balamurugan N B. The improved RF/stability and linearity performance of the ultrathin-body Gaussian-doped junctionless FinFET. J Comput Electron, 2020, 19, 613
[30] Schwierz F, Liou J J. Semiconductor devices for RF applications: Evolution and current status. Microelectron Reliab, 2001, 41, 145
[31] Sarkar A, Kumar Das A, De S, et al. Effect of gate engineering in double-gate MOSFETs for analog/RF applications. Microelectron J, 2012, 43, 873

Devenderpal Singh completed M.Tech degree in VLSI Design and CAD from Thapar University, India in 2013. He has worked as a Research Associate at IIT Jodhpur and Assistant Professor at Chitkara University, Chandigarh, India, during 2014–2019. He is currently pursuing Ph.D in the Department of Electronics and Communication Engineering from Malaviya National Institute of Technology, Jaipur, India. His research interests include Microelectronic device modeling and simulation, SRAM design, Compute-In-Memory.

Shalini Chaudhary received M.Tech degree in VLSI designing from the Banasthali University, India. She is currently pursuing Ph.D degree in Department of Electronics and Communication Engineering from Malaviya National Institute of Technology, Jaipur, India. Her research interests include micro and nano-electronic device modeling and simulation.

Basudha Dewan received M.Tech degree in Electronics and Communication Engineering from Punjab Engineering College (PEC), Chandigarh, India, in 2018. She is currently pursuing Ph.D in the Department of Electronics and Communication Engineering from Malaviya National Institute of Technology, Jaipur, India. Her research intersets include modeling and simulation of advanced semiconductor devices, design and development of semiconducotr based hybrid sensor systems.

Menka Yadav has completed her B.E. from Government Engineering College Ajmer in 2006, M.Tech from MNIT Jaipur in 2008 and Ph.D from IIT Roorkee in 2016. She has worked at BML University Gurugram, NIT Tiruchirappalli before joining MNIT Jaipur in 2019. Her research interest is device design and modeling. Applications of emerging devices to digital, analog and sensor domain, Solar cell etc.