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Study of the influence of virtual guard ring width on the performance of SPAD detectors in 180 nm standard CMOS technology

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Abstract: The influence of the virtual guard ring width (GRW) on the performance of the p-well/deep n-well single-photon avalanche diode (SPAD) in a 180 nm standard CMOS process was investigated. TCAD simulation demonstrates that the electric field strength and current density in the guard ring are obviously enhanced when GRW is decreased to 1 μm. It is experimentally found that, compared with an SPAD with GRW = 2 μm, the dark count rate (DCR) and afterpulsing probability (AP) of the SPAD with GRW = 1 μm is significantly increased by 2.7 times and twofold, respectively, meanwhile, its photon detection probability (PDP) is saturated and hard to be promoted at over 2 V excess bias voltage. Although the fill factor (FF) can be enlarged by reducing GRW, the dark noise of devices is negatively affected due to the enhanced trap-assisted tunneling (TAT) effect in the 1 μm guard ring region. By comparison, the SPAD with GRW = 2 μm can achieve a better trade-off between the FF and noise performance. Our study provides a design guideline for guard rings to realize a low-noise SPAD for large-array applications.

Key words: single-photon avalanche diode (SPAD); virtual guard ring; dark count rate (DCR); photon detection probability (PDP); afterpulsing probability (AP)

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1. Introduction

Single-photon avalanche diodes (SPADs) operating in Geiger mode are high-sensitivity, low-noise semiconductor devices that can detect weak light using avalanche pulses. Si-SPADs fabricated in a deep-submicron (DSM) CMOS process have the characteristics of low dark count rate, high photon-detection probability, and weak afterpulsing effect, and can also be integrated with back-end readout and signal processing circuits at a low cost, leading to wide applications such as light detection and ranging (LiDAR), fluorescence lifetime imaging microscopy, and 3-D vision[1−3].

The research on silicon-based SPADs has developed toward high photon detection probability (PDP) and fill factor (FF). Many groups have focused on the design of the avalanche regions and guard rings to guarantee an excellent PDP and a high FF. In recent years, a variety of SPADs have been proposed based on p+/n-well, p+/deep n-well (DNW), p-well/DNW, etc. junctions[4−6]. The progressively thicker depletion layer helps enhance the spectral response and increases the quantum efficiency[7], thereby enhancing PDP. Whereas, it means that higher operating voltages desired can easily lead to the breakdown of the edge electric field and the disability of SPADs.

To enable the proper operation of SPADs, the guard ring structure becomes critical. As the technology nodes shrink, diverse layers and doping profiles are available to form the guard rings, such as a diffusion guard ring, a low-doped guard ring, and a virtual guard ring. Traditional low-doped p-well guard rings in a p+/DNW SPAD are successful at preventing premature edge breakdown (PEB)[8]. The p-well guard ring needs to remain away from the cathode, so it is difficult to scale down the pixel pitch[9]. In Ref. [10], an approach of using the retrograde deep n-well as a virtual guard ring has been presented, which can lower the doping concentration in the periphery of the avalanche area to avoid edge breakdown. The pixel pitch can be scaled down through it, benefiting the improvement of FF.

Additional care needs to be taken with the virtual guard ring width (GRW). If the virtual GRW is too small, a high electric field will be laid in the guard ring area, which leads to a significant electric field-related tunneling effect. In particular, lots of traps near the shallow trench isolation (STI) interface[11] drift into the high-field region to activate the SPADs by mistake, resulting in a high dark count rate and the performance degradation of the SPADs. In contrast, if the GRW is too large, it will increase the pixel pitch and decrease the integration of the detector array. Therefore, the virtual GRW should be chosen properly so as to balance SPAD performance and the FF.

To obtain the most appropriate GRW, the p-well/DNW SPADs with GRW = 1, 2, and 3 μm were designed and fabricated in SMIC 180 nm standard CMOS technology. The impact of GRW on the physic characteristics of the SPAD devices was revealed by TCAD simulation and the various fea-

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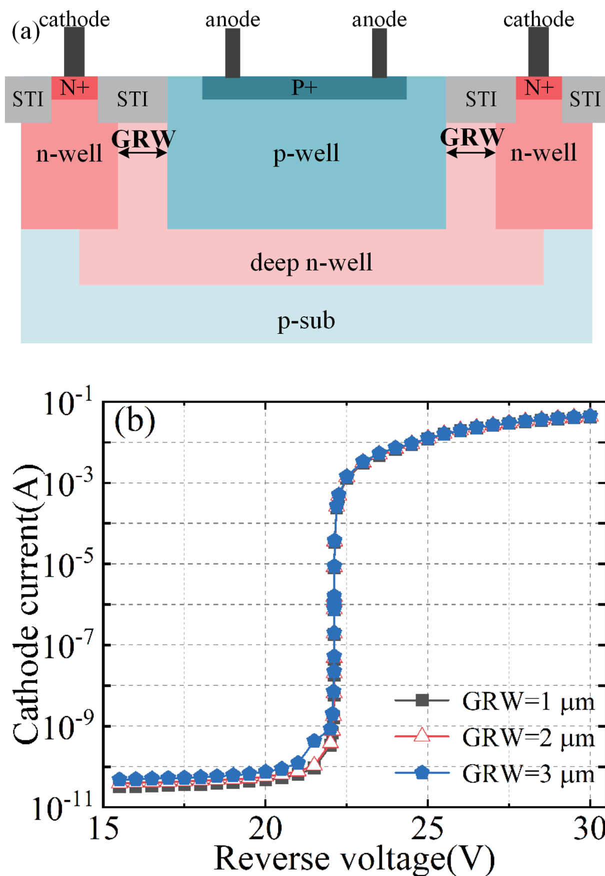

Fig. 1. (Color online) (a) Schematic cross-section of the p-well/deep n-well SPAD. (b) TCAD simulation of the reverse *I*–*V* characteristics.

tures such as photon detection probability, dark count rate, and afterpulsing probability were characterized by experimental results.

2. SPAD structure and simulation

The cross-section of the proposed SPAD structure is illustrated in Fig. 1(a). The active area is constructed by the p-well in conjunction with the deep n-well, forming a wide depletion region that can increase quantum efficiency and thus enhance the spectral response[12]. The p-well is surrounded by the n-well and a certain distance is set aside between the n-well and p-well, that is, the GRW. A virtual DNW guard ring width with the retrograde doping profile helps to lower the doping concentration and the electric field at the edge of the avalanche area and prevents PEB.

The proposed SPAD devices with GRW = 1, 2, and 3 μm, respectively, were simulated by Silvaco TCAD based on a 180 nm standard CMOS technology, to study the impact of GRW on SPAD performance and FF. The electrical reverse *I*–*V* characteristic is shown in Fig. 1(b). It is seen that all three SPADs can operate in Geiger mode with a similar breakdown voltage (V_{BD}) of ~22.4 V, meaning that PEB does not occur on the edges of the devices.

Fig. 2 illustrates the 2D electric field distributions with different GRW at an excess bias voltage of 4 V. The difference between them in the avalanche multiplication region and guard ring merits close attention. Firstly, the center of the multiplication zone of three SPADs is laid at Y = 1.3 μm and the peak high electric field (red) is uniformly distributed around it, all of which are 4.98 × 10^5 V/cm, so the GRW has little effect on the avalanche multiplication region. Another, it is also found that there is a high electric field region (yellow) located in the SPAD with GRW = 1 μm. However, the electric field strength in the same regions of the SPADs with GRW = 2 and 3 μm is relatively low (blue-green).

Further, the electric field strength of the guard ring is intercepted at Y = 0.52 μm and the electric field strength in the 1 μm-GRW SPAD reaches 3.5 × 10^5 V/cm, while the 2 and 3-μm GRW devices are almost identical at 2.9 × 10^5 V/cm, as shown in Fig. 3(a).

It is known that the defects introduced at the Si-SiO_2 interface easily lead to a surge in the carrier generation and recombination in the guard ring area near the STI. The defect-induced carriers are driven into the center of the multiplication zone by the high electric field and then could trigger the avalanche events, whose drift path is indicated in Fig. 3(b). In Fig. 3(c), we note that the total current density extracted at the 1 μm-GRW guard ring is about 1 × 10^5 A/cm^2, higher than two others ~8.3 × 10^4 A/cm^2. By comparison in Fig. 3(c), the electric field strength and total current density in the guard ring will decline and remain unchanged when the GRW is increased to 2 and 3 μm.

Nevertheless, the increase in the GRW will cause a decrease in FF. Photon detection efficiency (PDE) is the product of the FF and photon detection probability (PDP), which might be reduced by the increasing guard ring width. Because SPAD performance is no longer affected when GRW is larger than 2 μm, the subsequent experiments on PDP, DCR, and AP are only conducted on SPADs with GRW = 1 and 2 μm.

3. Experimental results and discussion

To study the impact of GRW on the photoelectric properties in detail, two SPADs with GRW = 1 and 2 μm were fabricated in SMIC 180 nm standard CMOS process. The micrographs of the two octagonal devices are shown in Fig. 4. Both SPADs have the same 7-μm active diameter and the difference is only the width of the virtual guard ring.

3.1. Experimental setup

The experimental setup for photon counting is shown in Fig. 5(a). The DCR measurement is conducted in the absence of any incident photons. The anode of the SPADs is connected to a field-programmable gate array (FPGA) to record the dark count pulses. To measure the PDP, the light from lasers with a wavelength range of 405—940 nm is projected into an integrating sphere with a probe of the optical power meter at one port of the sphere and the SPAD at the other. The amount of incident photons is calibrated by the optical power meter to make sure that SPAD operates in a single-photon state. Stacking effects can be suppressed so as not to impede the accurate calculation of PDP.

3.2. *I*–*V* characteristics

The reverse *I*–*V* characteristics were measured using a Keithley 4200A-SCS semiconductor parameter analyzer, which exhibits a V_{BD} of ~22.4 V, matching well with the TCAD simulation results in Fig. 1(b). A steeper curve indicates that the dark current of the SPAD with GRW = 1 μm could reach 100 μA faster than the 2 μm-GRW SPAD. There might be two

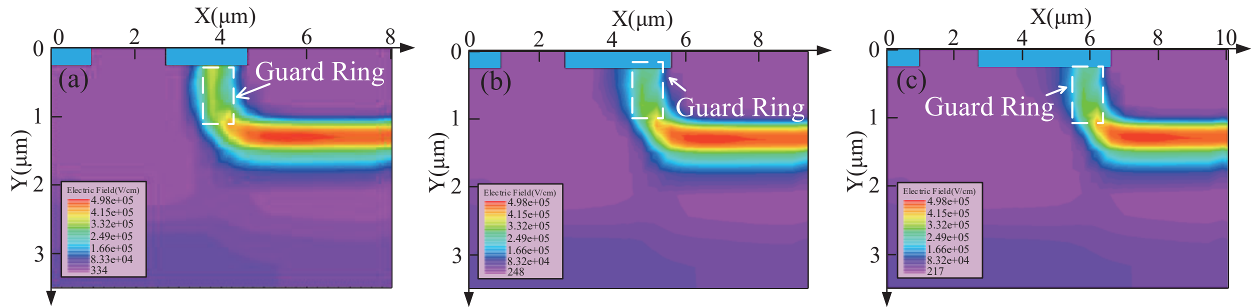

Fig. 2. (Color online) TCAD simulation of the electric field for devices with guard ring width (a–c) GRW = 1, 2, 3 μm.

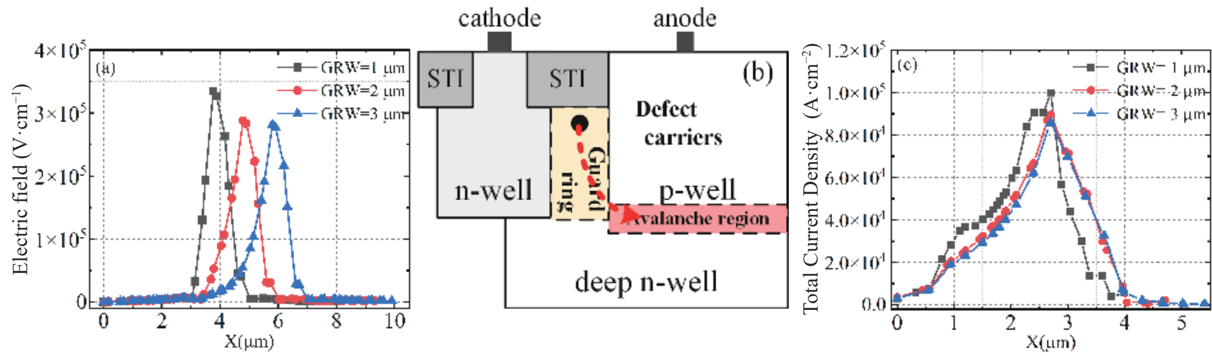

Fig. 3. (Color online) (a) TCAD simulation of electric field strength extracted at Y = 0.52 μm. (b) Drift path of minority electrons in the guard ring. (c) TCAD simulation of total current density extracted at Y = 0.52 μm.

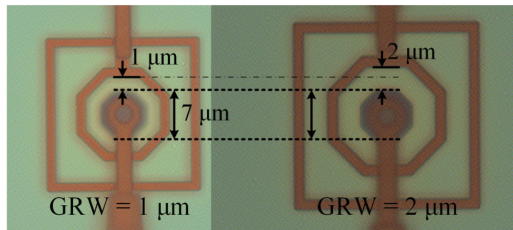

Fig. 4. (Color online) Micrograph of SPADs with GRW = 1 and 2 μm fabricated in a 180 nm standard CMOS technology.

potential reasons for this. A good deal of unwanted avalanche events caused by carriers flowing through the guard ring region accelerate the rise of the dark current. On the other hand, the distance between the cathode and anode is shortened, resulting in a shortened current path and a reduced on-resistance[13].

3.3. Dark count rate (DCR)

There are three main mechanisms for dark count generation in deep-submicron CMOS technology: thermal generation (SRH), trap-assisted tunneling (TAT), and band-to-band tunneling (BTBT). The total dark count is the sum of three mechanisms:

$$\mathrm{DCR} = \mathrm{DCR_{SRH}} + \mathrm{DCR_{TAT}} + \mathrm{DCR_{BTBT}}. \qquad (1)$$

The thermally generated non-equilibrium carriers transition principally through the defect centers in the bandgap for bulk silicon, so the SRH generation rate is mainly determined by the temperature and defect concentration[14]. The TAT mechanism is not only associated with the defect concentration but also enhanced by the electric field[15]. Besides, as the electric field strength increases to 7 × 10^5 V/cm, BTBT becomes the most important source of DCR generation[16]. SPADs fabricated with process modification have the ability to improve the defect concentration and electric field of the avalanche area[17], for instance, double-diffused source/drain implantation and hydrogen annealing in CMOS image sensor (CIS) technology lead to a reduction in defect-related dark counts. However, devices manufactured in DSM standard CMOS process are still plagued by defects.

The tested DCR of two SPADs as a function of excess bias voltage (V_{ex}) at room temperature is shown in Fig. 6(a). The measured results demonstrate ~48.9 kHz when GRW = 1 μm and ~17.7 kHz when GRW = 2 μm at V_{ex} of 3 V. It is found that the variation of GRW from 1 to 2 μm leads to a more than twofold decrease in DCR.

The dependence of DCR on temperatures at V_{ex} = 2 V is exhibited in Fig. 6(b). DCR rises linearly with the increase in temperature. The inset of Fig. 6(b) shows the Arrhenius-type relationship between DCR and temperatures, which can be expressed by[17]:

$$\mathrm{DCR} \propto T^2 \exp\left(-\frac{E_a}{kT}\right). \qquad (2)$$

Here E_a is the activation energy, T is the operating temperature and k is Boltzmann's constant.

The activation energy E_a of DCR is a good indicator of the main DCR generation mechanisms[18]. When GRW = 2 μm, the extracted E_a is about 0.747 eV, suggesting that the dark count noise mainly comes from the thermal generation at an excess bias of 2 V. However, the SPAD with GRW = 1 μm shows a reduced activation energy of 0.596 eV, which is due to the enhanced TAT effect[19]. With the aid of the TCAD simulation, the electric field strength in the avalanche area is much less than 7 × 10^5 V/cm at V_{ex} = 2 V, indicating a weak influence of BTBT. Therefore, the carrier generation from the

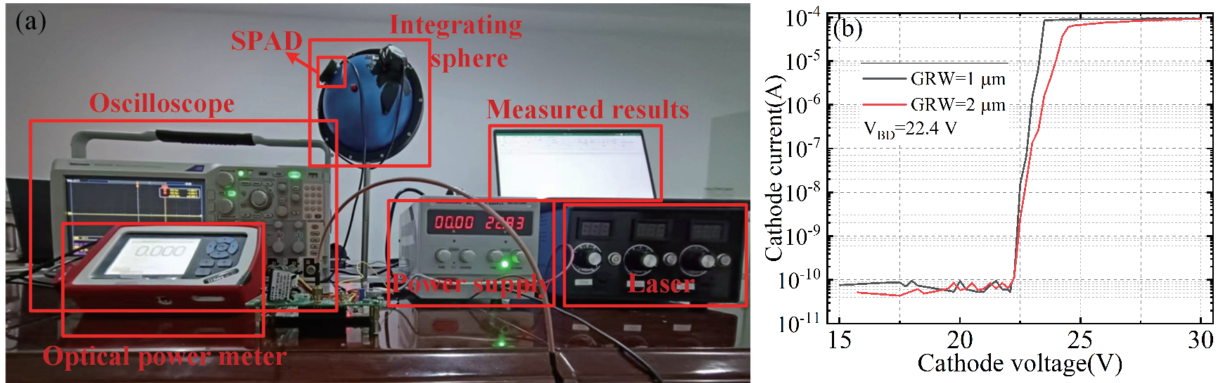

Fig. 5. (Color online) (a) Experimental setup for photon counting. (b) Measured reverse *I*–*V* characteristics of SPADs with two guard ring widths.

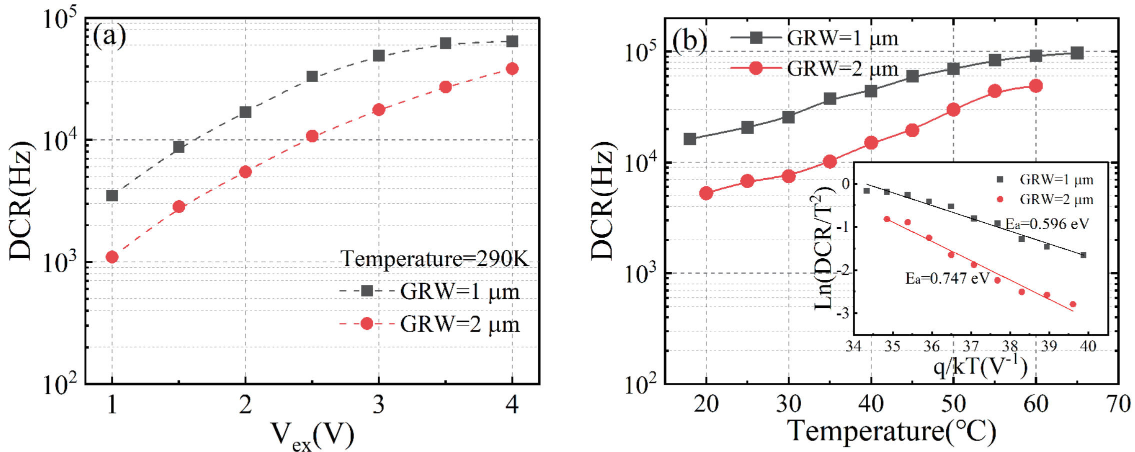

Fig. 6. (Color online) Variations of DCR (a) with V_{ex} at room temperature (T = 290 K) and (b) with the temperature at the excess bias of 2 V.

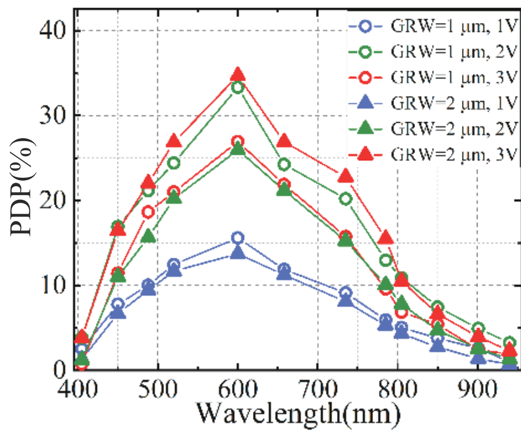

Fig. 7. (Color online) Measured PDP of SPADs at different excess bias voltages.

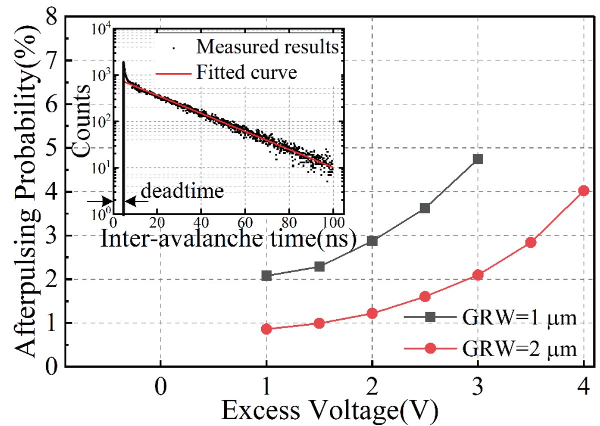

Fig. 8. (Color online) Measured AP of SPADs at different excess bias voltages.

TAT becomes the main source of dark counts. The STI guard ring introduces a large number of defect carriers on the surface, which would be driven by the electric field of the virtual guard ring region in the SPAD, triggering avalanche breakdowns and resulting in a DCR higher in the SPAD with GRW = 1 μm.

3.4. Photon detection probability (PDP)

PDP measurement results for two SPADs at different V_{ex} of 1–3 V are displayed in Fig. 7. As V_{ex} rises to 2 V, there is a remarkable increase in PDP contributed by the multiplication region due to the improved breakdown probability and quantum efficiency[20]. Moreover, a high field is located in the guard ring so that the photo-generated carriers absorbed in this region will also be accelerated and ionized, resulting in a higher PDP for GRW = 1 μm than that for GRW = 2 μm. At V_{ex} = 3 V, the SPAD with GRW = 2 μm has a peak PDP of 35% (600 nm) and maintains >4% at 901 nm. Conversely, the PDP of another one decreases instead of increasing. The simulated electric field distribution and tested DCR of 1 μm-SPAD raise our speculation: since more interface states are allowed to drift into the multiplication zone with the help of a higher electric field in the guard ring, this may lead to a larger non-ideal avalanche pulse generation rate and result in higher DCR, reaching 48.9 kHz. The avalanche pulses caused by the

incident photons overlap with the wrong pulses generated by the dark noise and cannot be distinguished. As a result, its PDP-reached saturation and could not be further improved.

3.5. Afterpulsing probability (AP)

The release of trapped carriers caused by defect levels contributes to an afterpulse. A passive quenching circuit was constructed with a 50-kΩ resistor and the dead time could be set to 6 ns. To avoid the inaccuracy of afterpulsing probability, the intervals of millions of dark counts need to be recorded to form histograms for statistical calculations[21]. An exponential fit is made to the counts' distribution, and the part above the fitted curve is contributed by the afterpulses, as shown in the inset of Fig. 8. Then the AP is calculated by dividing the afterpulses by the total counts. Fig. 8 demonstrates that at V_{ex} = 3 V, the AP is 4.7% for GRW = 1 μm and only 2% for GRW = 2 μm. The AP measurement results are consistent with DCR. The DCR increases rapidly with V_{ex} when GRW = 1 μm, therefore more carriers are trapped in the deep-level trap, being released to form the secondary dark count after a while.

4. Conclusions

The influence of the virtual guard ring width (GRW) on the characteristics of the PW/DNW junction SPAD was investigated based on SMIC 180 nm standard CMOS technology. TCAD simulation reveals that the electric field in the guard ring region is significantly increased when the GRW is reduced from 2 to 1 μm. The experimental results further indicate that the characteristics of the DCR and AP are seriously degraded when the GRW is scaled down to 1 μm, which may be attributed to the enhanced TAT effect in the narrower guard ring. When the GRW = 2 μm is selected, the SPAD can obtain the optimal performance with a high PDP of about 4% at 901 nm and a low DCR. The proposed virtual guard ring design method can be applied in low-noise SPAD arrays in near-infrared imaging applications.

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