# Development of a simple two-step lithography fabrication process for resonant tunneling diode using air-bridge technology

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**Abstract:** This article reports on the development of a simple two-step lithography process for double barrier quantum well (DBQW) InGaAs/AlAs resonant tunneling diode (RTD) on a semi-insulating indium phosphide (InP) substrate using an air-bridge technology. This approach minimizes processing steps, and therefore the processing time as well as the required resources. It is particularly suited for material qualification of new epitaxial layer designs. A DC performance comparison between the proposed process and the conventional process shows approximately the same results. We expect that this novel technique will aid in the recent and continuing rapid advances in RTD technology.

Key words: air-bridge; indium phosphide; microfabrication; resonant tunneling diode

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## 1. Introduction

Resonant tunneling diodes (RTDs) have received a lot of attention due to their structural simplicity, ultra-high freguency capability, low power consumption, and their ability to operate at room temperature<sup>[1-6]</sup>. They are widely applied in micro/nanoelectronics and communications (oscillators, logic circuits, transmitter, wireless link), optoelectronics (phototransistor, photodetector, light emitting diode, optical modulator, single photon detector), and recently in neuromorphic applications<sup>[7–21]</sup>. RTDs typically consist of a quantum well sandwiched in between two barriers and work on the principle of quantum tunneling effect. Negative differential resistance (NDR), which is a unique characteristic of this semiconductor device, allows them to be applicable in a wide range of areas (as mentioned above). Research on RTDs commenced with the start of the theoretical studies on tunneling phenomenon in a superlattice by Leo Tsu and Raphael Esaki in the 1970s and along with Chang in 1974<sup>[22-24]</sup>. These RTDs were experimentally demonstrated for the first time in 1974 at liquid nitrogen temperature, where the NDR region was observed in the current voltage (I-V) characteristics; however, the first room temperature experiment was only conducted in 1985<sup>[24, 25]</sup>.

The conventional fabrication process for RTDs requires six lithography steps and mainly employs the polyimide process<sup>[26, 27]</sup> for passivation. The first step here is the deposition of top metal contact, followed by the top mesa step (where etching is conducted until the emitter layer). The bottom mesa step, which etches till the substrate, is followed by the

Correspondence to: S Samanta, swagata.s@srmap.edu.in Received 9 APRIL 2023; Revised 21 MAY 2023. ©2023 Chinese Institute of Electronics formation of a bottom metal contact. A polyimide is used in the passivation step. The use of a polyimide passivation layer is essential to protect the device from external contaminants and to prevent unwanted surface recombination effects that can degrade the device performance at the cost introducing parasitic capacitance, which is crucial for high frequency applications. Finally, via-opening and metal bond pads deposition completes the fabrication process. Opening of the top contact (i.e., via-opening) after passivation is a critical step in enabling an electrical connection between top contact and bond pad, and is a challenging step, especially while fabricating the nanoscale dimension RTDs. The air-bridge approach overcomes the critical top-contact connection step of the conventional processes, where a suspended air-bridge structure is made that connects the top metal and the bond pad. Although similar fabrication approaches have been reported in the literature<sup>[28-32]</sup>, they all require at least four lithography steps.

In this work, we report details of the process and compare the DC performance of a 4 × 4  $\mu$ m<sup>2</sup> DBQW RTD using the proposed air-bridge technique with that from similarly sized devices made from the same epitaxial wafers but fabricated using the conventional polyimide process. DC characterization shows that both these processes have nearly the same performance.

This paper is organized as follows: Section 2 describes the RTD device epi-structure and fabrication details. Section 3 deals with the device characterization, while concluding remarks and future perspectives are discussed in Section 4.

## 2. Device structure and fabrication

The epi-structure of the RTD device used in this work was grown by MBE (molecular beam epitaxy) on a semi-insulating (SI) indium phosphide (InP) substrate. This structure,



Fig. 1. InGaAs/AIAs RTD epistructure.



Fig. 2. Cross-section of the designed RTD device.

shown in Fig. 1, consists of a 4.5 nm indium gallium arsenide (In<sub>0.53</sub>Ga<sub>0.47</sub>As) quantum well that is sandwiched in between 1.4 nm AlAs barriers; the barriers being surrounded by undoped and lightly doped In<sub>0.53</sub>Ga<sub>0.47</sub>As spacer layers (In<sub>0.53</sub>Ga<sub>0.47</sub>As) on both sides. The collector and emitter layers are made of heavily doped In<sub>0.53</sub>Ga<sub>0.47</sub>As material doped with silicon. The devices were fabricated by both photolithography and electron beam lithography. Only two lithography steps were required. Fig. 2 shows the cross section of the device. The emitter and collector contact pads were patterned by using electron beam lithography. The metal pattern was then used as a mask for an orthophosphoric based chemical wet etch to the emitter (bottom) contact layer. Next, the collector pad and RTD were protected with photoresist by using photolithography, followed by a final chemical wet etching step to the substrate. Fig. 3 illustrates the process steps, while Fig. 4 shows the scanning electron microscopic view of the fabricated RTD device showing the airbridge, which is 5  $\mu$ m wide and 55  $\mu$ m long.

## 3. Device characterization

Performance analysis for the fabricated RTD device is done by DC characteristics measurement. The setup is shown in Fig. 5. A semiconductor device parameter analyzer (Keysight B1500A) was used for DC characterization of the device. The bond pads ( $60 \times 100 \,\mu$ m<sup>2</sup>) are connected to the terminals on the parameter analyzer through two DC probes. The measured *I–V* characteristic of the 4 × 4  $\mu$ m<sup>2</sup> RTD at room temperature is shown in Fig. 6(a). The device exhibits a peak-to-valley current ratio of 3 and peak current density of 143 kA/cm<sup>2</sup>. The detailed results, including the comparison with conventionally fabricated devices are shown in Table 1



Fig. 3. Fabrication process flow (a) emitter and collector contact patterning by using electron beam lithography, (b) wet etch to bottom contact layer, (c) air-bridge patterning by using photolithography, (d) wet etch to substrate (due to anisotropic etching, air-bridge is formed) and stripping-off etching mask S1818.



Fig. 4. Scanning electron microscopic view of the fabricated RTD device with air-bridge.

and Fig. 6. It can be seen that both processes have nearly the same performance. Thus, the proposed simple RTD fabrication process is robust and has comparable performance with the conventional polyimide process.

The performance of  $4 \times 4 \mu m^2$  RTD device (fabricated by our proposed air-bridge process) is also compared with the available literature (based on air-bridge work) and the results are given in Table 2. It should be noted that the comparison here is made with the available work where the clear fabrication steps of RTD device and results are described.

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Fig. 5. (Color online) DC measurement setup for characterizing the fabricated RTD.



Fig. 6. Room temperature current–voltage characteristics of  $4 \times 4 \mu m^2$ RTD device using (a) proposed air-bridge process, (b) polyimide process.

#### 4. Conclusions and future perspectives

Double barrier quantum well resonant tunneling diode of active device area  $4 \times 4 \mu m^2$  based on the InGaAs/AIAs system is developed using a novel air-bridge process. Current–voltage characteristics at room temperature for this device results in a peak-to-valley current ratio of 3.02 and a peak current density of 143.46 kA/cm<sup>2</sup>. The measured results nearly match with the polyimide process with similar device dimension. This novel fabrication process may be extended to other material systems.

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Table 1. Comparison of DC characteristics for a  $4 \times 4 \ \mu m^2$  RTD fabricated using the air-bridge and polyimide processes.

Parameter	Polyimide process	Proposed air-bridge process
Peak current, I <sub>p</sub> (mA)	22.2	23
Valley current, <i>I</i> <sub>v</sub> (mA)	6.2	7.6
Peak-valley current difference, $\Delta I$ (mA)	16.1	15.4
Peak voltage, V <sub>p</sub> (V)	0.97	0.96
Valley voltage, $V_{\rm v}$ (V)	1.62	1.26
Peak-valley voltage difference, $\Delta V$ (V)	0.65	0.3
Peak-to-valley current ratio, PVCR	3.6	3
Peak current density, J <sub>p</sub> (kA/cm <sup>2</sup> )	139	143

Table 2. Performance comparison of InGaAs/AIAs RTD device fabricated by air-bridge process found in the literature and in our proposed method.

Parameter							
Active device area (µm²)	DBQW		21/62		-Ref.		
	t <sub>barrier</sub> (nm)	t <sub>well</sub> (nm)	t <sub>barrier</sub> (nm)	PVCR	J <sub>p</sub> (kA/cm²)		
4 × 4	1.3	4.5	1.3	3.2	260	[29]	
3 × 3	1.2	4.5	1.2	8.35	40.9	[ <mark>30</mark> ]	
8×8	3.0	5.1	2.8	8.6	24.6	[31]	
176	2.0	4.0	2.0	43	24	[32]	
$4 \times 4$	-	-	-	1.2	250	[ <mark>28</mark> ]	
4×4	1.4	4.5	1.4	3	143	This work	

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