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Study of enhancement-mode GaN pFET with H plasma treated gate recess

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Abstract: This letter showcases the successful fabrication of an enhancement-mode (E-mode) buried p-channel GaN field-effect-transistor on a standard p-GaN/AlGaN/GaN-on-Si power HEMT substrate. The transistor exhibits a threshold voltage (V_{TH}) of −3.8 V, a maximum ON-state current (I_{ON}) of 1.12 mA/mm, and an impressive I_{ON}/I_{OFF} ratio of 10^7. To achieve these remarkable results, an H plasma treatment was strategically applied to the gated p-GaN region, where a relatively thick GaN layer (i.e., 70 nm) was kept intact without aggressive gate recess. Through this treatment, the top portion of the GaN layer was converted to be hole-free, leaving only the bottom portion p-type and spatially separated from the etched GaN surface and gate-oxide/GaN interface. This approach allows for E-mode operation while retaining high-quality p-channel characteristics.

Key words: GaN pFET; E-mode; H plasma treatment; I_{ON}/I_{OFF} ratio

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1. Introduction

The development of third-generation wide bandgap semiconductor materials and devices has facilitated the improvement of the overall performance of power integrated circuits. Due to the superior properties of GaN and AlGaN/GaN heterostructure, AlGaN/GaN high electron mobility transistors (HEMTs) have been widely used as the main switching devices in various high-frequency and high-efficiency power devices. To fully exploit the performance advantages of GaN power integrated circuits, it is necessary to increase the degree of integration between switching devices, control circuits, and passive devices as much as possible. Since traditional GaN HEMTs are mainly n-channel devices, most GaN-based integrated circuits adopt n-type metal oxide semiconductor (NMOS) logic. However, compared with complementary metal oxide semiconductor (CMOS) logic, NMOS logic still has some power consumption losses. Therefore, to further improve the overall performance of full GaN integrated circuits, besides improving the process and circuit topology, another direct method is to adopt CMOS logic. However, the performance of GaN p-channel FETs differs significantly from that of n-channel HEMTs and it is difficult to match the two. Directly adopting CMOS logic would lower the performance of the entire circuit. Therefore, improving the GaN p-channel FET device structure and process level is an important part of promoting the advance of GaN CMOS technology.

Several recent studies have shown that Ⅲ-nitride heterostructures can generate two-dimensional hole gases (2DHG) through spontaneous and piezoelectric polarization effects. Examples include InGaN/GaN[1], GaN/AlInGaN[2], p-GaN/AlGaN[3], and GaN/AlN[4]. Among them, the p-GaN/AlGaN/GaN epitaxial structure is compatible with HEMT technology and is very suitable for single-chip integration of GaN n-channel and p-channel devices. This is also the reason why this epitaxial structure was selected for the present study.

In depletion-mode GaN p-channel devices, a certain amount of current still flows through the channel when the gate-source voltage (V_{GS}) is 0 V. To turn off the device, a positive bias needs to be applied to deplete the 2D hole gas (2DHG) under the gate, which increases the complexity of the circuit design and significantly increases power consumption in practical applications. Therefore, developing enhancement-mode GaN p-channel devices is crucial to promote their applications in power electronics. Currently, the most common method to achieve enhancement-mode is to use inductively coupled plasma (ICP) dry etching to create a gate trench, which reduces the carrier concentration in the channel underneath the gate and cuts off the 2DHG channel. However, the ion bombardment during the dry etching process may damage the p-GaN layer and the channel, leading to issues such as low saturation current density, high off-state leakage, and poor reliability of the device[5–8].

In 2016, Hao *et al*.[9, 10] proposed using hydrogen plasma treatment to transform p-GaN into high-resistance GaN (HR-GaN) based on the compensation mechanism of holes. This approach has been shown to be effective in avoiding the introduction of defects in the active region of the device that could degrade its performance, unlike ICP dry etching. This technique has now been applied to the fabrication of high-

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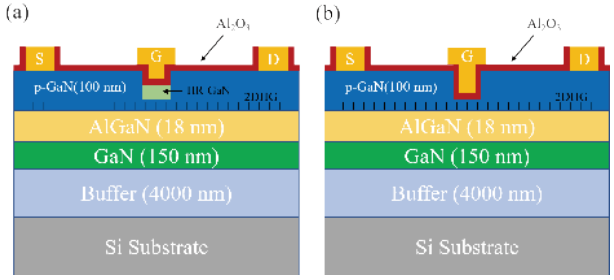

Fig. 1. (Color online) Schematic of pFETs on the p-GaN gate power HEMT platform. (a) Device A; (b) device B.

performance enhanced p-GaN gate HEMTs[11, 12] and diodes[13–15].

This study proposes a novel approach to process the gate-underneath region of GaN-based devices. Specifically, a relatively shallow ICP dry etching is performed on the gate-underneath region, followed by H plasma treatment of the bottom of the etched groove. The H plasma treatment converts a certain thickness of p-GaN at the bottom of the groove into HR-GaN without hole carriers, while preserving a certain thickness of p-GaN as the channel. This achieves the enhancement mode under zero bias, while also isolating the etched surface from the channel. The resulting devices exhibit low off-state leakage current, high saturation current density, and a switch ratio of up to 10^7. Compared to conventional methods, this approach avoids introducing defects in the active region of the device and offers superior performance.

2. Device fabrication

A cross-sectional schematic of the fabricated devices is shown in Fig. 1. Both device A and device B are grown on an 8-inch Si(111) substrate by metalorganic chemical vapor deposition (MOCVD). The epitaxial structure from bottom to top consists of Si(111) substrate, 4 μm buffer layer, 15 nm of GaN, 18 nm of AlGaN (with an Al composition of approximately 23%), and 100 nm of p-GaN channel layer. The Mg doping concentration in the p-GaN layer is 3×10^{19} cm^{-3} and the body hole concentration is 4×10^{17} cm^{-3}. The 8-inch wafer is cut into rectangular pieces of 1.5×1.5 cm^2 by a Disco dicing saw. Both devices are mesa isolated by F ion implantation and Ni/Au = 20/100 nm source-drain metals are deposited by electron beam evaporation. Before metal deposition, the p-GaN surface is rinsed with BOE (7 : 1) solution for 2 min to remove the native oxide layer, which is essential for achieving low specific contact resistance. Then, ohmic contacts are formed by annealing at 500 ˚C for 5 min in O_2 atmosphere. The transfer length method (TLM) measurements show that the specific contact resistivity is 5.81×10^{-4} Ω·cm^2 and the contact resistance is 58.5 Ω·mm.

For device A, we utilized ICP dry etching to slowly etch a 30 nm deep trench in the gate region, leaving 70 nm thickness of p-GaN. During the etching process, the RF power was set at 55 W, ICP power at 0 W, BCl_3 flow rate at 25 sccm, and Cl_2 flow rate at 0 sccm. After etching, we performed *in situ* H plasma treatment on the gate trench bottom using a self-aligned process. The treatment was conducted using an Oxford Plasmalab System 100 ICP 180, with ICP power of 300 W, RF power of 2 W, chamber pressure of 8 mTorr, and the treatment time was 2 min. For device B, we also used ICP dry etching to slowly etch an 85 nm deep trench in the gate region, leaving 15 nm thickness of p-GaN to provide a 2DHG channel for the device. After etching, we immersed device B in an 85 ˚C solution of tetramethylammonium hydroxide (TMAH) for 60 min to repair the etch damage at the bottom of the trench.

Following that, the two devices, A and B, were then placed into an atomic layer deposition (ALD) apparatus to deposit a 10 nm Al_2O_3 layer as a gate dielectric. The deposition was carried out at a chamber temperature of 300 ˚C, with a growth rate of 0.9 Å/cycle. Next, Ni/Au = 50/150 nm was deposited onto the gate metal of both devices using an electron beam evaporator. The Al_2O_3 on the surfaces of the gate and drain metal was then etched off using an ICP 180, followed by a 5-min annealing at 450 ˚C in an N_2 atmosphere for both samples. The purpose of this step was to facilitate the diffusion of H atoms into the p-GaN, and to eliminate the surface states between the Al_2O_3 film and the p-GaN.

The gate-source distance (L_{GS}) of the device is 6 μm, the gate-drain distance (L_{GD}) is also 6 μm, the gate length (L) is 3 μm, and the gate width (W) is 110 μm.

3. Results and discussion

The linear transfer curve of device A is shown in Fig. 2(a). During the measurement, the source was grounded, the drain voltage (V_D) was set to −5 V, and the gate voltage (V_{GS}) was swept from 1 V to −8 V. The peak transconductance ($g_{m\text{-}max}$) of device A was 0.45 mS/mm, which occurred at V_{GS} of −5.57 V. Using the linear extrapolation method at the maximum transconductance, the threshold voltage (V_{TH}) of device A was extracted to be −3.8 V. Alternatively, the threshold voltage can be defined using the specific current value method (taking the current density $-I_D$ = 10 μA/mm), which yields a V_{TH} of −3.41 V. In either case, the V_{TH} of device A, which was fabricated with a 30 nm-deep gate trench and *in situ* H plasma treatment, is negative, indicating that the device operates in enhancement mode as intended.

The linear transfer characteristics of device B are shown in Fig. 2(b). The device was tested using the same method as device A. The peak transconductance of device B was 0.21 mS/mm, and the threshold voltage (V_{TH}) was extracted using the linear extrapolation method at maximum transconductance, which gave a value of −1.4 V. The specific current method, which utilized a current density of I_D = −10 μA/mm, was also employed to define the threshold voltage of device B, resulting in a value of −0.35 V. These results demonstrate that device B has also achieved enhancement-mode operation after etching a gate trench with a depth of 85 nm. Table 1 presents a comparison of the threshold voltages extracted using different methods for devices A and B.

The carrier mobility in field-effect transistors is affected by three physical mechanisms, which can be defined as[16–19]:

$$\frac{1}{\mu} = \frac{1}{\mu_{ph}} + \frac{1}{\mu_C} + \frac{1}{\mu_{sr}}, \quad (1)$$

μ_{ph} is the mobility corresponding to phonon scattering, μ_C is the mobility corresponding to Coulomb scattering, and μ_{sr} is the mobility corresponding to dislocation scattering caused by surface roughness. Studies have shown that in the range of 298–348 K, the field-effect mobility is mainly affected by surface roughness[20]. ICP dry etching can bring significant rough-

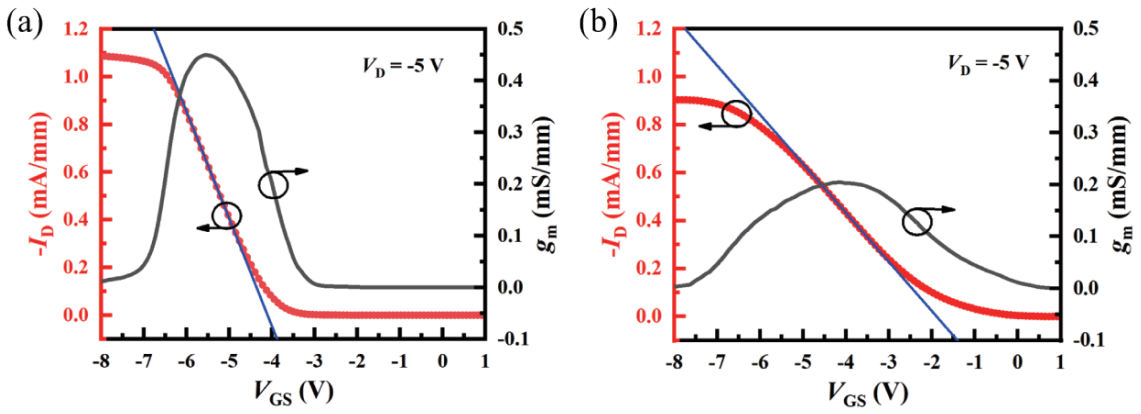

Fig. 2. (Color online) Linear scale transfer characteristics of the devices. (a) Device A; (b) device B.

Table 1. Threshold voltages of device A and B extracted by different methods.

Extract method	Linear extrapolation method at maximum transconductance	Specific current method ($-I_D$ = 10 μA/mm)
V_{TH} of device A (V)	−3.8	−3.41
V_{TH} of device B (V)	−1.4	−0.35

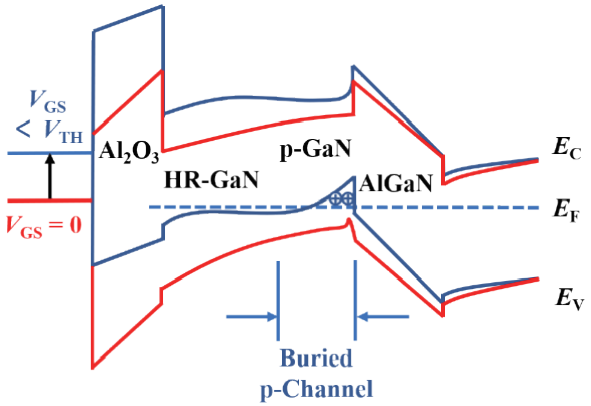

Fig. 3. (Color online) Energy band diagram under the gate region of the device A at V_{GS} = 0 V and V_{GS} < V_{TH}.

ness to the etched surface, and the direct contact between the etched surface of device B and the 2DHG channel reduces the carrier mobility in the channel. In order to further substantiate the aforementioned proposition, the mobility of devices A and B was individually calculated. The mobility of the device in its linear regime satisfies the following relationship:

$$\mu = \frac{g_m L}{C_{OX} W (V_{TH} - V_{GS})}, \tag{2}$$

C_{OX} represents the capacitance of the oxide gate dielectric, the gate dielectric material used in this experiment is Al_2O_3, with a corresponding C_{OX} value of 5.77×10^{-7} F/cm^2. For device A, the maximum mobility was obtained at V_{GS} = −3.86 V.

$$\mu_{max\text{-}A} = \frac{1.54 \times 10^{-5}\ \text{S} \times 3\ \mu\text{m}}{5.77 \times 10^{-7}\ \text{F/cm}^2 \times 110\ \mu\text{m} \times (-3.8\ \text{V} + 3.86\ \text{V})} = 12.13\ \text{cm}^2/(\text{V} \cdot \text{s}). \tag{3}$$

For device B, the maximum mobility was obtained at V_{GS} = −1.43 V.

$$\mu_{max\text{-}B} = \frac{6.398 \times 10^{-6}\ \text{S} \times 3\ \mu\text{m}}{5.77 \times 10^{-7}\ \text{F/cm}^2 \times 110\ \mu\text{m} \times (-1.4\ \text{V} + 1.43\ \text{V})} = 10.08\ \text{cm}^2/(\text{V} \cdot \text{s}). \tag{4}$$

Regarding p-channel devices, the threshold voltage V_{TH} can be understood from a band perspective as the voltage at which the valence band E_V is just above the Fermi level. Fig. 3 shows the band diagram of device A in the region below the gate for V_{GS} = 0 V and V_{GS} < V_{TH}. The p-GaN at the top of this region has been plasma treated with hydrogen, resulting in the formation of Mg-H neutral complexes with H atoms due to the Mg acceptor doping. The passivated Mg acceptors are unable to provide holes, causing the band to bend downwards and creating a hole barrier, which separates the p-type carrier channel from the top of the p-GaN etch interface. The downward band bending extends the depleted region of the p-GaN layer into the underlying AlGaN barrier layer, resulting in a depleted channel region below the gate for V_{GS} = 0 V, where there are not enough holes to conduct and the device is in the off state. The HR-GaN passivated with H plasma maintains its single-crystal structure, with the Fermi level located at the middle of the HR-GaN band[21]. When a negative voltage is applied to the gate, the band of the channel moves relative to the Fermi level, and when V_{GS} < V_{TH}, the valence band of the channel moves above the Fermi level, resulting in the appearance of a 2D hole gas channel and the device turns on.

An ideal power switch should have zero leakage current in the off state but in reality this cannot be achieved, which is the source of static power consumption in power switch devices. In other words, the larger the switch ratio, the lower the circuit loss. The transfer characteristics in semi-log coordinates of devices A and B are presented in Fig. 4 and it can be observed that the off-state leakage current density of device

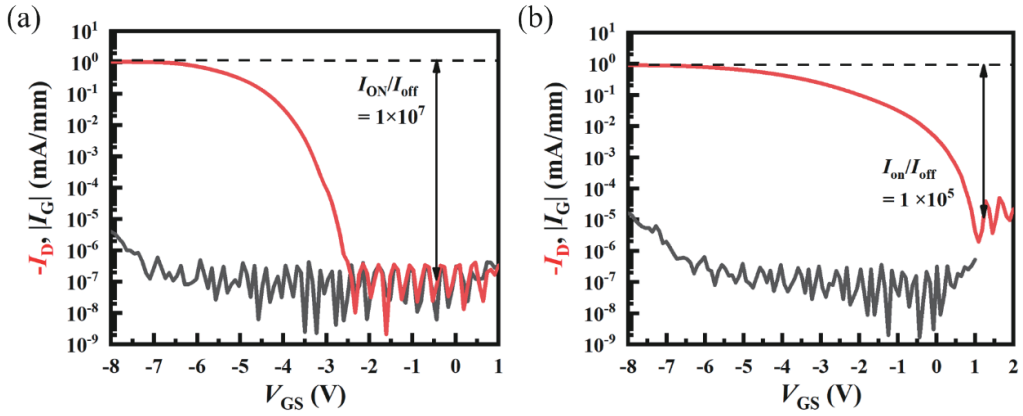

Fig. 4. (Color online) Semi-log scale transfer characteristics and gate leakage currents of devices. (a) Device A; (b) device B.

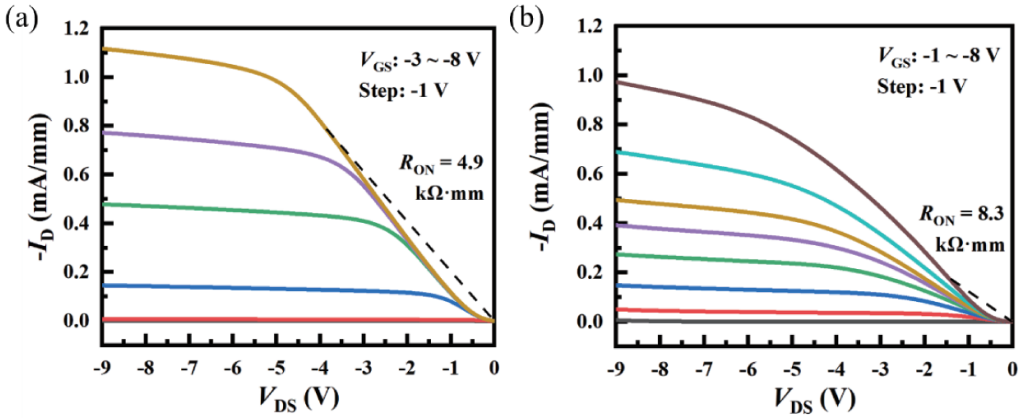

Fig. 5. (Color online) Output characteristics of devices: (a) device A; (b) device B.

A is effectively controlled at the level of 10^{-7} mA/mm, while the off-state leakage current density of device B reaches the level of 10^{-5} mA/mm, which is much higher than that of device A. This happens because ion bombardment during etching processes causes physical damage to the etched surface, resulting in leakage paths that lead to increased leakage current[8]. Due to its lower off-state leakage, device A achieves a switch ratio of 1×10^7, which is two orders of magnitude higher than that of device B.

In an ideal device, no current should flow at the gate, so gate leakage in circuits is considered a noise source that can degrade overall circuit performance. Fig. 4 shows the logarithmic plot of the gate leakage current (I_G) for devices A and B, with source and drain grounded and gate voltage V_{GS} swept from 1 to −8 V. The $|I_G|$ of device B is stable below 1×10^{-6} mA/mm for V_{GS} greater than −5.5 V, and it starts to increase when V_{GS} is less than −5 V, reaching 1.62×10^{-5} mA/mm at V_{GS} = −8 V. This is because the gate dielectric material Al_2O_3 has a large bandgap and a relatively high dielectric constant. Defect states at the interface between the gate dielectric layer and the semiconductor and within the gate dielectric layer can significantly affect the device's gate leakage and threshold voltage stability[22]. Rapid thermal annealing (RTA) is an effective method for repairing defect states[22, 23]. Devices A and B were annealed for 5 min at 450 °C in an N_2 atmosphere after the gate dielectric was grown, which repaired the defect states at the interface between the gate dielectric and p-GaN and within the gate dielectric layer. This is also one reason why devices A and B exhibit low gate leakage current.

The performance of device A exhibits superior ability in suppressing gate leakage current compared to device B. As shown in Fig. 4, $|I_G|$ remains below 1×10^{-6} mA/mm and stable when V_{GS} is greater than −7 V, and only begins to increase after V_{GS} exceeds −7 V. At V_{GS} = −8 V, the I_g of device A is 4.01×10^{-6} mA/mm. This is because the HR-GaN obtained through H plasma treatment can act as a gate dielectric to some extent, suppressing gate leakage current.

To investigate the impact of etching damage on carrier transport in the channel, we tested the output characteristics of device A and device B, and extracted the on-resistance at the threshold voltage. During the test, the source was grounded, and V_{DS} was scanned from 0 to −9 V. For device A, V_{GS} was scanned from −3 to −8 V with a step of −1 V. For device B, V_{GS} was scanned from −1 to −8 V due to its higher threshold voltage. As shown in Fig. 5, device A exhibited a higher saturation current density of 1.12 mA/mm at V_{GS} = −9 V, while device B only reached a saturation current density of 0.97 mA/mm at the same gate voltage. In the absence of other factors, the trade-off between the saturation current density and the threshold voltage is expected because reducing the thickness of the gate region channel layer to achieve a more enhanced threshold voltage also limits the carrier concentration and thus reduces the saturation current density. Device A showed a higher saturation current density despite having a more enhanced threshold voltage than device B, which indicates the significant role played by etching damage. The etching damage creates N vacancies[24], which act as donor levels that will release an electron to compound with hole carriers in the channel, thus reducing the carrier concen-

Table 2. Benchmark of p-channel GaN-based FETs

Work unit	Platform	V_{TH}[a] (V)	$I_{ON\text{-}max}$ (mA/mm)	I_{ON}/I_{OFF}[b]
RWTH[2]	p-/i-GaN/AlInGaN/GaN/AlN	−1.12 (V_D = −8 V)	6.79 (V_D = −8 V)	7
RWTH[25]	p-/i-GaN/AlInGaN/GaN/AlN	−0.5 (V_D = −5 V)	1.81 (V_D = −5 V)	8
HRL[26]	p-/i-GaN/AlGaN/GaN	−0.36 (V_D = −0.1 V)	1.65 (V_D = −5 V)	6
AIST[27]	p-/i-GaN/AlGaN/GaN	−0.75 (V_D = −5 V)	0.09 (V_D = −5 V)	3
HKUST[28]	p-GaN/AlGaN/GaN	−1.7 (V_D = −5 V)	3.38 (V_D = −5 V)	7
This work	p-GaN/AlGaN/GaN	−3.41 (V_D = −5 V)	1.12 (V_D = −5 V)	7

[a]Extracted at $-I_D$ = 10 μA/mm.

[b]Extracted at V_D which is the same as noted in V_{TH} and with overdriven V_{GS}.

tration. The on-resistance (R_{ON}) at the threshold voltage was extracted and found to be 4.9 kΩ·mm for device A and 8.3 kΩ·mm for device B. The smaller R_{ON} of device A compared to device B is beneficial for achieving low power consumption in the overall circuit.

In Table 2, a comparison is presented between this device and other reported enhanced GaN pFETs in the literature. Among all the devices listed in the table, our device exhibits a significant enhancement mode and high I_{ON}/I_{OFF} ration advantage. Moreover, another advantage of this device is that it is fabricated base on a p-GaN/AlGaN/GaN epitaxial structure, which is highly compatible for monolithic integration with HEMTs devices, thereby faciliting the realization of commercial GaN CMOS circuits.

4. Conclusion

Using an H plasma treatment technique, we successfully developed an E-mode p-GaN-MOSFET on a commercial p-GaN/AlGaN/GaN-on-Si platform. The buried p-GaN channel is positioned away from the top GaN surface and gate-oxide/GaN interface, effectively mitigating the severe I_{ON} degradation induced by aggressive gate recess. This approach involves retaining a thicker p-GaN layer as the buried channel under the HR-GaN layer. The p-GaN/AlGaN/GaN-on-Si platform presents a promising avenue for monolithically integrating E-mode pFET and nFET, which could lead to the development of complementary and more robust GaN power ICs.

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