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High-performance enhancement-mode GaN-based p-FETs fabricated with O_3-Al_2O_3/HfO_2-stacked gate dielectric

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Abstract: In this letter, an enhancement-mode (E-mode) GaN p-channel field-effect transistor (p-FET) with a high current density of −4.9 mA/mm based on a O_3-Al_2O_3/HfO_2 (5/15 nm) stacked gate dielectric was demonstrated on a p^{++}-GaN/p-GaN/AlN/AlGaN/AlN/GaN/Si heterostructure. Attributed to the p^{++}-GaN capping layer, a good linear ohmic *I*–*V* characteristic featuring a low-contact resistivity (ρ_c) of 1.34×10^{-4} Ω·cm^2 was obtained. High gate leakage associated with the HfO_2 high-*k* gate dielectric was effectively blocked by the 5-nm O_3-Al_2O_3 insertion layer grown by atomic layer deposition, contributing to a high I_{ON}/I_{OFF} ratio of 6×10^6 and a remarkably reduced subthreshold swing (SS) in the fabricated p-FETs. The proposed structure is compelling for energy-efficient GaN complementary logic (CL) circuits.

Key words: GaN; p-FETs; enhancement-mode; HfO_2; subthreshold swing

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1. Introduction

In last few decades, GaN power high-electron-mobility transistors (HEMTs) have become an indispensable core component of power electronics, owing to their high breakdown voltage and fast switching speed[1–6]. To further enhance the reliability and speed of the device, monolithically integrated GaN-based peripheral circuits composed of logic modules that serve as the driving, control, sensing and protection units, are highly desirable. One of the promising technologies, especially for high-temperature operation application, is the GaN-based CMOS platform, which delivers extremely low power consumption[7]. The key issue of GaN-based CMOS technology is the low current density of the GaN p-FETs, which ascribe to the high activation energy (~170 meV) of Mg doping, low hole mobility and the difficulty in forming ohmic contact due to the p-GaN deep valance bands[8–10]. To improve the conduction characteristic of the GaN p-channel device, polarization-enhanced epitaxy technology was adopted to induce high-density two-dimensional hole gas (2DHG), which can effectively increase carrier concentration[11–14]. At the same time, in order to achieve the enhancement mode (E-mode), a partial recessed p-GaN channel in the gate region is needed[15–22].

As the core component of the pull-up device in GaN-based CMOS logic circuit topology, the p-FETs with a low subthreshold slope (SS) are beneficial for achieving lower power consumption of the logic circuit due to the operating voltage reduction[23]. A high-*k* gate dielectric is a facile method that reduces the SS of the devices. Among all the high-*k* dielectrics, HfO_2 is favorable due to its large dielectric constant (~25) and perfect compatibility with CMOS fabrication processes[24]. Therefore, HfO_2 is selected as the high-*k* dielectric material for our fabricated GaN p-FETs.

In this work, E-mode GaN p-FETs with O_3-Al_2O_3/HfO_2-stacked gate dielectric are fabricated on a p^{++}-GaN/p-GaN/AlN/AlGaN/AlN/GaN heterostructure grown on a Si substrate. The O_3-Al_2O_3 insertion layer effectively improves the voltage blocking of the stack dielectric and reduces the leakage current. Meanwhile, the introduction of HfO_2 reduces the SS of GaN p-FETs from 161 mV/dec to 107 mV/dec, which significantly improves the current performance of the GaN p-FETs. The improved subthreshold performance of the p-FETs enables high ON-OFF current ratio with low operating voltage, which is beneficial for reducing the power consumption of GaN-based CMOS logic driver circuits.

2. Epitaxial structure and dielectric leakage characterization

Fig. 1(a) shows the cross-sectional schematic of the fabricated metal–oxide–semiconductor (MOS) device for dielectric leakage characterization. The employed p^{++}-GaN/p-GaN/AlN/AlGaN/AlN/GaN heterostructure was grown by metal–organic chemical vapor deposition (MOCVD) on the Si substrate. It consists of a ~10-nm p^{++}-GaN capping layer (Mg: 2×10^{20} cm^{-3}), a ~85-nm p-GaN layer (Mg: (4–6) $\times 10^{19}$ cm^{-3}), a ~2-nm AlN polarization enhancement layer, a ~3-nm $Al_{0.25}Ga_{0.75}N$ ultrathin barrier layer (UTB), a ~1-nm AlN interface enhancement layer, a 300-nm unintentionally doped

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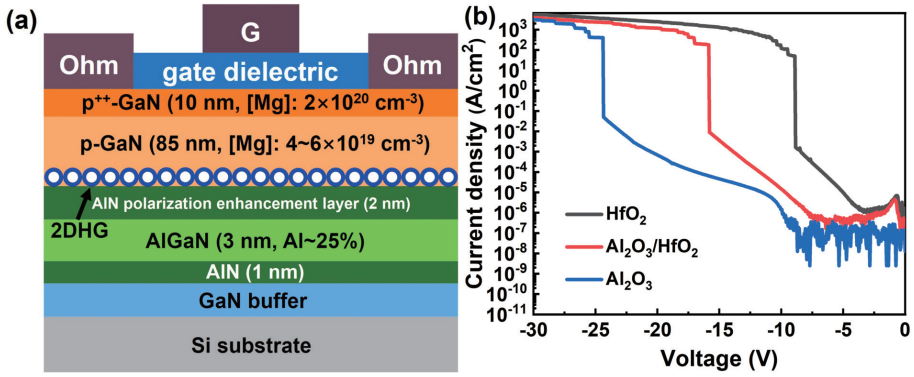

Fig. 1. (Color online) (a) Cross-sectional schematic and (b) current density–voltage curves of the MOS device on the p^{++}-GaN/p-GaN/AlN/AlGaN/AlN/GaN heterostructure.

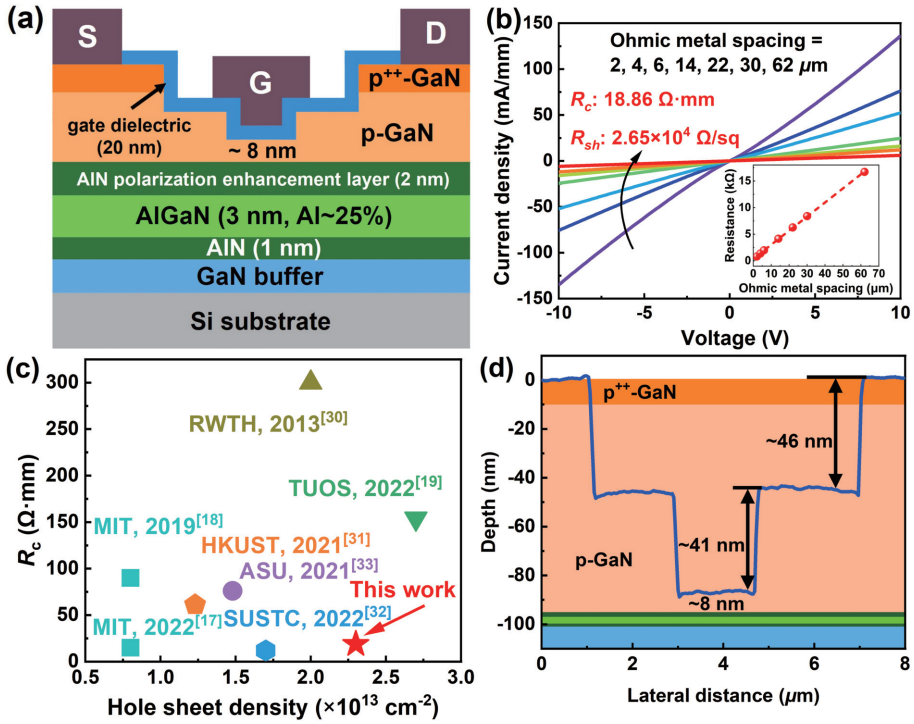

Fig. 2. (Color online) (a) Cross-sectional schematic of the fabricate E-mode GaN p-FETs. (b) TLM analysis of the ohmic contact. (c) Benchmarking the R_c and hole sheet density of the fabricated GaN p-FET with some state-of-the-art GaN p-FETs. (d) Depth profile of the gate recess trench measured by the atomic force microscope. The inset figure presents measured resistances as a function of ohmic metal spacing.

GaN n-channel layer and a 3.6-μm (Al)GaN high-resistivity buffer layer with C doping. The 3-nm UTB-$Al_{0.25}Ga_{0.75}N$ layer is intended for a AlGaN-recess-free E-mode n-FETs for p/n-FETs integration[25]. The hole sheet density and mobility were measured to be 2.3 × 10^{13} cm^{-2} and 11.5 $cm^2/(V{\cdot}s)$ respectively by Van der Pauw Hall measurement. The gate dielectrics for comparison are a 20-nm HfO_2, 20-nm O_3-Al_2O_3 and an O_3-Al_2O_3/HfO_2 (5/15 nm) stack, both of which are grown by atomic layer deposition (ALD).

The leakage characteristic of different dielectrics is shown in Fig. 1(b). The 20-nm HfO_2 shows a lower breakdown voltage and higher leakage current density than that of the 20-nm O_3-Al_2O_3 due to its lower band gap (HfO_2: ~5.8 eV, O_3-Al_2O_3: ~7.1 eV) and valence band offset from p-GaN (p-GaN/HfO_2: ~0.3 eV, p-GaN/O_3-Al_2O_3: ~1.7 eV)[26, 27]. The introduction of the 5-nm O_3-Al_2O_3 insertion layer can effectively reduce the leakage of the O_3-Al_2O_3/HfO_2 stack and improve its voltage-blocking capability.

3. Device fabrication and characteristics of E-mode GaN p-FETs

Fig. 2(a) exhibits the cross-sectional schematic of the fabricated E-mode GaN p-FETs. Device fabrication commenced with source/drain definition by photolithography, followed by Ni/Au (50/100 nm) metal stack evaporation. Rapid thermal annealing (RTA) in the air environment at 550 °C for 60 s was performed after lift-off. Thanks to the p^{++}-GaN capping layer, linear I–V curves were obtained. The contact resistance (R_c) of 18.86 Ω·mm (ρ_c = 1.34 × 10^{-4} Ω·cm^2) and sheet resistance (R_{sh}) of 2.65 × 10^4 Ω/sq are determined by the transfer length method (TLM) respectively, as shown in Fig. 2(b). Fig. 2(c) benchmarks the R_c and hole sheet density of the heterostructure used in this work with other similar Ⅲ-nitride heterostructures. The low R_c achieved is comparable to state-of-the-art results.

The mesa isolation was implemented by the Cl_2/BCl_3-

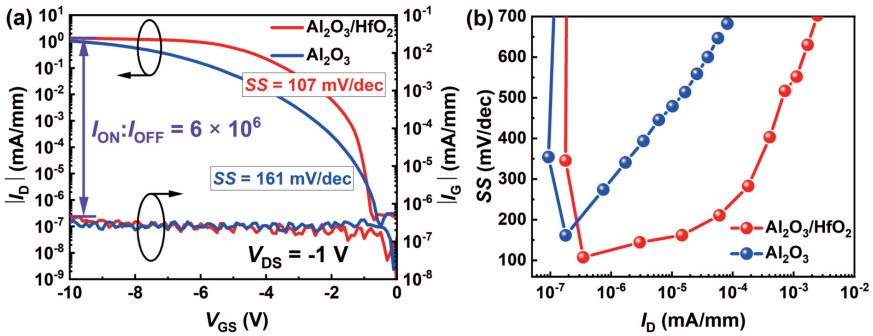

Fig. 3. (Color online) (a) DC transfer and (b) SS vs I_D plot of fabricated GaN p-FETs with the O_3-Al_2O_3 and O_3-Al_2O_3/HfO_2 stack as the gate dielectric.

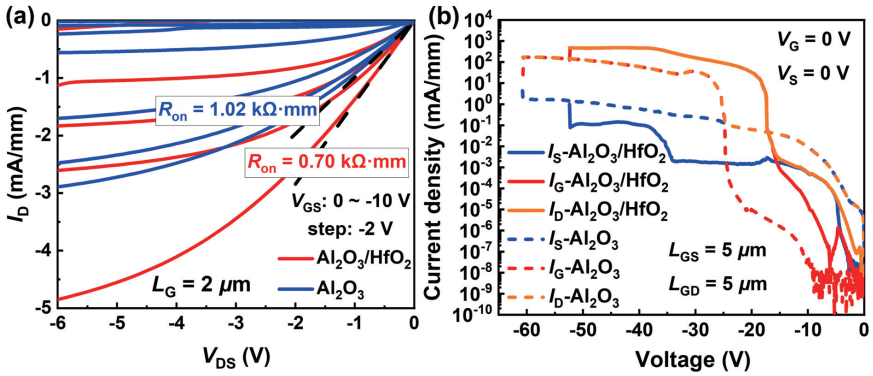

Fig. 4. (Color online) (a) DC output and (b) OFF-state characteristics of fabricated GaN p-FETs with the O_3-Al_2O_3 and O_3-Al_2O_3/HfO_2 stack as the gate dielectric.

based inductively coupled plasma-reactive ion etching (ICP-RIE) process to the GaN buffer. A two-step gate etching process was adopted to overcome the decreased OFF-state blocking voltage associated with the p^{++}-GaN capping layer[28]. The remaining p-GaN under the central gate trench is 8 nm as confirmed by atomic force microscopy (AFM), as shown in Fig. 2(d). The two-step gate trench was then subjected to an UV/O_3 treatment at 100 °C for 30 min. Prior to the deposition of the gate dielectric, *in-situ* remote plasma pretreatments (RPP)[29] by using NH_3/N_2 plasmas applied were conducted. After the source/drain region opening, the GaN p-FET fabrication was completed with an evaporated Ni/Au (40/400 nm) metal stack as the gate metal and probing pad. For comparison, the devices using the 20-nm O_3-Al_2O_3 and the O_3-Al_2O_3/HfO_2 (5/15 nm) stack as the gate dielectric are both fabricated. The fabricated GaN p-FETs possess a gate length (L_G) of 2 μm, an equivalent gate to source length (L_{GS}) and a gate to drain length (L_{GD}) of 5 μm.

Fig. 3(a) shows DC transfer characteristics of the fabricated GaN p-FETs with an O_3-Al_2O_3 and O_3-Al_2O_3/HfO_2 stack as the gate dielectric at V_{DS} of –1 V. Since the 8-nm p-GaN layer only remained at the bottom of the gate trench featuring the weakening of the built-in polarization, both of the devices behave as E-modes and exhibit a high I_{ON}/I_{OFF} ratio of 6 × 10^6. Thanks to the high-quality O_3-Al_2O_3 insertion layer, the device with the O_3-Al_2O_3/HfO_2 gate stack shows a low gate leakage below 10^{-6} mA/mm, the same as the device with 20-nm O_3-Al_2O_3 gate dielectric. In addition, a steeper transfer curve is obtained due to the high dielectric constant of HfO_2 for the GaN p-FET with the O_3-Al_2O_3/HfO_2 gate stack. Its minimum SS is extracted to be 107 mV/dec, which is significantly lower than the 161 mV/dec of the comparison device (see Fig. 3(b)).

Table 1. Benchmark of GaN-based p-FETs.

	V_{th} (V)	$I_{d,max}$ (mA/mm)	I_{ON}/I_{OFF}	SS (mV/dec)
MIT[16]	–0.5	–45	10^4	800
Cornell[20]	–0.35	–10	10^4	1027
HRL[22]	–0.36	–1.65	10^6	304
HKUST[30]	–1.7	–6.1	10^7	230
ASU[31]	–0.6	–0.2	5 × 10^7	123
This work	–0.8	–4.9	6 × 10^6	107

Fig. 4(a) depicts the output curves of the devices. Owing to the p^{++}-GaN cap layer of the epitaxial structure, an offset voltage, which is usually observed in I_{DS}–V_{DS} curves of p-FETs fabricated on the moderate Mg-doped p-GaN layer[31, 32], is effectively eliminated. The O_3-Al_2O_3/HfO_2-stacked device with better channel modulation capability delivers a high-saturation current density of –4.9 mA/mm and an on-resistance (R_{on}) of 0.70 kΩ·mm at V_{GS} = –10 V. Three-terminal OFF-state characteristics of the fabricated GaN p-FET is plotted in Fig. 4(b). A destructive hard breakdown was observed at –52 and –61 V on the devices with the O_3-Al_2O_3/HfO_2 gate stack and the O_3-Al_2O_3 gate dielectric, respectively.

Table 1 benchmarks the fabricated GaN p-FETs in this work with some other reported GaN p-FETs. Our E-mode GaN p-FETs exhibit high I_{ON}/I_{OFF} ratio and low SS.

The scaling effect on the gate length of the GaN p-FETs was also studied. Much higher $|I_{D,max}|$ and lower R_{on} are obtained (Fig. 5). By optimizing the size of the devices or directly using self-alignment structure[16, 17], the current density of GaN p-FETs will be further improved.

4. Conclusion

In this work, the leakage characteristic of O_3-Al_2O_3 and HfO_2 is investigated on the p-channel GaN device platform.

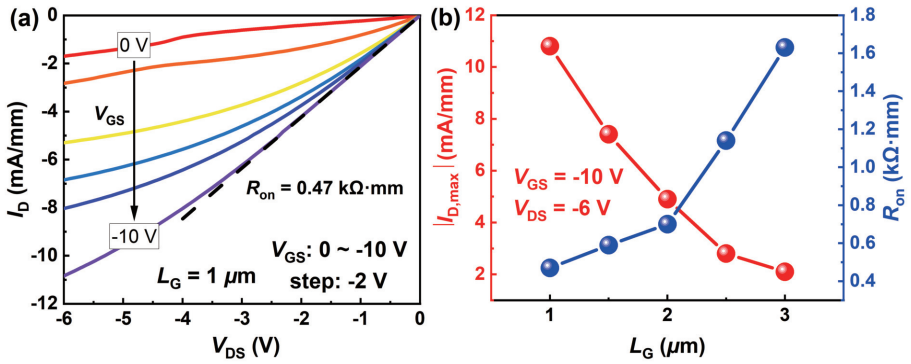

Fig. 5. (Color online) (a) Output characteristics for the GaN p-FET using O_3-Al_2O_3/HfO_2 as the gate stack with L_G of 1 μm. (b) Trend of $|I_{D,max}|$ enhancement and R_{on} reduction with L_G scaling.

The introduction of the O_3-Al_2O_3 insertion layer can effectively reduce the leakage and increase the breakdown voltage of the O_3-Al_2O_3/HfO_2 stack. E-mode GaN p-FETs with an O_3-Al_2O_3/HfO_2 gate stack were fabricated on the p^{++}-GaN/p-GaN/AlN/AlGaN/AlN/GaN/Si heterostructure. The fabricated GaN p-FETs possess a high current density of −4.9 mA/mm, a high I_{ON}/I_{OFF} ratio of 6×10^6 and a low SS of 107 mV/dec, which are promising for applications in GaN CMOS logic platforms.

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