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An 80-GHz DCO utilizing improved SC ladder and promoted DCTL-based hybrid tuning banks

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Abstract: An 80-GHz DCO based on modified hybrid tuning banks is introduced in this paper. To achieve sub-MHz frequency resolution with reduced circuit complexity, the improved circuit topology replaces the conventional circuit topology with two binary-weighted SC cells, enabling eight SC-cell-based improved SC ladders to achieve the same fine-tuning steps as twelve SC-cell-based conventional SC ladders. To achieve lower phase noise and smaller chip size, the promoted binary-weighted digitally controlled transmission lines (DCTLs) are used to implement the coarse and medium tuning banks of the DCO. Compared to the conventional thermometer-coded DCTLs, control bits of the proposed DCTLs are reduced from 30 to 8, and the total length is reduced by 34.3% (from 122.76 to 80.66 μm). Fabricated in 40-nm CMOS, the DCO demonstrated in this work features a small fine-tuning step (483 kHz), a high oscillation frequency (79–85 GHz), and a smaller chip size (0.017 mm^2). Compared to previous work, the modified DCO exhibits an excellent figure of merit with an area (FoM$_A$) of –198 dBc/Hz.

Key words: DCO; switched-capacitor ladder; sub-MHz; digitally controlled transmission lines; tuning bank

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1. Introduction

High-performance digitally controlled oscillators (DCOs) play a crucial role in the development of a credible digital phase-locked loop (DPLL)[1–3]. However, the design of DCOs operating at higher frequency bands, especially in the millimeter wave band, remains challenging due to several limitations such as frequency resolution, tuning range and circuit complexity[4, 5].

As shown in Fig. 1, the DPLL is composed of time to digital converter (TDC), digital loop filter (DLF), a reference phase accumulator (RPA), a phase error calculation module and a variable phase accumulator (VPA). The RPA is responsible for counting the reference phase. The VPA is used to count an integral part of the CKV cycle after frequency division, and the TDC quantizes the fractional modulation. The phase error calculation module obtains the phase error, which arrives at the calibration module through the DLF. The calibration module then calculates a new OTW and sends it to the DCO. Since the fractional modulation is generated by the combination of other modules in the DPLL loop, the resolution of the DPLL loop can be further improved without putting additional fine- tuning pressure on the DCO. Optimization of the tuning bank structure is essential to balance the trade-off between better frequency resolution, lower phase noise, and higher operating frequency for a given millimeter-wave (mm-wave) DCO topology. A switched-capacitor (SC) ladder is often used to pursue higher frequency resolution with less chip size in contrast to the digitally controlled transmission lines (DCTLs)[6–8]. The SC ladder with greater circuit complexity and parasitic capacitance is required for higher frequency resolution, resulting in a lower oscillation frequency and worse phase noise. In addition, the method of changing the operating frequency by controlling the inductance connected to the tuning bank through switches is used to achieve a higher frequency resolution. However, this also increases the complexity of the circuit and reduces the tuning range[9, 10]. Another option is to use DCTLs in the tuning banks of the DCO to achieve a higher Q factor and lower substrate losses[11, 12]. However, the parasitic capacitances caused by the large area of conventional DCTLs will also degrade the performance characteristics of the DCO, such as phase noise and oscillation frequency[13]. Therefore, modifying the tuning banks of the mm-wave DCO to improve the trade-off between chip size, oscillation frequency, phase noise, and frequency resolution remains a challenge.

To address the above challenges, this paper presents an 80-GHz DCO based on modified hybrid tuning banks. An improved SC ladder based on the binary-weighted SC cell is used to realize the DCO trim group (FB), and the sub-MHz trim step size is obtained with low circuit complexity. In addition, the promoted binary-weighted DCTLs technology is adopted in the medium-tuning bank (MB) and coarse-tuning bank (CB) of the DCO to achieve lower phase noise and higher oscillation frequency with a smaller chip size. Measurement results indicate a reasonable compromise among higher oscillation frequency, more compact chip size, lower phase noise, and higher frequency resolution in the DCO.

2. Circuit description and implementation

As shown in Fig. 2, the tuning banks of the 80-GHz DCO consist of a fine-tuning bank based on an improved SC ladder coupled to the secondary coil of a transformer, a coarse-tuning bank, and a medium-tuning bank based on pro-

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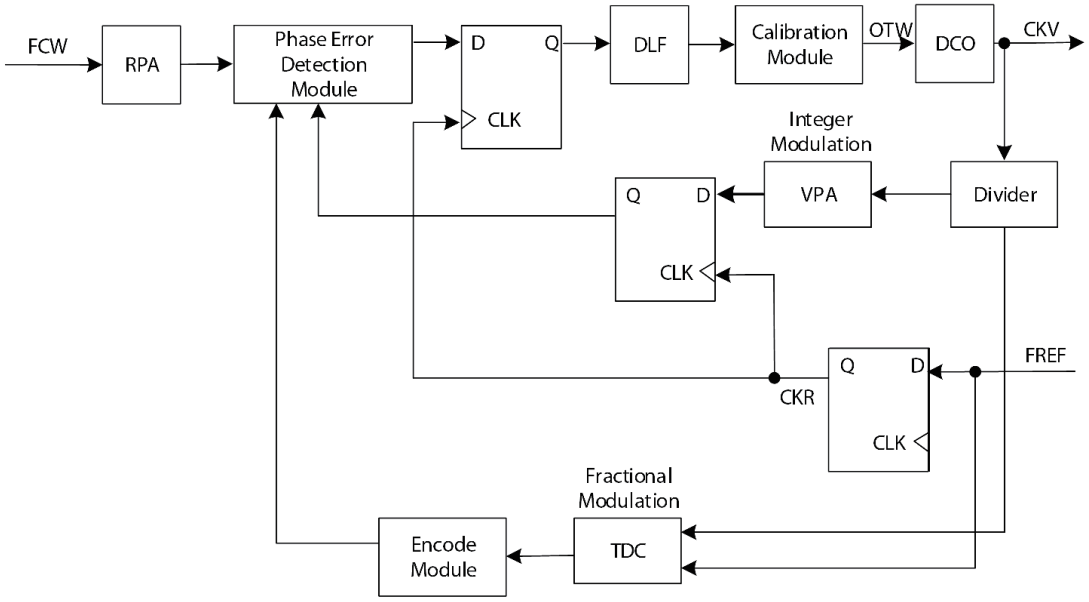


Fig. 1. Block diagram of DPLL.

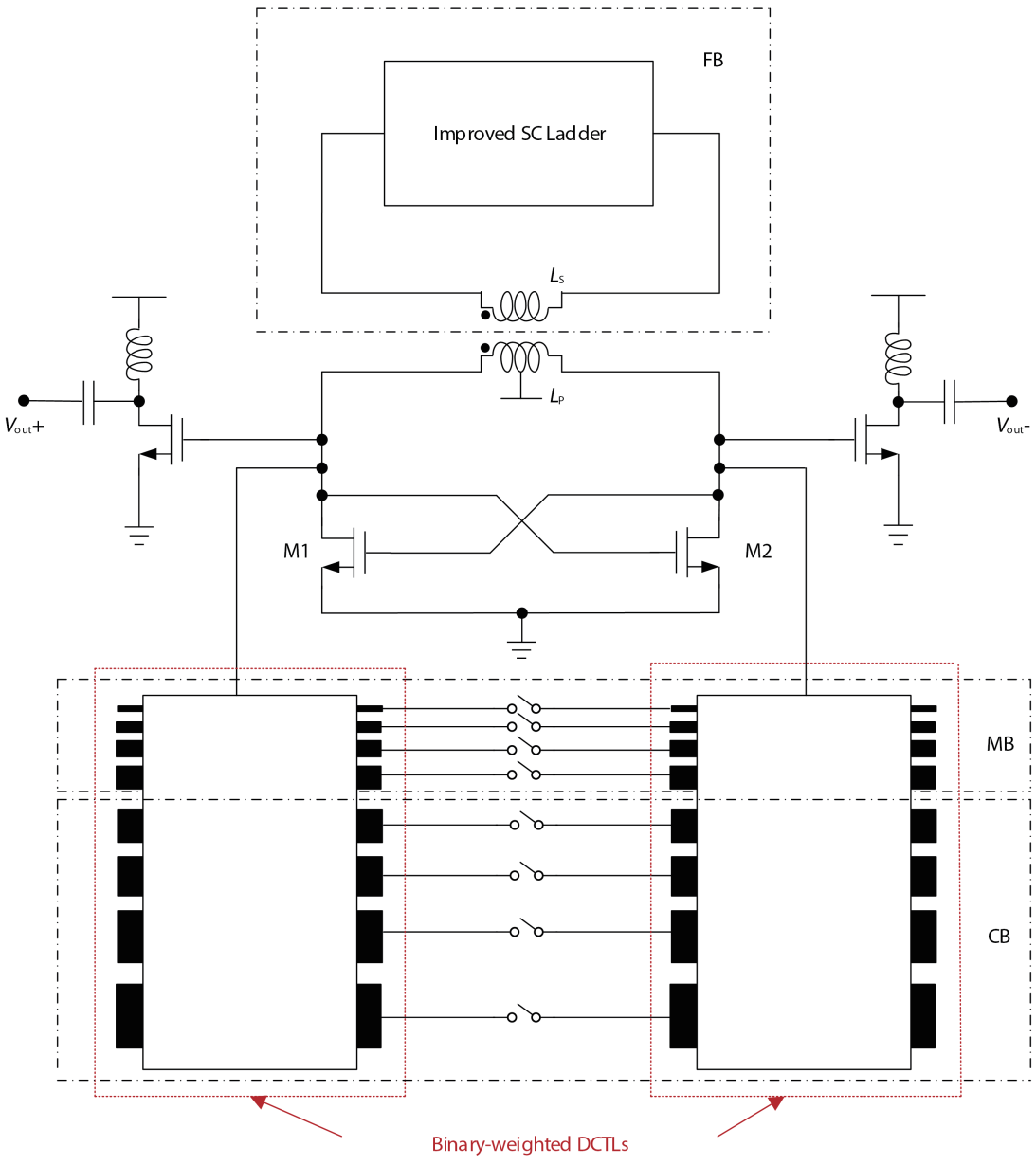
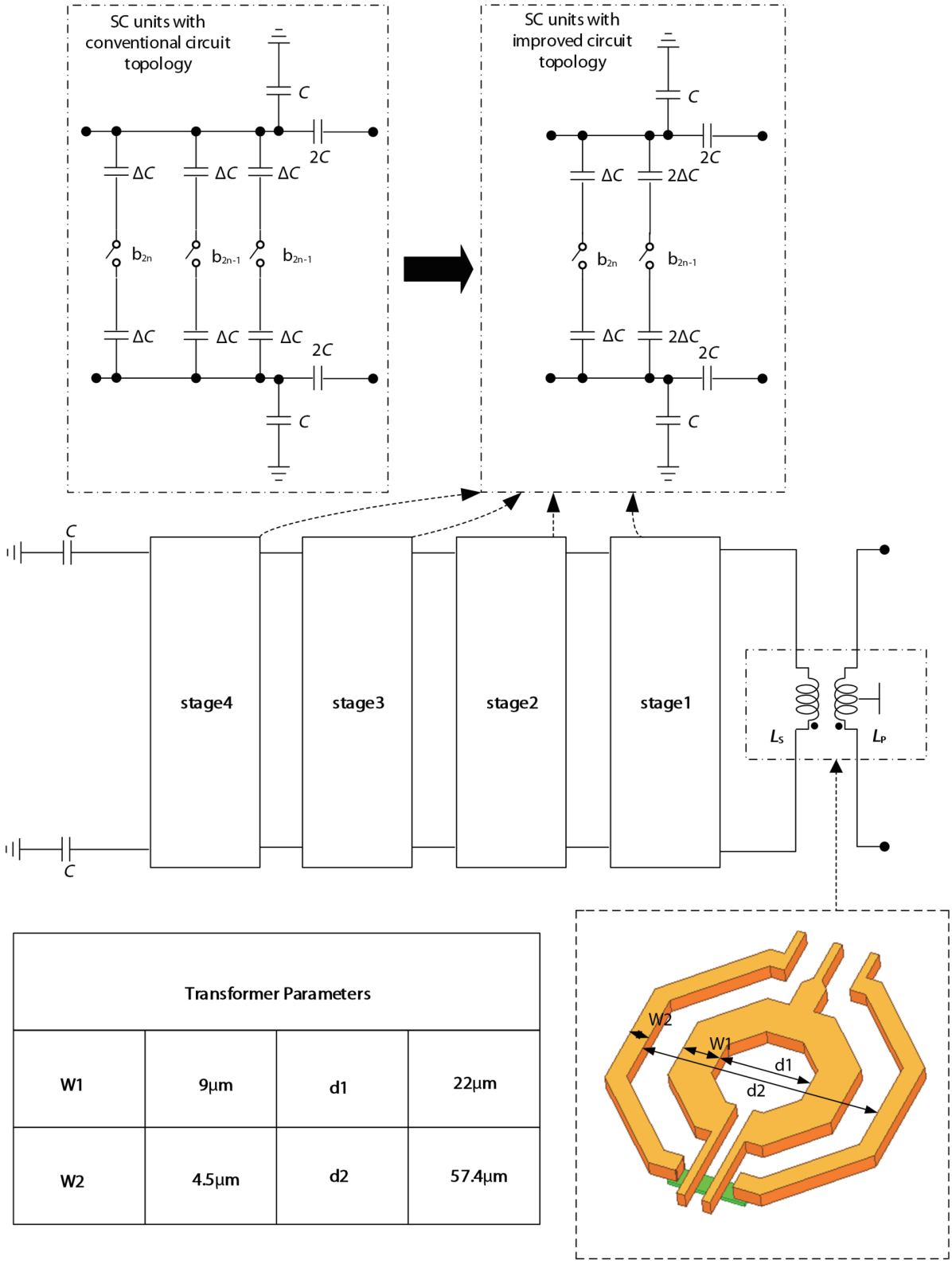


Fig. 2. (Color online) The architecture of the DCO with modified hybrid tuning banks.



Transformer Parameters			
W1	9μm	d1	22μm
W2	4.5μm	d2	57.4μm

Fig. 3. (Color online) The architecture of the FB.

moted binary-weighted DCTLs. Due to the optimized structure of the hybrid tuning resonator, only 16-bit binary control words are required to set the frequency of the DCO.

2.1. Fine-tuning bank

The SC-cell-based improved SC ladders proposed in this paper exhibits the advantage of lower circuit complexity. In addition, it helps to suppress the extra noise caused by more capacitive switches used in the conventional SC ladder. As shown in Fig. 3, the improved circuit topology is used in each SC unit stage of the SC ladder. An improved circuit topology replaces three thermometer-coded SC cells in a conventional circuit topology with two binary-weighted SC cells. The improved circuit topology allows eight modified SC ladder-based SC cells to achieve the same fine-tuning steps as twelve conventional SC ladder-based SC cells, while eliminating four switching tubes, reducing resonator tank losses and further optimizing the DCO's phase noise. The equivalent

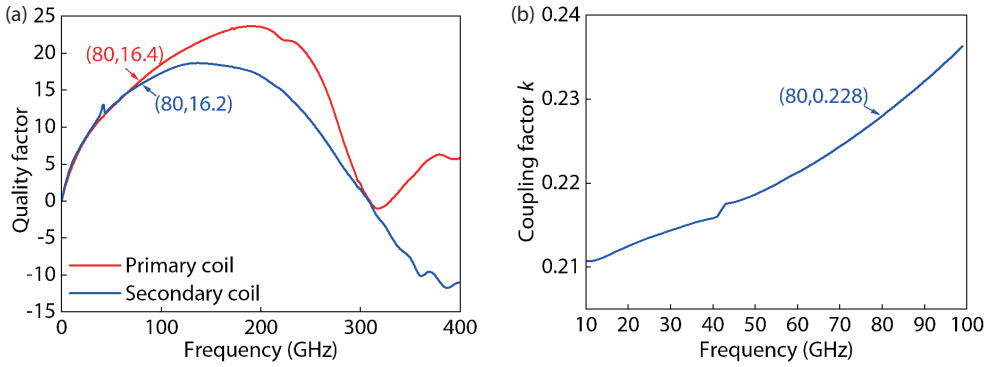


Fig. 4. (Color online) Simulation results of the on-chip transformer. (a) *Q*-factor curve. (b) Coupling coefficient *k* curve.

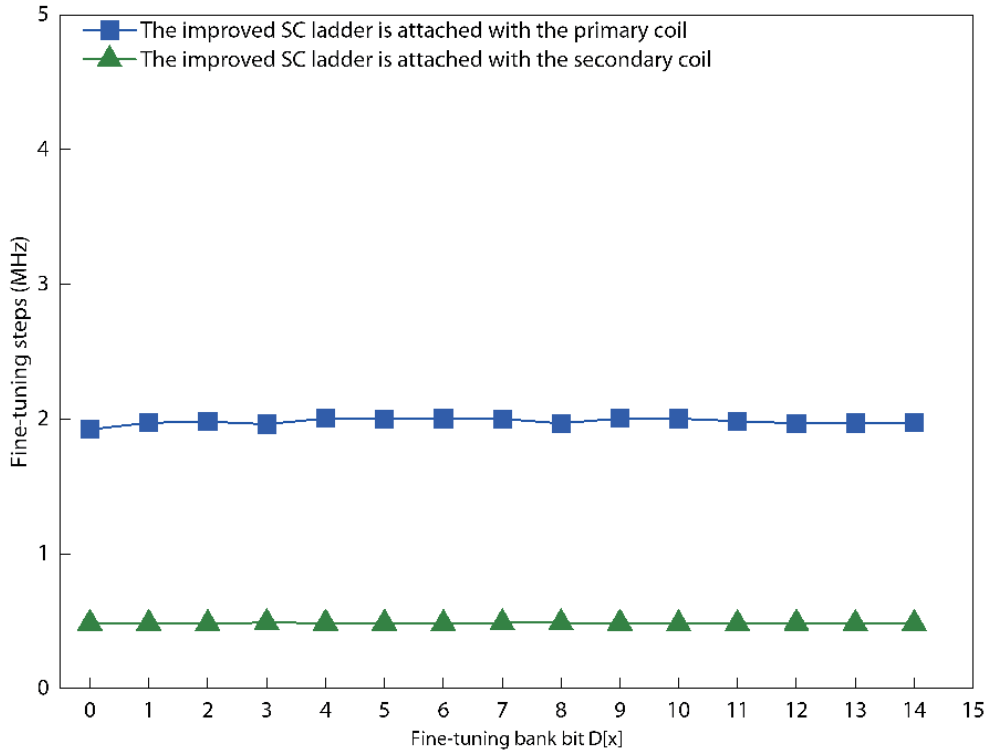


Fig. 5. (Color online) Comparison of simulated results of the fine-tuning steps for the different fine-tuning banks.

capacitance of the SC ladder shown in Fig. 3 can be expressed as[14]

$$C_{eq} \approx C + \left(\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \cdots + \frac{1}{2^{2n-1}} + \frac{1}{2^{2n}}\right)\Delta C. \quad (1)$$

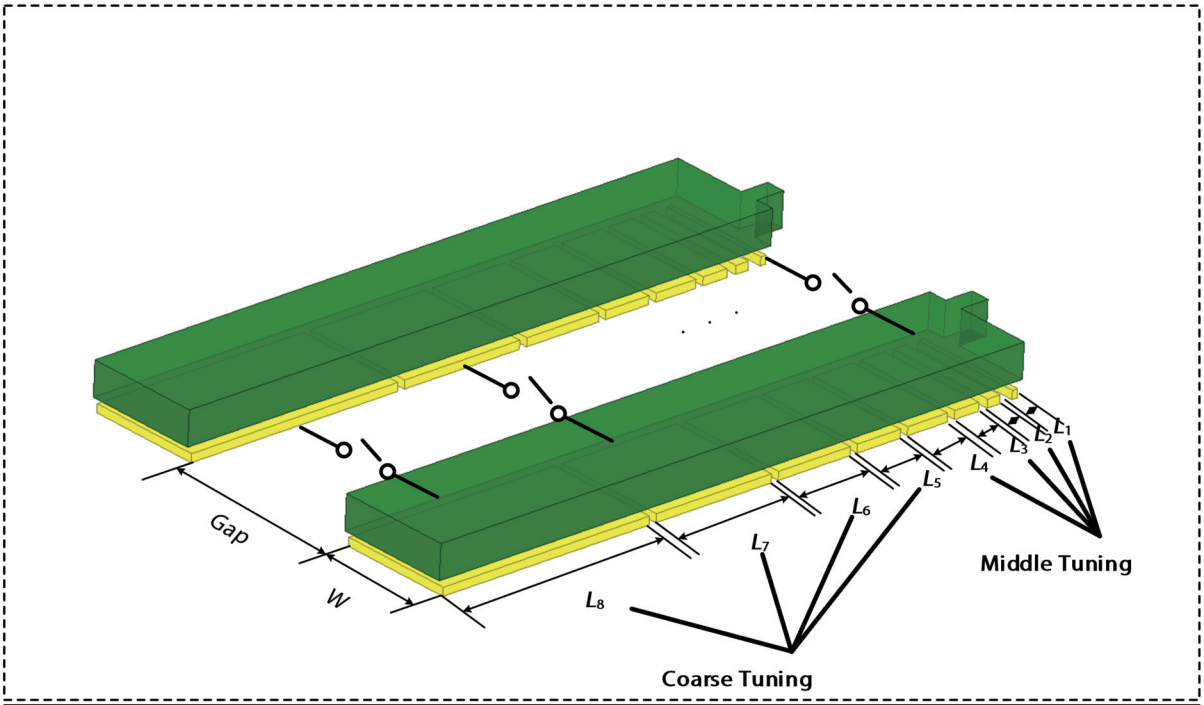
Here ΔC is the most negligible capacitance under the process of the SC ladder with n stage SC units. Eq. (1) shows that the minimum tunable capacitance can be reduced exponentially to $1/2^{2n}\Delta C$. This also means that the fine-tuning steps of the DCO can be further improved. However, too many stages introduce problems, such as increased switch parasitic capacitance and excessive circuit complexity. Therefore, the FB of the DCO consists of four stages of SC units for a better trade-off.

To compensate for the reduced frequency resolution due to fewer SC unit stages to achieve sub-MHz fine-tuning steps, the improved SC ladder is attached to the secondary coil of the transformer with a lower coupling coefficient. Therefore, the larger capacitance change in the SC ladder can be converted into the smaller inductance change in the whole tuning resonator of the DCO by the secondary coil of the transforme[15]. Fig. 4(a) shows that the Q of the two coils of the transformer at the operating frequency is greater than 15. Fig. 4(b) shows that the coupling coefficient of the transformer is less than 0.25, which meets the requirement of the weaker magnetic coupling between the two coils.

It can be seen from Fig. 5 that the simulated average fine-tuning step of the FB based on the improved SC ladder attached to the primary coil of the transformer is about 2 MHz. In comparison, that of the FB based on the improved SC ladder attached to the secondary coil of the transformer is 0.5 MHz.

2.2. Coarse & medium tuning bank

The structure of the DCO's CB and MB is shown in Fig. 6. Compared with conventional thermometer-coded DCTLs, the number of coarse and medium control bits is reduced from 30 to 8 with the promoted binary-weighted DCTLs, and the total length is reduced by 34.3% (from 122.76 to 80.66 μm), which reduces fixed parasitic capacitance and passive component losses, making it more suitable for mm-wave DCOs.



Parameters of the proposed differential transmission lines for digital control

L_1	0.61μm	L_6	10.16μm
L_2	1.58μm	L_7	16.17μm
L_3	2.85μm	L_8	28.4μm
L_4	4.5μm	W	12μm
L_5	6.35μm	*Gap*	20μm

Fig. 6. (Color online) The general layout of the promoted binary-weighted DCTLs in CB and MB.

The equivalent model for promoted binary-weighted DCTLs is shown in Fig. 7. L is the equivalent inductance every unit length of the DCTLs. C represents the coupling capacitance between two adjacent parallel DCTLs. C_M represents the MIM capacitance formed by the TLs and the metal strips underneath. Compared with conventional thermometer-coded DCTLs, this model can also realize the same frequency tuning range with a smaller chip size.

When C_M is turned on by the switches, the DCTLs' characteristic impedance can be calculated as

$$Z_0 = \sqrt{L_0/(C_0 + 2^n C_M/2)} \quad (0 \leqslant n \leqslant 3). \tag{2}$$

From Eq. (2), it can be seen that more capacitance contributed by the closed switches can reduce the characteristic impedance of the DCTLs.

Figs. 8(a) and 8(b) show that the coarse bank based on promoted binary-weighted DCTLs can achieve the same frequency tuning range with a total length 31.7% (from 97.5 to 66.62 μm) shorter than that based on the conventional thermometer-coded DCTLs, and the control bits are reduced from 15 to 4, which reduces fixed parasitic capacitance and passive component losses. Likewise, the total length of the medium bank based on the promoted binary-weighted DCTLs is 44.4% (from 25.26 to 14.04 μm) shorter than the conventional thermometer-coded DCTLs and the control bits are reduced from 15 to 4. As a result, the proposed DCO can achieve a wider frequency tuning range and higher oscillation frequency with fewer control bits and a more compact chip size. Fig. 8(c) compares the length of each bit of the promoted and conventional DCTLs in the CB. The promoted binary-weighted DCTLs have the advantages of fewer switching circuit bits and smaller die sizes than conventional DCTLs. Therefore, the CB and MB of the DCO in this paper are implemented with the modified binary-weighted DCTLs.

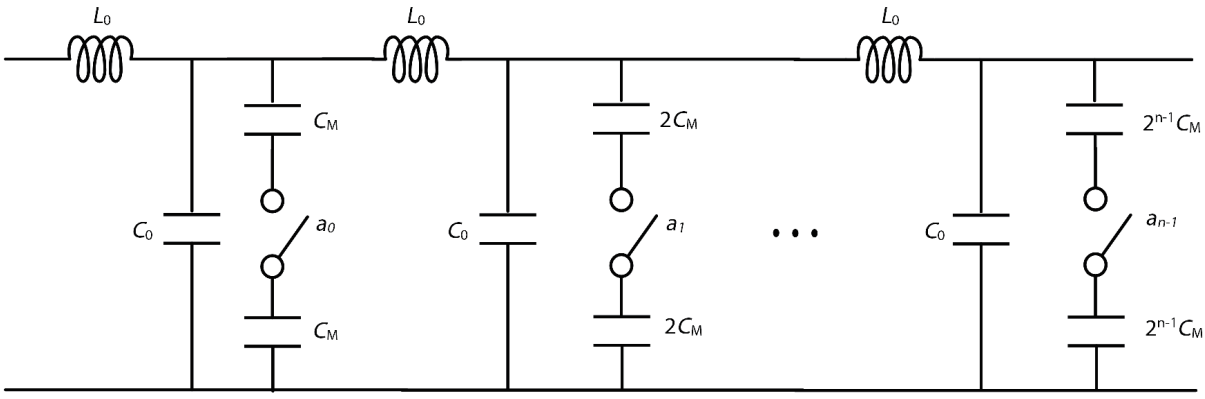


Fig. 7. The model of promoted binary-weighted DCTLs.

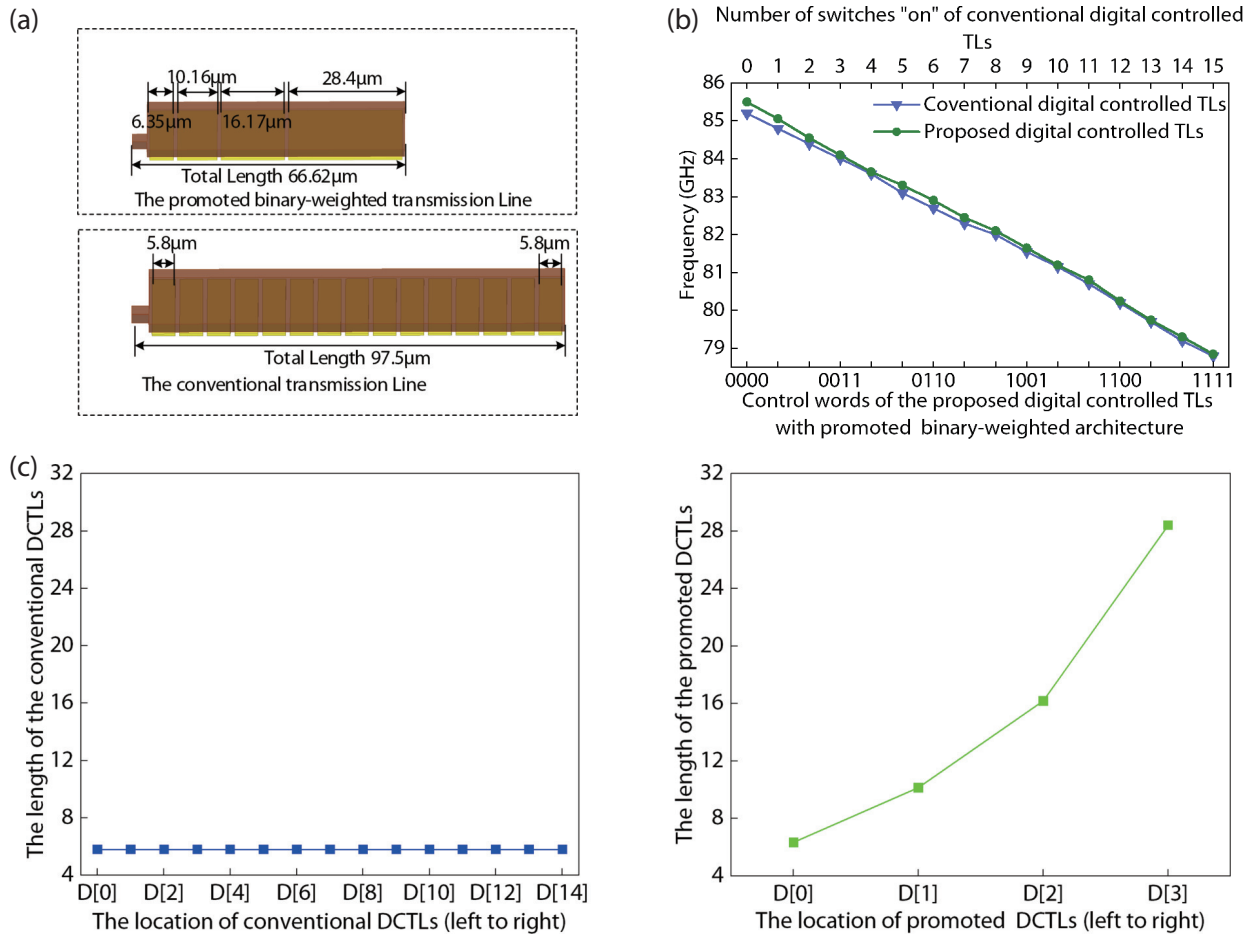


Fig. 8. (Color online) (a) Comparison of the digital-controlled TLs for CB with promoted binary-weighted architecture and the conventional digital-controlled TLs for CB. (b) Simulated tuning characteristics of the DCO with the tuning banks based on the two kinds of digital-controlled TLs mentioned above. (c) Simulated L/bit of the two kinds of DCTLs for CB.

3. Measurement results

As shown in Fig. 9, the DCO was fabricated in 40-nm CMOS. As shown in Fig. 10, the tuning word is fed into the chip's serial peripheral interface (SPI) module through a microcontroller. The SPI then converts the serial input to the parallel output, thus changing the tuning control words of DCO. The millimeter wave GSG probe is connected through the waveguide to the eighth harmonic mixer and finally to the FSUP50 spectrum analyzer.

The oscillation frequency range of the DCO is 79–85 GHz. Fig. 11 shows the measured medium-tuning curves under different coarse tuning codes. The average coarse-tuning step is about 380 MHz/bit, and the average medium-tuning step is about 33 MHz/bit. The measured fine-tuning characteristic is shown in Fig. 12. While both the control word of the MB and that of the C.B. are 0, the control word of the first four bits of the FB can achieve a frequency-tuning step of 2.8 MHz/bit, and the control word of the last four control bits of the FB can achieve a frequency-tuning step of 483 kHz/bit. This means that the tuning range of the fine-tuning bank is about 42 MHz. It is larger than the medium-tuning step of this frequency band. The tuning range of the medium-tuning bank is about 495 MHz, which is also larger than the coarse-tuning

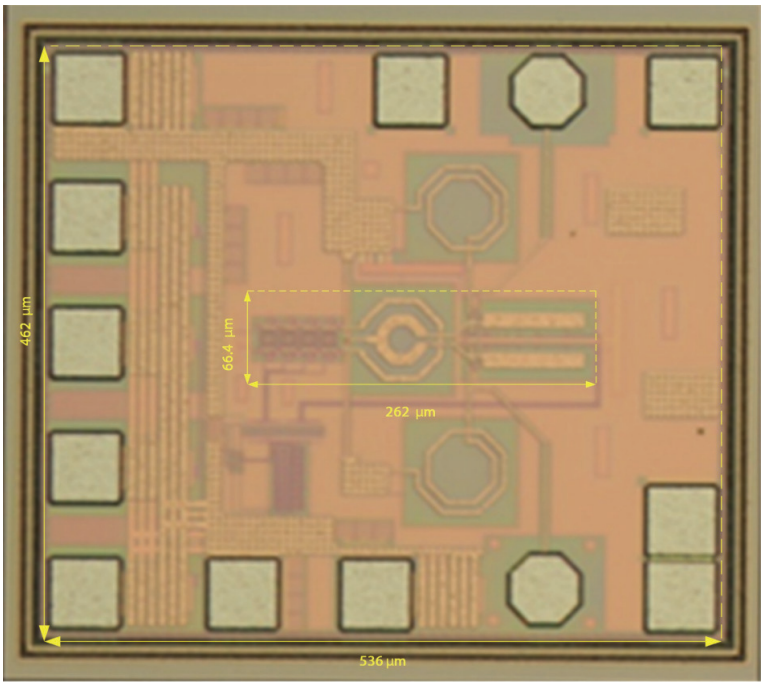


Fig. 9. (Color online) DCO chip microphotograph.

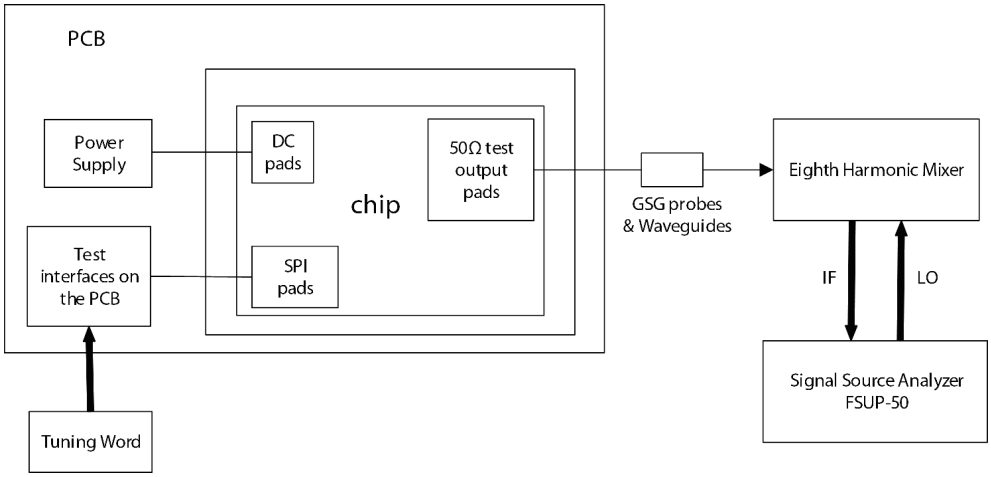


Fig. 10. Simplified schematic of phase noise measurement setup.

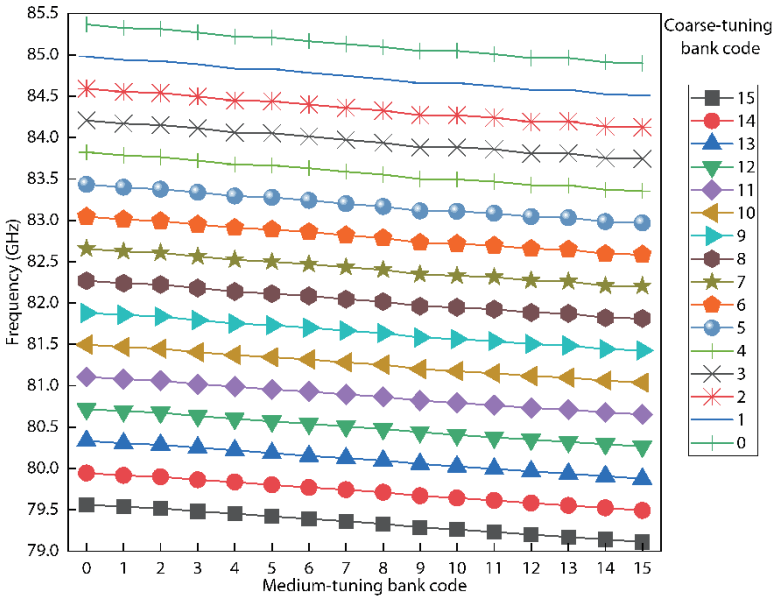


Fig. 11. (Color online) Measured medium-tuning characteristics.

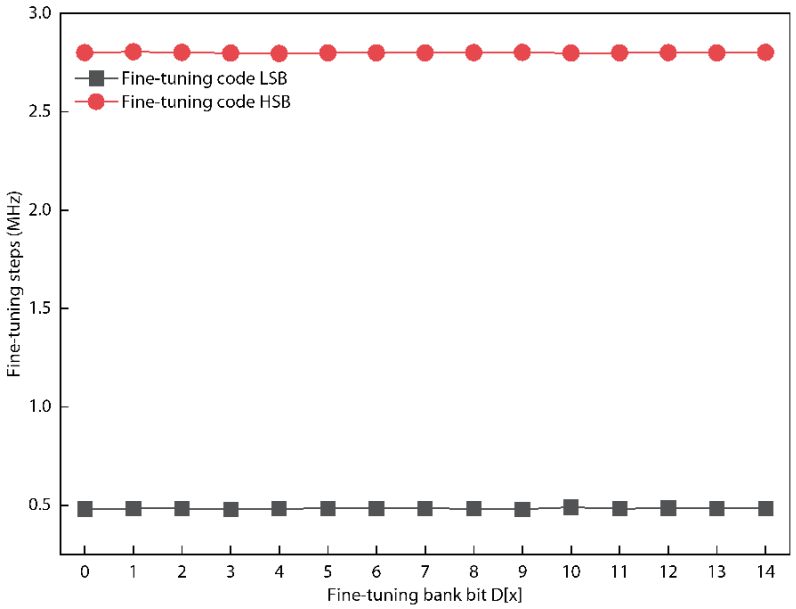


Fig. 12. (Color online) Measured fine-tuning characteristics.

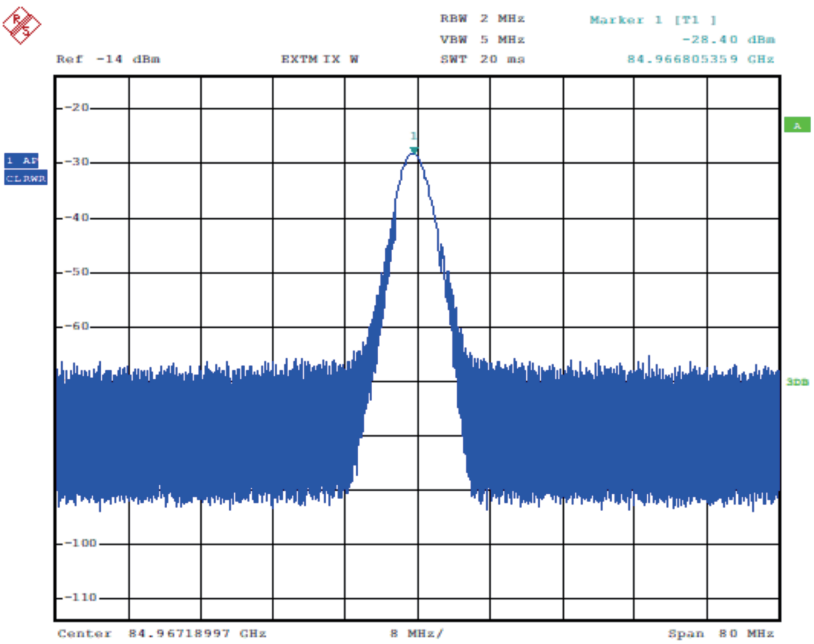


Fig. 13. (Color online) Measured DCO output spectrum.

step of this frequency band. In total, the fine-tuning range can completely cover the medium-tuning bank step, and the medium-tuning range can also completely cover the coarse-tuning bank step.

Figs. 13 and 14 show the measured spectrum and phase noise, respectively. Fig. 15 shows the measured phase noise and FoM over the whole frequency tuning range of the DCO. When the oscillation frequency is 84.6 GHz, the phase noise is −114 dBc/Hz at a 10-MHz offset. The measured phase noise of the circuit was kept at a low level under the high noise level condition. It shows the circuit performance of good anti-noise ability and high reliability. The power dissipation of the core part of the DCO is about 16 mW from 0.9 V supply voltage. During the millimeter wave measurement, the eighth harmonic mixer, the millimeter-wave GSG probe, and the RF coaxial connecting line will all introduce insertion loss and reduce the power of the oscillation signal. Therefore, the measured output power of the millimeter wave DCO is −28 dBm.

Table 1 shows the performance comparison between the DCO implemented in this work and previous works. Excellent normalized figure of merit (FoM)[16] and normalized figure of merit with area (FoM_A)[17] are achieved considering the chip area.

4. Conclusion

An 80-GHz DCO with the modified hybrid tuning banks is investigated and fabricated in 40 nm CMOS for better trade-offs among chip size, frequency resolution, oscillation frequency, and phase noise. The SC ladder based on the SC unit stages with improved circuit topology and the promoted binary-weighted DCTLs are incorporated into the tuning

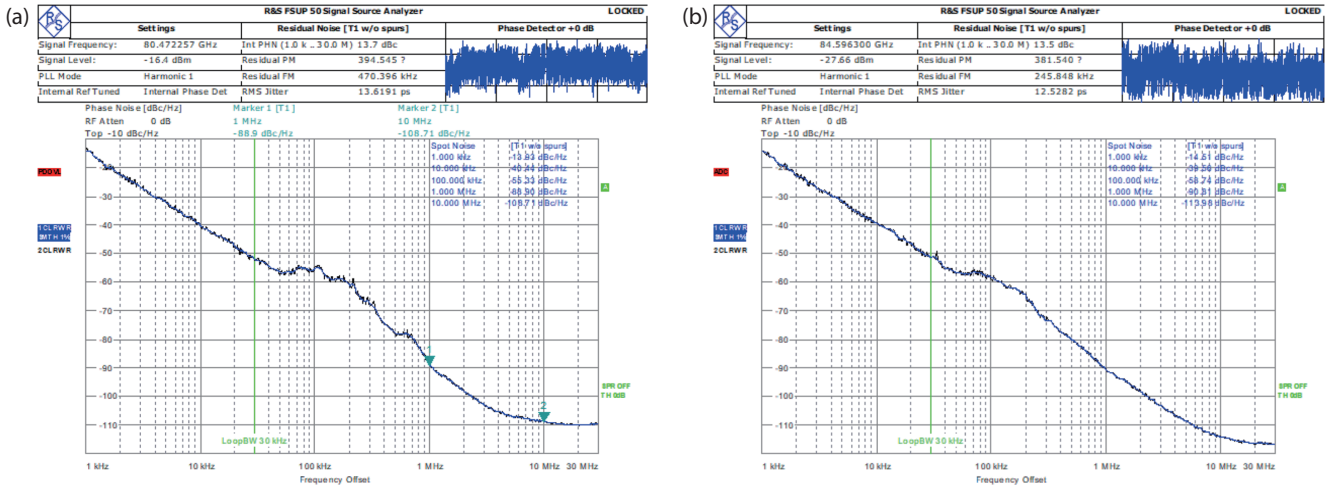


Fig. 14. (Color online) Measured DCO phase noise at (a) 80.47 GHz and (b) 84.59 GHz.

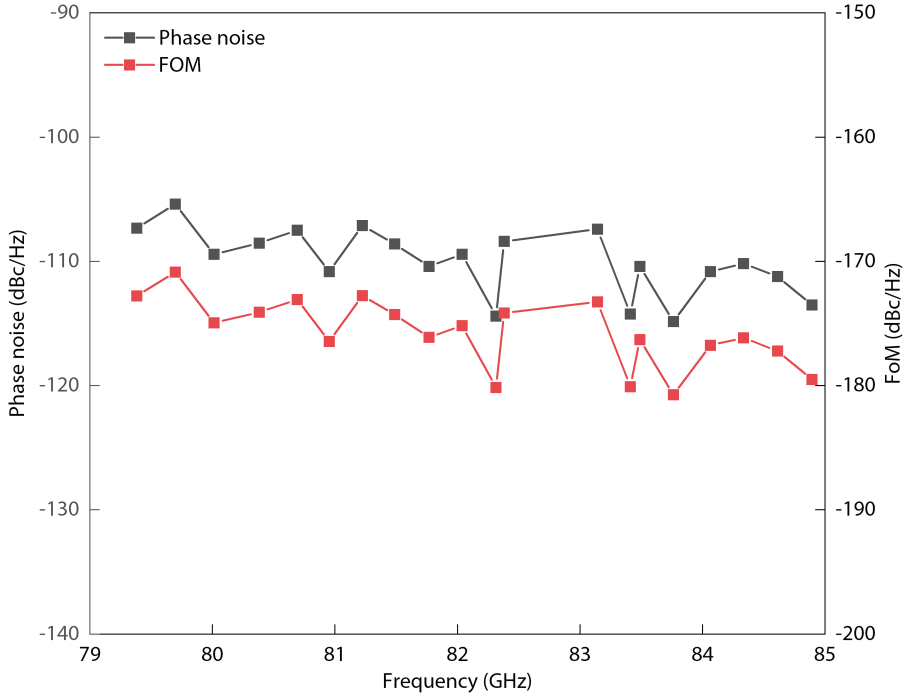


Fig. 15. (Color online) Measured phase noise and FoM over the whole frequency tuning range of the DCO.

Table 1. Performance comparison.

Parameter	Ref. [14]	Ref. [16]	Ref. [18]	Ref. [19]	This work
Technology	65-nm CMOS	90-nm CMOS	28-nm CMOS	0.13-μm CMOS	40-nm CMOS
Center frequency (GHz)	59	40.5	62.35	91	82
Phase noise (dBc/Hz)	−90.7[a]	−109[b]	−91[a]	−87[a]	−114[b]
Tuning range	54.79–63.16	52.2–61.3	57.5–67.2	90.77–91.23	79.3–84.9
Resolution (MHz)	0.3	0.024	3	–	0.5
Supply voltage (V)	1.2	0.7	1.05	1.8	0.9
P_{DC} (mW)	18	19	10.5	46	16
Area (mm^2)	0.1	0.075	0.155	0.3	0.017
FoM (dBc/Hz)[c]	−169	−168.9	−175.8	−169.6	−180.2
FoM_A (dBc/Hz)[d]	−179	−180.1	−183.9	−174.8	−198

[a] at $\Delta f = 1$ MHz, [b] at $\Delta f = 10$ MHz,

[c] $FoM = L(\Delta f) - 20\log(f_o/\Delta f) + 10\log(P_{DC}/1\text{ mW})$,

[d] $FoM_A = FoM - 10\log(\text{Area}/1\text{ mm}^2)$.

bank of the DCO. The oscillation frequency range of the DCO covers 79–85 GHz. The modified DCO exhibits an excellent FoM_A of −198 dBc/Hz compared to previous works. The DCO also achieves a high-frequency resolution of 483 kHz.

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References

[1] Li C C, Yuan M S, Liao C C, et al. A compact transformer-based fractional-N ADPLL in 10-nm FinFET CMOS. IEEE Trans Circuits Syst I Regul Pap, 2021, 68, 1881

[2] Tzeng C W, Huang S Y, Chao P Y. Parameterized all-digital PLL architecture and its compiler to support easy process migration. IEEE Trans Very Large Scale Integr VLSI Syst, 2014, 22, 621

[3] Tsai C H, Zong Z W, Pepe F, et al. Analysis of a 28-nm CMOS fast-lock Bang-Bang digital PLL with 220-fs RMS jitter for millimeter-wave communication. IEEE J Solid-State Circuits, 2020, 55, 1854

[4] Zhang C, Xu Y X, Ji S J, et al. A design of DCO with 73.1% frequency tuning range based on switched transformer. 2020 IEEE MTT-S International Wireless Symposium (IWS), 2021, 1

[5] Yang F, Wang R H, Liu X Z, et al. A high frequency resolution digitally controlled oscillator with differential tapped inductor. 2015 IEEE International Symposium on Circuits and Systems (ISCAS), 2015, 165

[6] Huang Z Q, Luong H C. A dithering-less 54.79-to-63.16GHz DCO with 4-Hz frequency resolution using an exponentially-scaling C-2C switched-capacitor ladder. 2015 Symposium on VLSI Circuits (VLSI Circuits), 2015, C234

[7] Huang Z Q, Luong H C. An 82–107.6-GHz integer-*N* ADPLL employing a DCO with split transformer and dual-path switched-capacitor ladder and a clock-skew-sampling delta–sigma TDC. IEEE J Solid-State Circuits, 2019, 54, 358

[8] C. Venerus and I. Galton. A TDC-Free Mostly-Digital FDC-PLL Frequency Synthesizer With a 2.8-3.5 GHz DCO. IEEE J Solid-State Circuits, 2015, 50(2), 45

[9] Wu W H, Staszewski R B, Long J R. A 56.4-to-63.4 GHz multi-rate all-digital fractional-N PLL for FMCW radar applications in 65 nm CMOS. IEEE J Solid-State Circuits, 2014, 49, 1081

[10] Lin C M, Kao K Y, Lin K Y. A wideband, low-noise, and high-resolution digitally-controlled oscillator for SDR applications. 2018 Asia-Pacific Microwave Conference (APMC), Kyoto, Japan, 2019, 270

[11] Mostafa P, Chatterjee S. A ditherless 2.4GHz high resolution LC DCO. 2019 2nd International Conference on Innovations in Electronics, Signal Processing and Communication (IESC), 2019, 279

[12] Xu N, Rhee W, Wang Z H. A 2 GHz 2 Mb/s semi-digital 2^+-point modulator with separate FIR-embedded 1-bit DCO modulation in 0.18 μm CMOS. IEEE Microw Wirel Compon Lett, 2015, 25, 253

[13] Ullah F, Liu Y, Wang X S, et al. Bandwidth-enhanced differential VCO and varactor-coupled quadrature VCO for mmWave applications. AEU Int J Electron Commun, 2018, 95, 59

[14] Huang Z Q, Luong H C. Design and analysis of millimeter-wave digitally controlled oscillators with C-2C exponentially scaling switched-capacitor ladder. IEEE Trans Circuits Syst I Regul Pap, 2017, 64, 1299

[15] Wu W H, Long J R, Staszewski R B. High-resolution millimeter-wave digitally controlled oscillators with reconfigurable passive resonators. IEEE J Solid-State Circuits, 2013, 48, 2785

[16] Lu T Y, Yu C Y, Chen W Z, et al. Wide tunning range 60 GHz VCO and 40 GHz DCO using single variable inductor. IEEE Trans Circuits Syst I Regul Pap, 2013, 60, 257

[17] Yu S, Kinget P R. Scaling LC oscillators in nanometer CMOS technologies to a smaller area but with constant performance. IEEE Trans Circuits Syst II Express Briefs, 2009, 56, 354

[18] Zong Z R, Chen P, Staszewski R B. A low-noise fractional: Digital frequency synthesizer with implicit frequency tripling for mm-wave applications. IEEE J Solid-State Circuits, 2018, 54, 755

[19] Tarkeshdouz A, Mostajeran A, Mirabbasi S, et al. A 91-GHz fundamental VCO with 6.1% DC-to-RF efficiency and 4.5 dBm output power in 0.13-μm CMOS. IEEE Solid-State Circuits Lett, 2018, 1, 102

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