ARTICLES

Journal of Semiconductors
(2023) 44, 102401
doi: 10.1088/1674-4926/44/10/102401

Exploration of high-speed 3.0 THz imaging with a 65 nm CMOS process

Min Liu[1, 2], Ziteng Cai[1, 3], Jian Liu[1, 2], Nanjian Wu[1, 2], and Liyuan Liu[1, 2, †]

[1]State Key Laboratory of Superlattices and Microstructures, Institute of Semiconductors, Chinese Academy of Sciences, Beijing 100083, China
[2]Center of Materials Science and Optoelectronics Engineering, University of Chinese Academy of Sciences, Beijing 100049, China
[3]Faculty of Information Technology, Beijing University of Technology, Beijing 100124, China

Abstract: This paper describes a promising route for the exploration and development of 3.0 THz sensing and imaging with FET-based power detectors in a standard 65 nm CMOS process. Based on the plasma-wave theory proposed by Dyakonov and Shur, we designed high-responsivity and low-noise multiple detectors for monitoring a pulse-mode 3.0 THz quantum cascade laser (QCL). Furthermore, we present a fully integrated high-speed 32 × 32-pixel 3.0 THz CMOS image sensor (CIS). The full CIS measures 2.81 × 5.39 mm^2 and achieves a 423 V/W responsivity (Rv) and a 5.3 nW integral noise equivalent power (NEP) at room temperature. In experiments, we demonstrate a testing speed reaching 319 fps under continuous-wave (CW) illumination of a 3.0 THz QCL. The results indicate that our terahertz CIS has excellent potential in cost-effective and commercial THz imaging and material detection.

Key words: power detectors; quantum cascade laser (QCL); CMOS image sensor (CIS); terahertz

Citation: M Liu, Z T Cai, J Liu, N J Wu, and L Y Liu, Exploration of high-speed 3.0 THz imaging with a 65 nm CMOS process[J]. *J. Semicond.*, 2023, 44(10), 102401. https://doi.org/10.1088/1674-4926/44/10/102401

1. Introduction

Terahertz (THz) waves fall between millimeter waves and far-infrared waves in the electromagnetic spectrum, whose frequency range (0.1–10 THz) is the so-called terahertz gap due to the lack of effective generation and detection in this regime. Terahertz waves can penetrate numerous non-metallic and non-polar materials, which have specific spectral fingerprints for many substances, and offer strong water absorbency. Compared to mm-wave radiation, THz radiation can achieve higher spatial resolution. Unlike X-ray radiation[1–4], THz radiation causes no harm to biological tissues. In addition, THz radiation can detect hidden objects compared to infrared radiation. Due to these unique characteristics, THz sensing and imaging have drawn particular attention in security screening[5], biosensing[6] and non-destructive testing (NDT) applications[7–9].

Since plasma-wave theory[10] was first proposed by the Dyakonov and Shur group in the early 1990s, research on silicon-based THz detectors and imagers has experienced tremendous progress, particularly in the sub-THz domain[11–17] (frequency below 1 THz). However, the higher terahertz frequency range (>1 THz), providing a particular sought-after convenience in high-resolution imaging applications of industrial defect detection and chemical and biomedical sensing, remains to be further explored.

With the sustainable development of THz quantum cascade lasers (QCLs)[18–21], the peak radiated power can reach 2 W with a single-mode 3 THz band[20]. Such powerful THz QCLs can counteract heavy atmospheric absorption[22, 23] and provide a feasible means for THz real-time imaging. The mainstream silicon-based CMOS process, which is easy to integrate, being low-cost and high-yield, is well appropriated by multipixel integration and CMOS image sensor (CIS) fabrication in the industry. To our knowledge, a significant number of CMOS terahertz detectors[24–28] at frequencies above 1 THz depend on the aid of external commercial amplifiers and ADCs to process the analog output from a chip[25–27] or integrate low-resolution in-pixel amplifiers[28]. Unfortunately, most of them have poor sensitivity or complex systems, which dramatically hinders the development of compact and miniaturized CISs.

Here, we focus on terahertz detection and imaging with silicon devices in the standard 65 nm CMOS process. First, we explored detectors with various resonance frequencies and monitored a 3.0 THz QCL working in pulse mode. Then, we selected the optimal detector and implemented a fully integrated 3.0 THz CMOS image sensor in a monolithic chip for real-time imaging. An optimal responsivity (Rv) of 423 V/W and a minimum integral noise equivalent power (NEP) of 5.4 nW in video mode were reported. In experimental tests, the imaging speed rate reached 319 fps under CW illumination of the 3.0 THz QCL. This exploration shows that our CIS has promising potential in commercial THz imaging and industrial detection. This paper is organized as follows: Section 2 describes the detection mechanism, detector implementation and characterization. Section 3 assesses the proposed high-speed 3.0 THz CIS, followed by a conclusion in Section 4.

2. THz detection with multiple CMOS terahertz detectors

2.1. Theoretical analysis

Since the Dyaknov and Shur group[10] proposed the potential of plasma-wave-induced rectification in field-effect transistors (FETs), there has been prime interest in using FETs for DC

Correspondence to: L Y Liu, liuly@semi.ac.cn
Received 24 JANUARY 2023; Revised 23 MARCH 2023.

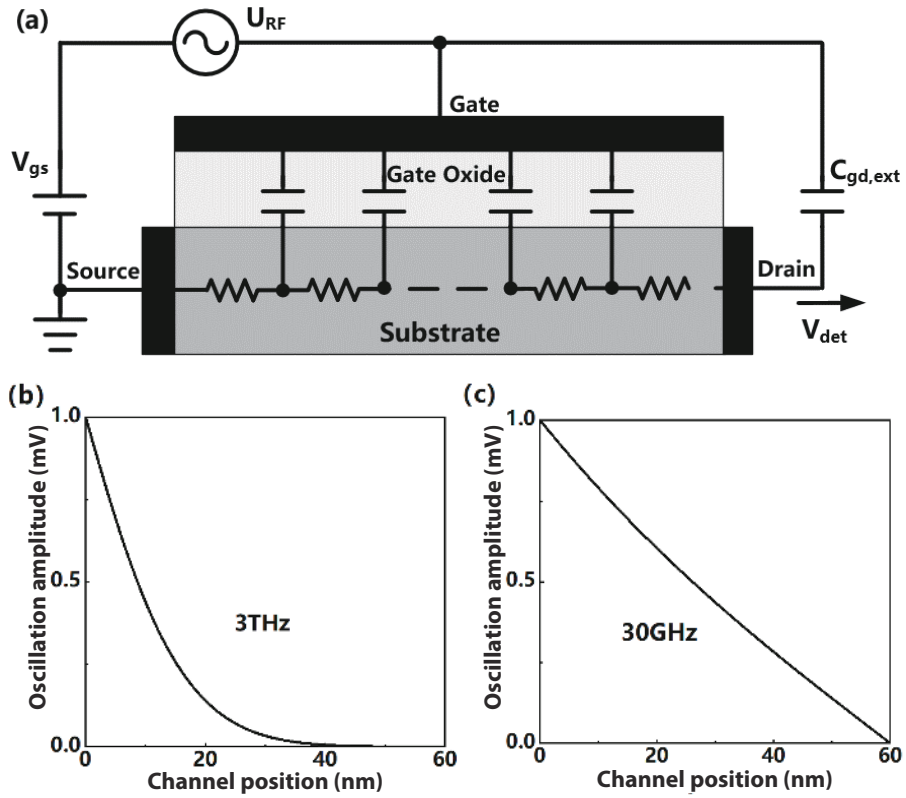

Fig. 1. (a) NQS RC-ladder model, (b) spatial evolution of carrier oscillation amplitude at excitation of 3.0 THz and (c) spatial evolution of carrier oscillation amplitude at excitation of 30 GHz.

power detection[29–33] in recent years. At low frequencies, square-law power detection can be described as a typical quasistatic (QS) resistive mixing procedure. The DC current response I_{det} or DC voltage response V_{det} extracted can be expressed as

$$I_{det} = \frac{\mu C_{ox} \cdot (W/L) \cdot V_a^2}{4}, \tag{1}$$

or

$$V_{det} = \frac{V_a^2}{4 \cdot (V_{gs} - V_{TH})}, \tag{2}$$

where W/L refers to the aspect ratio of the FET, μ is the carrier mobility, C_{ox} is the oxide capacitance per unit area, V_a is the amplitude of the received THz signal, V_{gs} is the gate-to-source voltage, and V_{TH} is the threshold voltage.

However, in the THz frequency range well above the cutoff frequency of an FET, the above low-frequency approximation is no longer active, and a nonquasistatic (NQS) description could be a substitute. The FET power detection mechanism in the THz frequency range is summarized as an NQS RC ladder model (shown in Fig. 1(a)). At higher frequencies (i.e., 3.0 THz), the FET motion at a specific position x acts in a nonresonant manner. It can be defined as the following simplified classic Euler equation of action and the continuity equation[29, 33]:

$$\frac{v(x,t)}{\tau} + \frac{e}{m}\frac{\partial U(x,t)}{\partial x} = 0, \tag{3}$$

$$\frac{\partial U(x,t)}{\partial t} + \frac{\partial (U(x,t) \cdot v(x,t))}{\partial x} = 0, \tag{4}$$

where $v(x, t)$ is the local drift electron velocity in the channel and $U(x, t)$ is the electrical potential along the channel. τ is the momentum relaxation time, $\tau = \mu m/e$, e is the elementary charge, and m is the effective transport mass. The boundary condition of the FET is as follows:

$$U(0,t) = (V_{gs} - V_{TH}) + V_a \cos\omega t, \tag{5}$$

$$J(L,t) = 0, \tag{6}$$

with radiated THz frequency ω, current density per width length $J(x, t)$, location in channel x, and time t. The current density determines the local drift velocity:

$$J(x,t) = ne \cdot v(x,t), \tag{7}$$

where the unified electron concentration n is related to the local gate-to-source voltage and subthreshold ideality factor η:

$$n = \frac{C_{ox}\eta V_{TH}}{e} \cdot \ln\left(1 + \frac{1}{2}\exp((V_{gs} - V_{TH})/\eta V_{TH})\right). \tag{8}$$

For $V_a \ll (V_{gs} - V_{TH})$, a DC potential could be extracted from the drain terminal according to Eqs. (3)–(8).

Fig. 1(b) shows a 3.0 THz numerical solution of the position-dependent gate-to-channel voltage $U(x,t)$ in the NQS regime in a 65 nm NMOS device. Suppose a bias $V_{gs} - V_{th} = 0.1$ V, a carrier mobility of 0.035 $m^2/(V{\cdot}s)$ and a received signal amplitude $V_a = 1$ mV. The time-harmonic THz radiation sig-

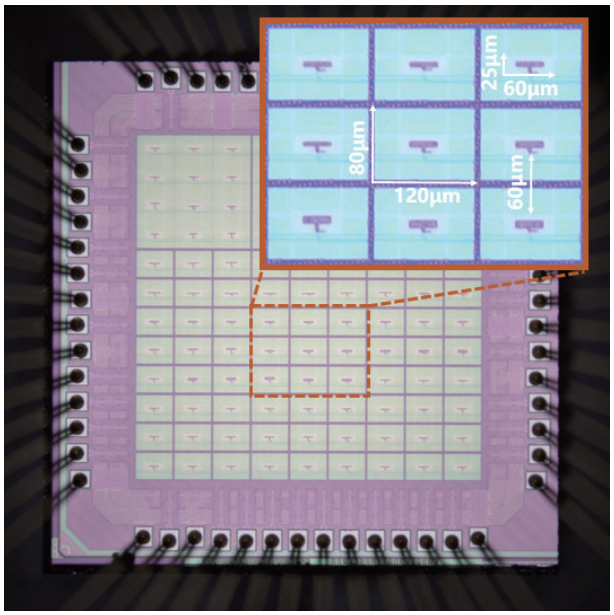

Fig. 2. (Color online) Micrograph of a 1.5 × 1.5 mm^2 silicon die showing different detectors with variable-sized patch antennas. A close-up photograph gives nine detectors of different resonant frequencies. Chip photograph reproduced from Refs. [24, 25].

nal V_a·cos(ωt) propagates through the channel and decays over a distance to zero before reaching the drain contact. For comparison purposes, Fig. 1(c) exhibits the numerical solution for 30 GHz. Unlike the 3.0 THz FET, the whole FET at 30 GHz can be regarded as a lumped element, and its motion acts in a quasistatic (QS) manner.

It is evident that effective plasma oscillation in the higher THz frequency band occurs near the FET source, while the remaining source–drain channel is considered to have parasitic distributed capacitances and resistances. A short channel device is usually adopted to weaken the inner parasitic part to obtain a THz-detecting unit with lower thermal noise and better responsivity.

2.2. Detector implementation

To facilitate the evaluation of individual power detectors, we arranged 12 × 9 detectors in a monolithic chip where the resonant frequency of the detectors spans from 2.0 to 3.3 THz. Fig. 2 shows a micrograph of the wire-bonded CMOS terahertz detectors with 120 × 80 μm^2 per pitch. Each detector is equipped with a half-wavelength single-end patch antenna coupled to a FET-based NMOS device. To suppress the antenna coupling effect, the space between adjacent antenna planes is 60 μm from one to another.

The detector model using the standard 65 nm CMOS 1P9M process is illustrated in Fig. 3. The patch antenna transmits the received terahertz signal to the source of a common-gate NMOS device through the microstrip line TL1 along with the via layers. When an external gate bias voltage V_g is applied, the coupled drain terminal will read out a DC signal U_d proportional to the received terahertz energy.

In this work, we select top metal M9 as the patch plane and M1 as the ground plane. There are two via layers. One joint is the center of the patch plane to the ground plane, providing a DC path and minimizing the substrate incurred losses. The other and TL1 serve as a matching network (MN) that matches the patch antenna and NMOS device. The

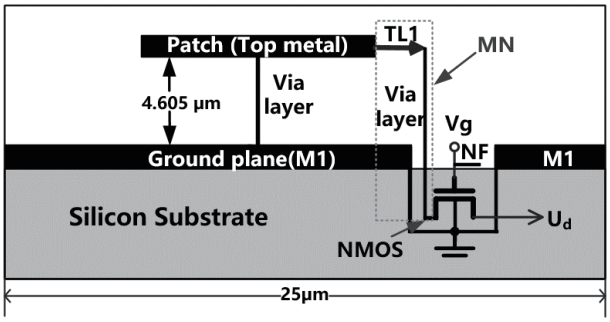

Fig. 3. Detector model: cross-section illustrating the patch-antenna-coupled NMOS device for THz detection. The ground plane size is 60 × 25 μm^2. The dielectric distance is 4.605 μm.

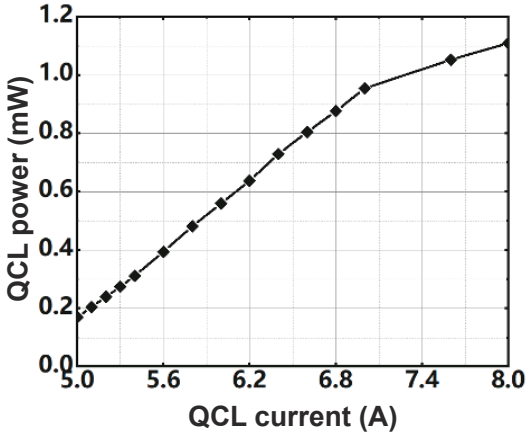

Fig. 4. QCL power versus different pulse currents. The QCL power is measured with the 3A-P-THz absolute power meter.

notch filter (NF) is inserted into the gate terminal to filter the parasitic influences of the external power supply. The NMOS device, with a 120 nm channel length and a 60 nm gate width, is selected for better responsivity values. By adjusting the size of the patch plane and TL1, we can obtain various detectors with different resonant frequencies. No amplifiers or other components are employed to avoid additional noise.

2.3. Detector characteristics

We prepare a current-controlled pulse QCL to generate a 3.0 THz frequency signal. Fig. 4 illustrates the QCL radiated power as a function of the current. When an 8 A current pulse drives the QCL with a 1% duty cycle, its radiation power is up to 1.1 mW. The measured QCL power exhibits an approximately linear dependence on currents. Meanwhile, our detector D14 indicates the detected voltage response under various drive currents (shown in Fig. 5). As the QCL current increases, the radiated frequency slightly deviates from 3.0 THz, thus yielding a variable gate bias to obtain an optimal response. While the QCL is operated at 8 A, the voltage response cannot keep up with the increased QCL power, and the detector tends to be saturated.

We adopt classic lock-in techniques[24, 25] to measure the voltage and noise response. The measured results for voltage responses of three different detectors versus gate bias are plotted in Fig. 6. A laser diode/temperature controller (Thorlabs. ITC4020)[34] provides a 5 kHz, 1% duty cycle pulse signal to the 3.0 THz QCL source. Maximum voltage responses are obtained in the subthreshold region where the

Table 1. Parameters and measured results of partial FET-based detectors.

Detector[1]	Patch size (μm^2)	TL1 (μm^2)	Resonant frequency (THz)	Directivity (dBi)	Max. voltage response (mV)	Responsivity[2] (V/W)	NEP ($pW/Hz^{1/2}$)	SNR (dB)
D88	30 × 8	4.2 × 2	2.80	3.50	2.72@0.79 V	422	189	90
D13	30 × 2	6.0 × 2	2.85	3.11	2.13@0.27 V	374	56	100
D95	30 × 7	4.5 × 2	2.89	3.12	2.93@0.19 V	528	174	90
D14	30 × 2	5.5 × 2	2.94	2.75	2.59@0.23 V	526	123	92
D15	30 × 2	5.0 × 2	3.04	2.29	2.56@0.16 V	618	139	89
D72	30 × 4	4.5 × 2	3.04	2.37	3.35@0.16 V	791	245	84
D55	20 × 2	6.0 × 2	3.11	3.79	4.15@0.21 V	741	174	90
D36	25 × 2	5.0 × 2	3.16	2.22	3.22@0.13 V	855	71	94
D16	30 × 2	4.0 × 2	3.25	1.88	3.02@0.18 V	915	39	98

[1] Dxy refers to the detector in the x-th row and y-th column.

[2] The responsivity is estimated according to the raster-scanning source beam with D14.

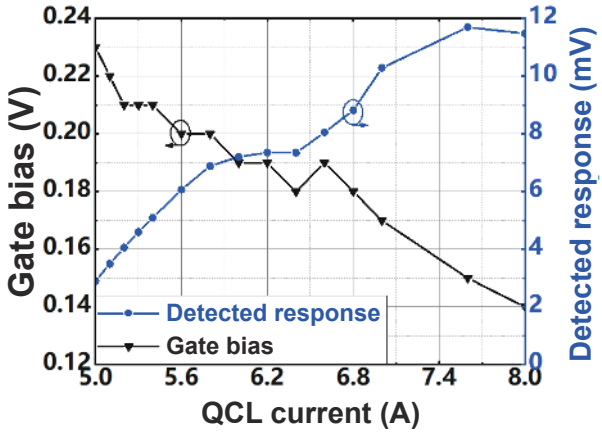

Fig. 5. (Color online) Detected maximum voltage response and its corresponding gate bias at different pulse currents. Detector in the first row and the fourth column D14 was selected for analysis.

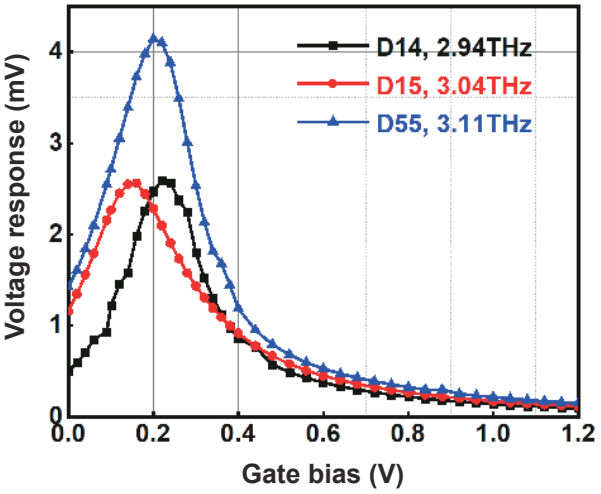

Fig. 6. (Color online) Measured voltage response of three different detectors with QCL illumination. The detector in the x-th row and the y-th column is expressed as Dxy.

noise responses are also remarkable, as shown in Fig. 7. The bias partly dictates the detector's signal-to-noise ratio (SNR).

QCLs are the most popular THz emission sources at higher THz frequencies beyond 3 THz. They are powerful and narrow-band, providing an opportunity for THz detection and imaging but also a challenge for electronics and electromagnetic design in this band. Most often, resonant frequencies of

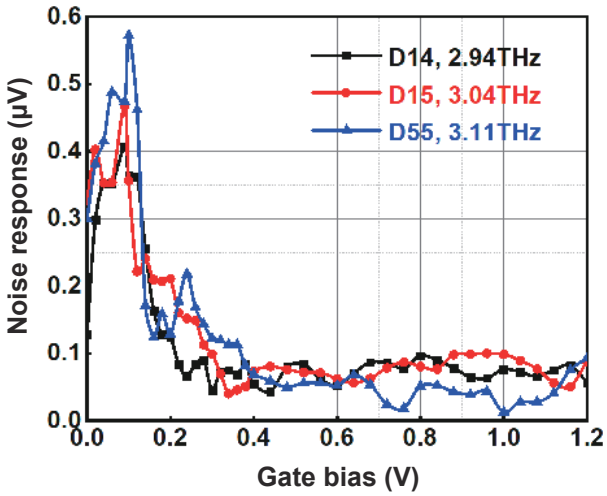

Fig. 7. (Color online) Measured noise response of three different detectors without QCL illumination. The detector in the x-th row and the y-th column is expressed as Dxy.

the actual fabricated antenna-coupled detectors deviate from the original designs. It is essential to achieve the optimal detector to better monitor the THz QCL and fabrication for our further 3.0 THz multipixel CIS.

Table 1 summarizes the parameters and measured results of nine different detectors for monitoring the 3.0 THz QCL described above. Apparently, at higher frequencies, the physical length of an antenna differs from its theoretical electrical length in our design. Moreover, the detector is sensitive to patch scaling and microstrip TL1. D13, D14, D15 and D16 have the same patch size but varying TL1. Their resonant frequencies are 2.85, 2.94, 3.04 and 3.25 THz, respectively. D95 and D72 have the same TL1 size, while their patch sizes are slightly different, creating a 150 GHz resonant frequency difference. Interestingly, we find that D15 and D72 have different patch sizes and TL1 sizes but have the same resonant frequency. Moreover, D72, which has higher directivity, yields a higher voltage response.

In this section, D55 achieves an optimal 4.15 mV voltage response and an outstanding 3.79 dBi directivity value. Therefore, we chose D55 for our follow-up 3.0 THz CIS design.

Its favorable resolution (i.e., 50 μm at 3.0 THz) would benefit industrial defect detection and biomedical imaging. However, raster-scan imaging using a single CMOS detector takes a long time. Our team's leaf-scanned image in Ref. [25]

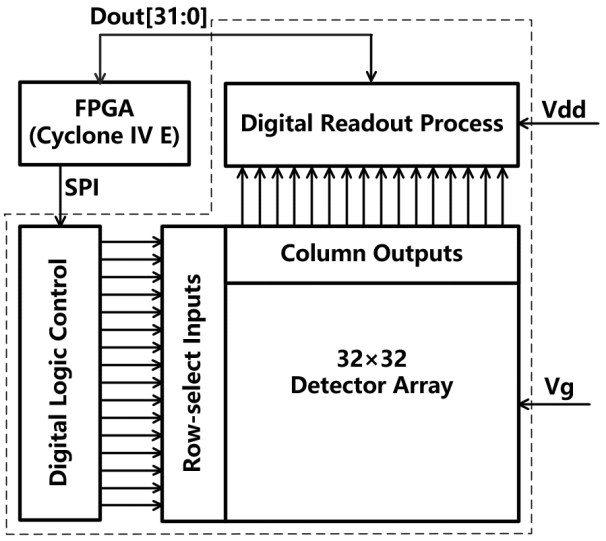

Fig. 8. Block diagram of the off-chip FPGA-controlled 32 × 32-pixel CIS.

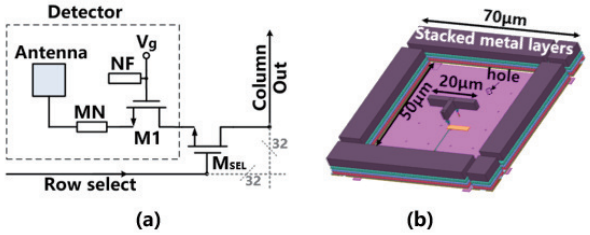

Fig. 9. (Color online) (a) Schematic of a single pixel; (b) the pixel layout model.

requires approximately 2 h, which is undesirable in the industrial market. If possible, a multipixel THz CMOS image sensor for real-time imaging should be developed.

3. A high-speed 3.0 THz digital CIS

In this contribution, we will discuss a fully compact CIS that integrates a pixel array including 1024 antenna-coupled detectors, digital readout processing (DRP)[29] modules, and a digital logic control (DLC) module into an on-chip system. With the illumination of a CW 3.0 THz QCL, the CIS demonstrates real-time imaging capability and achieves a high-speed rate of 319 fps.

3.1. CIS architecture

Our CIS employs the high-parallelism readout processing architecture[15, 29, 35, 36] to effectively and quickly process and read out the detector responses. Fig. 8 shows the block diagram of the CIS. The pixel array operates in rolling-shutter mode and outputs the DC detected signals (one full 32-pixel row) row by row. The 32-column analog outputs are concurrently processed by DRPs and then converted to a digital bit stream for off-chip FPGA processing. The DLC module drives the row-select inputs.

The designed detector is D55, selected from Section 2. Fig. 9(a) displays the schematic of a single-pixel circuit. It mainly consists of a half-wavelength single-end patch antenna, a matching network MN, a detecting NMOS device M1, a notch filter NF and an additional transistor switches M_{SEL}. One row-select line controls 32-column pixels by

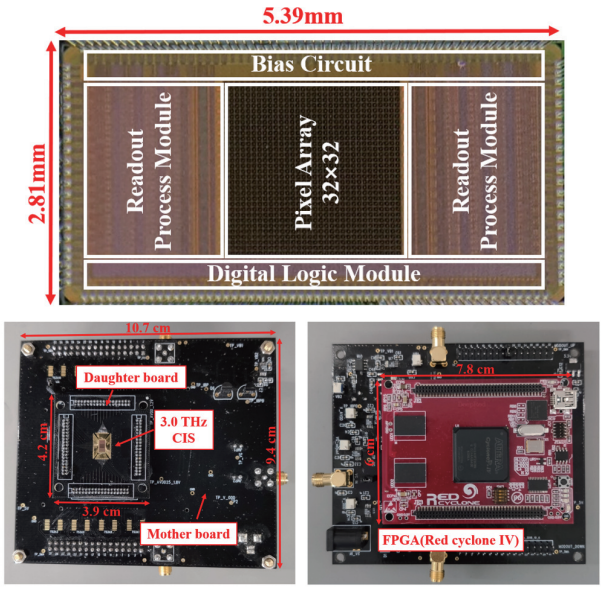

Fig. 10. (Color online) Chip die microphotograph (upper panel). The front side and the back side (lower panel) of testing PCB for the 3.0 THz CIS.

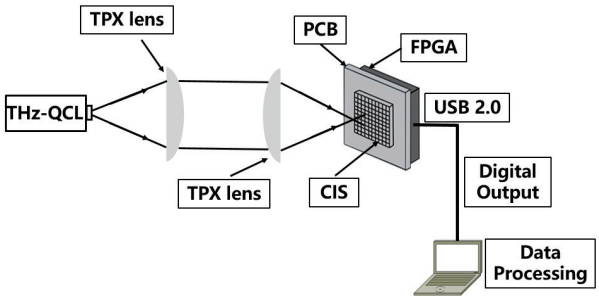

Fig. 11. Measurement setup for characterizing the CIS.

switches (M_{SEL}), while the column bus reads out the detected outputs synchronously.

The ground plane of the pixel layout in Fig. 9(b) occupies a 50 × 50 μm^2 area that violates design rule checking (DRC) due to unreleased stress. Moreover, no other metals exist between the patch and ground planes, thus introducing metal density issues. Those omitted design rules may inevitably influence the yield of the fabricated detector array. To address these issues, 10 μm-wide metal layers are stacked around the ground plane for stress release; slots are employed for metal density requirements.

3.2. CIS performance

The CIS structures a monolithic system that fully integrates the 1024 pixels and DRP modules. It is fabricated in 65 nm standard CMOS technology on a 2.81 × 5.39 mm^2 silicon die (see Fig. 10). The pixel array occupies a 1.92 × 1.92 mm^2 area with a single pitch of 60 × 60 μm^2. At the same time, one readout process module possesses a 1.92 × 1.36 mm^2 area. All circuits operate under 1.2 V. At the same time, the printed circuit board (PCB) bonds our sensor and connects off-chip FPGA for a compact experimental system.

Fig. 11 illustrates the measurement setup for CIS characterization. All are measured under the CW illumination of a 3.0 THz QCL. The THz frequency power generated by the QCL is focused and collimated to the pixel array via two TPX lenses.

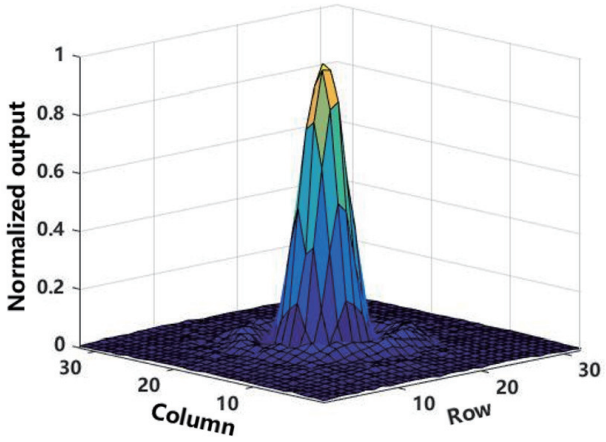

Fig. 12. (Color online) Image of the normalized 3.0 THz QCL beam in video mode.

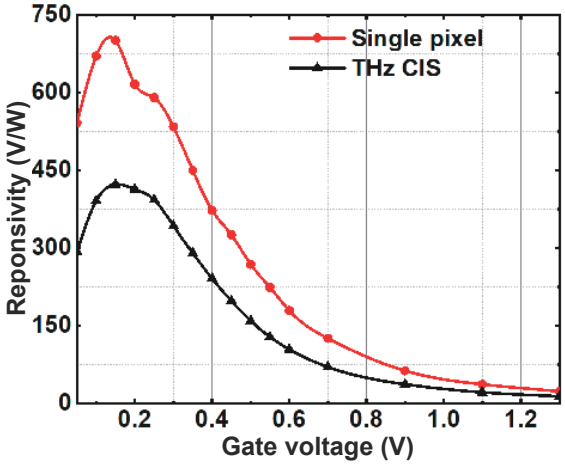

Fig. 13. (Color online) Measured responsivity of single pixel and CIS versus gate-bias voltage.

Subsequently, the detected signal is converted to a digital signal and sent to an off-chip FPGA for processing. The CIS is placed slightly out-of-focus to capture a more homogeneous source beam.

Typically, the single-pixel responsivity can be calculated via the pixel response U_{out} divided by the power incident to the on-chip pixel P_{in} [24, 37]

$$R_{\text{v,s}} = \frac{U_{\text{out}}}{P_{\text{in}}} = \gamma \cdot \frac{\sum_{i=1}^{1024} U_i \cdot A_{\text{pix}}}{P_{\text{beam}} \cdot A_{\text{eff}}}, \tag{9}$$

where U_i is the output value of the i_{th} pixel, γ is the response-relevant constant, with a measured value of 1.3, P_{beam} is the available source beam power in the pixel plane, A_{pix} is the physical area of a single pixel, A_{eff} is the effective area of a single pixel, which is determined by $A_{\text{eff}} = D\lambda^2/4\pi$, and D is the simulated directivity of the antenna.

In regard to the responsivity of pixel arrays, the calculated effective area is no longer reliable since pixels are subdiffraction-limited and pitch-fixed. We define the effective area A_{eff} as equal to the physical area A_{pix}. Therefore, the CIS responsivity in the video-rate mode can be determined by normalizing the sum of the detector responses in the pixel array area to the available source beam power P_{beam}. Fig. 12 shows the acquired image of the measured focused 3.0 THz spot. A beam power of 5 mW is measured by a free-space absolute power meter (from 3A-P-THz). The normalized voltage responsivity R_{v} of the CIS can be expressed as[12, 14]

$$R_{\text{v}} = \sum_{i=1}^{1024} U_i \Big/ P_{\text{beam}}. \tag{10}$$

Fig. 13 exhibits the bias dependence of the single-pixel responsivity and CIS responsivity, respectively. Owing to the inhomogeneity between pixels and the effective electrical area A_{eff}, our CIS achieves a video-mode responsivity value of 423 V/W at 0.15 V and a single-pixel-mode responsivity of 701 V/W at 0.15 V.

In addition, we find that the single-pixel responsivity differs from the responsivity of D55 in Section 2. The different testing QCLs and different pixel pitches mainly cause this difference.

Unlike the traditional definition of a CIS-detector NEP[14, 38, 39], we use the ratio of the root-mean-square (RMS) noise voltage U_{noise} to the voltage responsivity R_{v} as the CIS's noise figure-of-merit (FOM)[12, 40]. That is,

$$\text{NEP} = \frac{U_{\text{noise}}}{R_{\text{v}}}. \tag{11}$$

By sampling 67 frames, we calculate the standard deviation for each pixel corresponding to the RMS noise. Under the experimental tests, a minimum integral NEP of 5.4 nW at 0.25 V is obtained, as shown in the blue curve in Fig. 14.

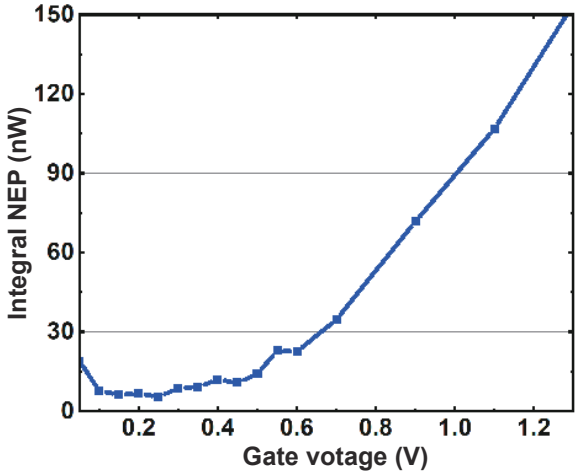

Fig. 14. (Color online) Measured CIS integral NEP dependance on gate-bias voltage.

The signal readout strategy is to perform CIS integration in rolling-shutter mode. During the row-exposure periods, the readout chains will continuously sample the output. The higher the frame rate is, the richer the acquired information, but the lower the SNR. One can lower the required samplings per frame to achieve a higher frame rate. Fig. 15 lists nine different captured source beams of various frame rates. The CIS is placed slightly out-of-focus to exhibit more diffraction rings for better comparison. Our CIS reaches a high speed of up to 319 fps with a still distinguishable image.

A performance comparison between this work and other reported THz CMOS imagers is presented in Table 2. Compared to other implementations, our CIS has a smaller pixel

Table 2. Comparison with other published CMOS imagers.

Freq. (THz)	Technology	Pixel (x×y)	Rv[1] (kV/W)	NEP (nW)	Readout chain	Frame rate (fps)	Optics	Reference
3.0	65-nm CMOS	32 × 32	423	5.4	On-chip	Max.319	None	This work
0.79–0.96	65-nm CMOS	32 × 32	562–1124	10–20	External	Max.500	Si lens	[12]
0.59	150-nm CMOS	12 × 12	348	15.2	External	16	None	[14]
0.46–0.75	130-nm CMOS	32 × 32	0.014 A/W	36	On-chip	25	Si lens	[17]
0.27–0.6	130-nm CMOS	31 × 31	272–378	0.6–0.8	On-chip	25–100	None	[41]

[1] The responsivity is a normalized value excluding gain and measured at video mode.

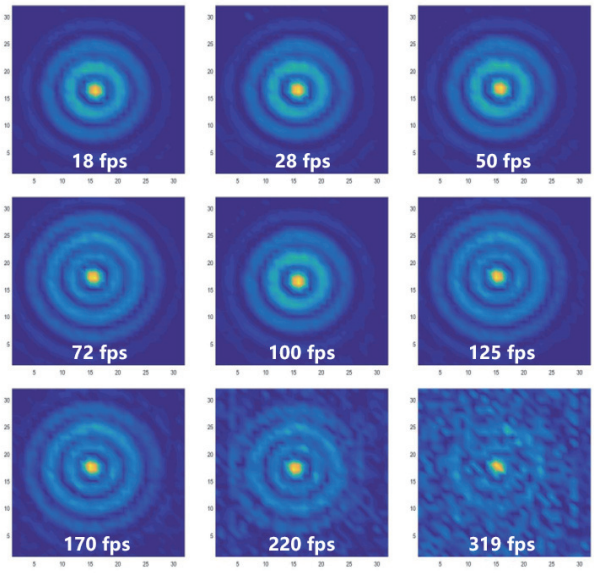

Fig. 15. (Color online) Measured source beams in different frame rate.

pitch size, better responsivity and higher speed. In addition, no optical elements or external auxiliary devices are integrated into our CIS, which is compatible with low-cost industrial multipixel THz CMOS camera fabrication.

4. Conclusions

In summary, we explored a promising route for high-speed 3.0 THz imaging. After studies on multiple detectors with different resonant frequencies for monitoring a 3.0 THz QCL, we fabricate a high-speed 3.0 THz CIS that fully integrates the monolithic pixel array and on-chip DRPs in the 65 nm CMOS process. The CIS achieves a voltage responsivity of 423 V/W and an integral NEP of 5.4 nW in video mode at room temperature. Meanwhile, our chip realizes a favorable framerate up to 319 fps. Our CIS is expected to promote further development of large-scale pixel CIS and compact THz imaging systems.

Acknowledgments

Project supported by the National Natural Science Foundation of China under Grant Nos. 61874107, 62075211.

References

[1] Su Y R, Ma W B, Yang Y M. Perovskite semiconductors for direct X-ray detection and imaging. J Semicond, 2020, 41, 051204

[2] Sun Q S, He Y Z, Liu K, et al. Recent advances in terahertz technology for biomedical applications. Quant Imaging Med Surg, 2017, 7, 345

[3] Son J H, Oh S J, Cheon H. Potential clinical applications of terahertz radiation. J Appl Phys, 2019, 125, 190901

[4] D'Arco A, Di Di Fabrizio M, Dolci V, et al. THz pulsed imaging in biomedical applications. Condens Matter, 2020, 5, 25

[5] Woolard D L, Jensen J O, Hwu R J, et al. Terahertz science and technology for military and security applications. World scinetific, 2007

[6] Brun M A, Formanek F, Yasuda A, et al. Terahertz imaging applied to cancer diagnosis. Phys Med Biol, 2010, 55, 4615

[7] Zhang H, Sfarra S, Saluja K, et al. Non-destructive investigation of paintings on canvas by continuous wave terahertz imaging and flash thermography. J Nondestruct Eval, 2017, 36, 34

[8] Kawase K, Shibuya T, Hayashi S, et al. THz imaging techniques for nondestructive inspections. Comptes Rendus Physique, 2010, 11, 510

[9] Steyaert W, Reynaert P. A THz signal source with integrated antenna for non-destructive testing in 28nm bulk CMOS. 2015 IEEE Asian Solid-State Circuits Conference (A-SSCC), 2016, 1

[10] Dyakonov M, Shur M. Shallow water analogy for a ballistic field effect transistor: New mechanism of plasma wave generation by dc current. Phys Rev Lett, 1993, 71, 2465

[11] Ojefors E, Pfeiffer U R, Lisauskas A, et al. A 0.65 THz focal-plane array in a quarter-micron CMOS process technology. IEEE J Solid State Circuits, 2009, 44, 1968

[12] Al Hadi R, Sherry H, Grzyb J, et al. A 1 k-pixel video camera for 0.7–1.1 terahertz imaging applications in 65-nm CMOS. IEEE J Solid State Circuits, 2012, 47, 2999

[13] Kim D Y, Park S, Han R, et al. 820-GHz imaging array using diode-connected NMOS transistors in 130-nm CMOS. 2013 Symposium on VLSI Circuits, Kyoto, Japan, 2013, C12

[14] Lisauskas A, Bauer M, Boppel S, et al. Exploration of terahertz imaging with silicon MOSFETs. J Infrared Milli Terahz Waves, 2014, 35, 63

[15] Fang T, Dou R J, Liu L Y, et al. A 25 fps 32 × 24 digital CMOS terahertz image sensor. 2018 IEEE Asian Solid-State Circuits Conference (A-SSCC), 2018, 87

[16] Yokoyama S, Ikebe M, Kanazawa Y, et al. 5.8 A 32 × 32-pixel 0.9THz imager with pixel-parallel 12b VCO-based ADC in 0.18μm CMOS. 2019 IEEE International Solid-State Circuits Conference-(ISSCC), 2019, 108

[17] Jain R, Hillger P, Grzyb J, et al. 34.3 A 32 × 32 pixel 0.46-to-0.75THz light-field camera SoC in 0.13µm CMOS. 2021 IEEE International Solid- State Circuits Conference (ISSCC), 2021, 484

[18] Zhuo N, Liu F Q, Wang Z G. Quantum cascade lasers: From sketch to mainstream in the mid and far infrared. J Semicond, 2020, 41, 010301

[19] Kindness S J, Jessop D S, Wei B, et al. 100% amplitude modulation of an external cavity terahertz QCL using an optoelectronic chopper based on metamaterials and graphene. 2017 Conference on Lasers and Electro-Optics Europe & European Quantum Electronics Conference (CLEO/Europe-EQEC), 2017, 1

[20] Jin Y, Reno J L, Kumar S. Phase-locked terahertz plasmonic laser

array with 2 W output power in a single spectral mode. Optica, OPTICA, 2020, 7, 708
[21] Li W J, Ma Y, Xu Y F, et al. Continuous-wave single-mode quantum cascade laser at 5.1 THz based on graded sampled grating design. Photon Res, 2022, 10, 2686
[22] International Telecommunication Union ITU-R P. 676-11: Attenuation by Atmospheric Gases (ITU, 2016).
[23] The HITRAN Database. Accessed on Mar. 2019. [Online]. Available: http://www.cfa.harvard.edu/hitran/
[24] Fang T, Liu Z Y, Liu L Y, et al. Detection of 3.0 THz wave with a detector in 65 nm standard CMOS process. 2017 IEEE Asian Solid-State Circuits Conference (A-SSCC), 2017, 189
[25] Fang T, Liu L Y, Liu Z Y, et al. A 3.0 THz detector in 65 nm standard CMOS process. J Infrared Millim Waves, 2020, 39, 56
[26] Ikamas K, Lisauskas A, Boppel S, et al. Efficient detection of 3 THz radiation from quantum cascade laser using silicon CMOS detectors. J Infrared Millim Terahertz Waves, 2017, 38, 1183
[27] Boppel S, Lisauskas A, Mundt M, et al. CMOS integrated antenna-coupled field-effect transistors for the detection of radiation from 0.2 to 4.3 THz. IEEE Trans Microw Theory Tech, 2012, 60, 3834
[28] Smith T J, Broome A, Stanley D, et al. A hybrid THz imaging system with a 100-pixel CMOS imager and a 3.25–3.50 THz quantum cascade laser frequency comb. ESSCIRC 2019-IEEE 45th European Solid State Circuits Conference (ESSCIRC), 2019, 151
[29] Liu Z Y, Liu L Y, Yang J, et al. A CMOS fully integrated 860-GHz terahertz sensor. IEEE Trans Terahertz Sci Technol, 2017, 7, 455
[30] Knap W, Teppe F, Meziani Y, et al. Plasma wave detection of sub-terahertz and terahertz radiation by silicon field-effect transistors. Appl Phys Lett, 2004, 85, 675
[31] Dyakonov M, Shur M. Detection, mixing, and frequency multiplication of terahertz radiation by two-dimensional electronic fluid. IEEE Trans Electron Devices, 1996, 43, 380
[32] Crowne F J. Microwave response of a high electron mobility transistor in the presence of a Dyakonov–Shur instability. J Appl Phys, 2002, 91, 5377
[33] Lisauskas A, Glaab D, Roskos H G, et al. Terahertz imaging with Si MOSFET focal-plane arrays. SPIE OPTO: Integrated Optoelectronic Devices. Proc SPIE 7215, Terahertz Technology and Applications II, 2009, 119
[34] THORLABS ITC4000 Series Operation Manual, Version 3.9. New Jersey, U. S. A: Thorlabs, Inc. , Jul. 2018.
[35] Guo Z J, Yu N M, Wu L S. Column readout circuit with improved offset mismatch and charge sharing for CMOS image sensor. J Semicond, 2019, 40, 122404
[36] Wu R, Huijsing J H, Makinwa K A A. Read-out integrated circuits. Springer, 2012, 137
[37] Fang T, Liu M, Liu L Y, et al. A 32 × 32 array terahertz sensor in 65-nm CMOS technology. 2021 IEEE International Conference on Integrated Circuits, Technologies and Applications (ICTA), 2022, 259j
[38] Javadi E, But D B, Ikamas K, et al. Sensitivity of field-effect transistor-based terahertz detectors. Sensors, 2021, 21, 2909
[39] Ferreras M, Čibiraitė-Lukenskienė D, Lisauskas A, et al. Broadband sensing around 1 THz via a novel biquad-antenna-coupled low-NEP detector in CMOS. IEEE Trans Terahertz Sci Technol, 2021, 11, 16
[40] Zdanevičius J, Bauer M, Boppel S, et al. Camera for high-speed THz imaging. J Infrared Milli Terahz Waves, 2015, 36, 986
[41] Boukhayma A, Dupret A, Rostaing J P, et al. A low-noise CMOS THz imager based on source modulation and an In-pixel high-Q passive switched-capacitor N-path filter. Sensors (Basel), 2016, 16, 325

Min Liu (S'22) is pursuing a Ph.D. degree with the State Key Laboratory of Super-lattices and Microstructures, Institute of Semiconductors, Chinese Academy of Sciences, Beijing, China. Her research interests include low-noise readout integrated circuits design, terahertz spectrometer design, and CMOS-integrated terahertz image sensors design.

Ziteng Cai (S'22) is pursuing a B.S. degree at the Beijing University of Technology, Beijing, China, and trained at the State Key Laboratory of Super-lattices and Microstructures, Institute of Semiconductors, Chinese Academy of Sciences, Beijing, China. His research interests include terahertz detector design and CMOS-integrated terahertz image sensor design.

Jian Liu is a Full Professor in microelectronics and solid-state electronics with the State Key Laboratory of Super-lattices and Microstructures, Institute of Semiconductors, Chinese Academy of Sciences, Beijing, China, since 2005. His research interests include semiconductor optoelectronic detectors, terahertz imagers, and metamaterials.

Nanjian Wu (M'06) has been a Professor with the State Key Laboratory of Super-lattices and Microstructures, Institute of Semiconductors, Chinese Academy of Sciences, Beijing, China, since 2000. Since 2009, he has been an Honorable Guest Professor with the Research Institute of Electronics, Shizuoka University, Hamamatsu, Japan. His research includes the field of mixed-signal LSI and vision chip design.

Liyuan Liu (M'11) joined the State Key Laboratory of Super-lattices and Microstructures, Institute of Semiconductors, Chinese Academy of Sciences, Beijing, as an Associate Professor in 2012, where he became a Professor in 2018. His research interests include mixed-signal IC design, CMOS image sensors design, terahertz image sensors design, and monolithic vision chip design.