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An E-band CMOS frequency quadrupler with 1.7-dBm output power and 45-dB fundamental suppression

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Abstract: This paper presents an E-band frequency quadrupler in 40-nm CMOS technology. The circuit employs two push–push frequency doublers and two single-stage neutralized amplifiers. The pseudo-differential class-B biased cascode topology is adopted for the frequency doubler, which improves the reverse isolation and the conversion gain. Neutralization technique is applied to increase the stability and the power gain of the amplifiers simultaneously. The stacked transformers are used for single-ended-to-differential transformation as well as output bandpass filtering. The output bandpass filter enhances the 4th-harmonic output power, while rejecting the undesired harmonics, especially the 2nd harmonic. The core chip is 0.23 mm^2 in size and consumes 34 mW. The measured 4th harmonic achieves a maximum output power of 1.7 dBm with a peak conversion gain of 3.4 dB at 76 GHz. The fundamental and 2nd-harmonic suppressions of over 45 and 20 dB are achieved for the spectrum from 74 to 82 GHz, respectively.

Key words: capacitor neutralization; CMOS; E-band; frequency doubler; frequency quadrupler; push–push

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1. Introduction

Millimeter-wave (mm-Wave) automotive radar systems are one of the essential enabling technologies in autonomous vehicles. Thanks to smaller wavelength and smaller antenna size, 77-GHz automotive radars attract much attention over the latest decade[1–3]. These systems call for high-quality and power-efficient local oscillators (LOs). However, mm-Wave voltage-controlled oscillators (VCOs) suffer from limited tuning range and poor spectral purity due to low-Q inductors and low-capacitance-ratio varactors. As summarized in Fig. 1, the phase noise performance of recent-published mm-VCOs degrades by 24 dB from 20 to 80 GHz, which is much larger than the theoretical degradation value of 12 dB. To obtain low phase noise and wide tuning range LOs, lower frequency oscillators with their output multiplied up to the desired frequency are preferred. Therefore, a synthesizer architecture with a PLL embedded with a 20-GHz VCO, followed by frequency quadrupler is utilized to generate E-band LO signals, as shown in Fig. 2. To ensure the overall performance of the synthesizer, the quadrupler is required to be wideband, while providing high output power and robust operation. In addition, the quadrupler must suppress unwanted harmonics with low power consumption.

To build a frequency quadrupler, both the linear superposition technique[8] and the direct ×4 nonlinear class-B/C stages[9] can be employed. However, these techniques provide limited output power of the 4th harmonic. Besides, they usually rely on the accuracy of device modeling and are sensitive to process variations. Injection-locked[10, 11] and single-stage phase-controlled push–push frequency quadruplers[12] occupy compact chip area. Nevertheless, these techniques require additional buffer amplifiers due to the low conversion gain. Thus, cascading frequency doublers are preferred.

To address the above challenges, this paper introduces an E-band frequency quadrupler utilizing two push–push frequency doublers, achieving 1.7-dBm output power and over 45 dB fundamental suppression. As an extension of Ref. [13], this paper presents an in-depth analysis of the frequency quadrupler, which guides the design and optimization.

2. Design considerations

The nonlinearity of a class-B biased transistor can be employed to generate strong harmonic contents, which naturally forms a frequency multiplier. Researches on single-ended frequency doubler are mainly focused on extracting the 2nd harmonic by resonating the LC output tanks, and employing the transmission line based quarter-wavelength open stub to suppress the fundamental signal. However, the operation bandwidth is usually narrow, and the fundamental suppression is sensitive to the output frequency. Meanwhile, higher output power can be obtained via the differential swing in a balanced design. Thus, push–push topology[14–16] is considered. As shown in Fig. 3(a), the class-B biased pair (M_1 and M_2) generates in-phase 2nd-harmonic ($2f_0$) signals and the phase-shifted fundamental (f_0) signals. The two $2f_0$ signals are added while the f_0 signals are cancelled by each other at the combined drain. Thus, the balanced topology has the advantage of achieving wideband fundamental and high odd-harmonic suppression without using resonator tanks.

On the basis of the push–push topology, a cascode device (M_3) is added, as shown in Fig. 3(b). It not only ampli-

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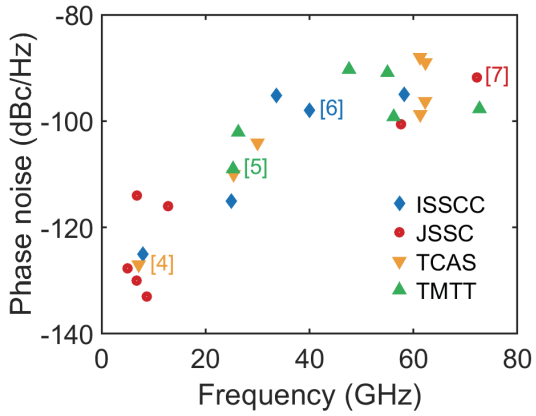


Fig. 1. (Color online) Phase noise performance of recent-published VCOs at 1 MHz.

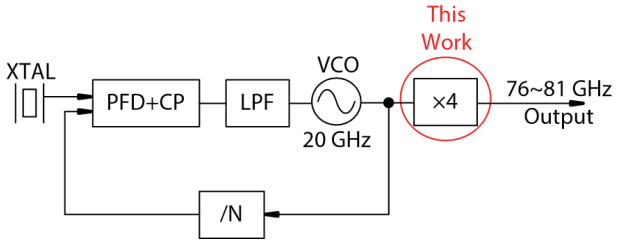


Fig. 2. The architecture of the proposed E-band frequency synthesizer.

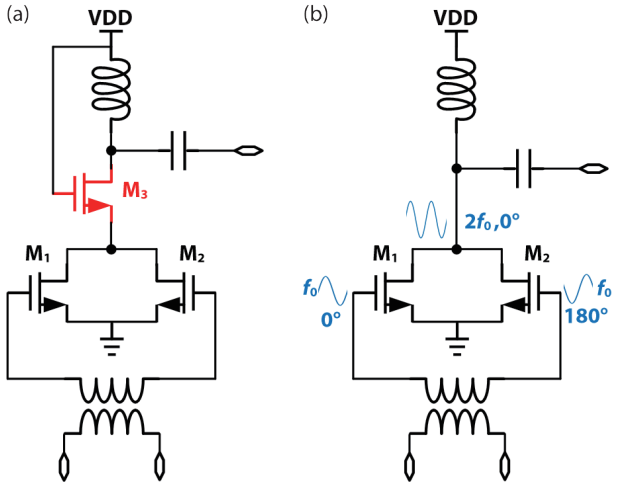


Fig. 3. The topology of (a) push-push doubler and (b) cascode structure.

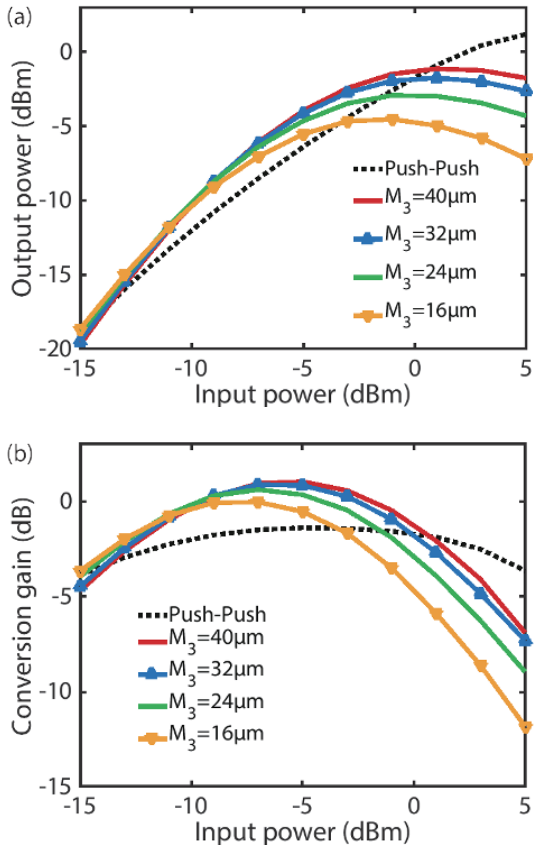


Fig. 4. (Color online) The simulation results of (a) output power and (b) conversion gain at 77-GHz.

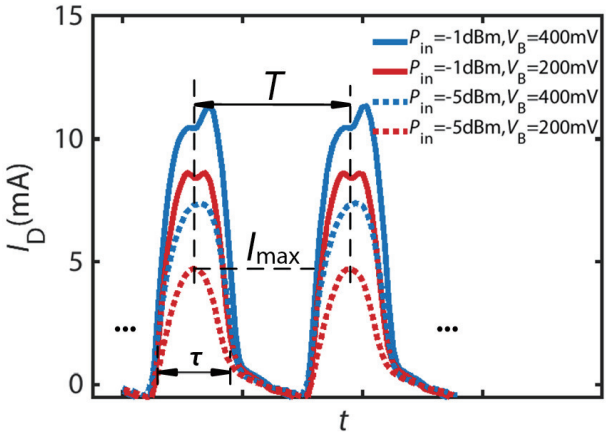


Fig. 5. (Color online) The drain current of M_1 with different input power and bias voltage.

fies the $2f_0$ component from the combined drain, but also reduces the Miller effect of M_1 and M_2, resulting in a higher gain-bandwidth product of the transistor. To meet the requirement of the output power, 16-μm devices are employed for the doubler pair. However, the addition of the M_3 decreases the drain voltage of the push–push pair. With a 1-V supply, the combined drain voltage decreases to 500 mV or below with a higher input power, leading to a deteriorated generation of $2f_0$ component. As a trade-off between conversion gain (CG) and power consumption, the supply voltage of the cascode doubler is raised to 1.5 V. Meanwhile, the size of M_3 also influences the generation of $2f_0$ component. Fig. 4 depicts the output power and CG at 77 GHz with the size of M_3 equals to 16, 24, 32, and 40 μm, respectively. It indicates that larger M_3 provides lower V_{GS}, raising the voltage of the combined drain, which further enhances CG. The maximum output power and conversion gain improvement gradually saturated when the size exceeds 32 μm, achieving a maximum output of –1.15 dBm with a peak CG of 1.2 dB from a 1.5-V supply. Moreover, the performance of the push–push one is also compared, which obtains a saturation power of 1.2 dBm with a limited CG of –1.5 dB. Hence, taking output power, conversion gain, reverse isolation and power consumption into consideration, the cascode topology is adopted, while a 32-μm cascode device is selected for the best performance.

As indicated in Fig. 4(a), the output power of the 2nd harmonic decreases when the input signal sweeps from 0 to 5 dBm. To address this issue, the drain current of the doubler pair is analyzed. Fig. 5 plots the drain current transient waveform of M_1. With different input power (–5 and –1 dBm) and

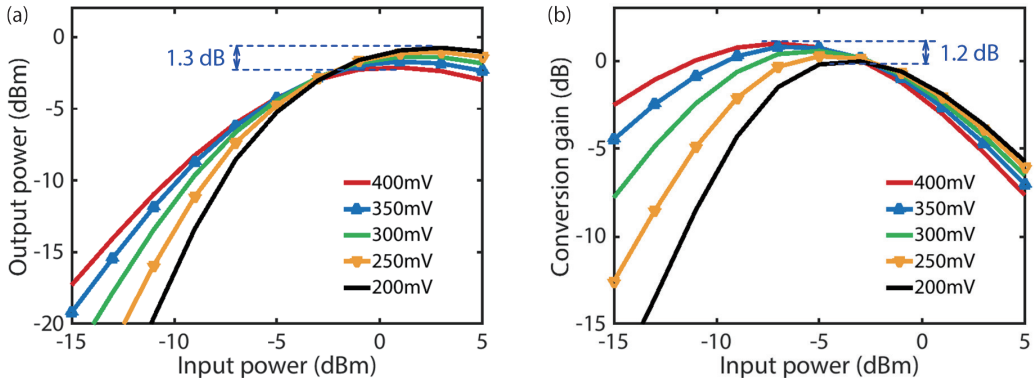


Fig. 6. (Color online) The simulation results of (a) output power and (b) conversion gain at 77-GHz with different bias.

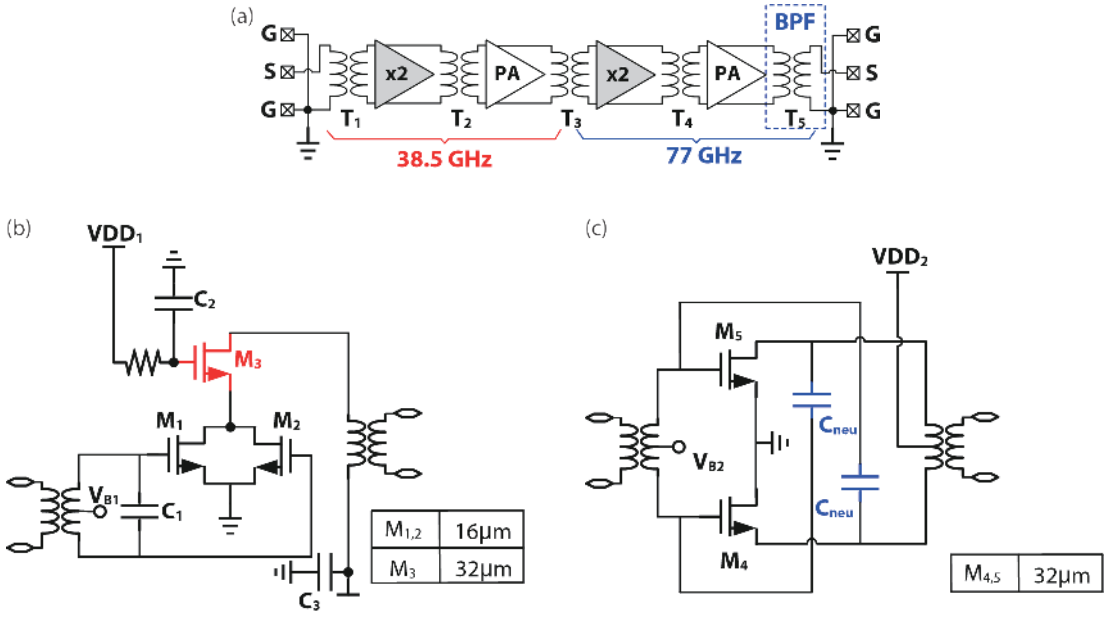


Fig. 7. (a) The block diagram of the proposed frequency quadrupler. The schematic of (b) frequency doubler and (c) power amplifier.

bias condition (200 and 400 mV), the operating state of the doubler pair changes, which influences the generation of the 2nd harmonic. In Fig. 5, I_{max} represents the maximum drain current, τ is the length of the pulse, and T is the period of the fundamental frequency. The even harmonic components at the combined drain node are controlled by the input power and the gate bias voltage. Besides, each even harmonic has a clear maximum below $\tau/T = 0.5$[17]. The simulated results of output power and conversion gain with the bias of 200, 250, 300, 350 and 400 mV are plotted in Fig. 6. When the input power increases to 0 dBm, I_{max} and the conduction duty cycle (τ/T) raises, which enhances the 2nd harmonic (see Fig. 6(a)). When increasing the input power to 5 dBm, I_{max} improves but τ/T becomes a bottleneck, resulting in reduction of 2nd harmonic. Meanwhile, the bias condition also influences I_{max} and τ/T, as indicated in Fig. 5. With a –1-dBm input, a bias of 400 mV provides higher I_{max} (see Fig. 5 solid-blue), while a bias of 200 mV achieves enhanced output power (see Fig. 6(a) black). Fig. 6 also suggests that a lower bias condition delivers 1.3 dB higher saturation power, while a higher bias offers compelling conversion gain. Consequently, taking dc power into account, 300 mV is the optimal choice.

3. Circuit implementation

The block diagram of the proposed frequency quadrupler is depicted in Fig. 7(a). Two single-stage power amplifiers (PAs) are implemented following each frequency doubler to compensate for loss. The inter-stage PA is designed to drive the second doubler into saturation and reduce the fundamental leakage from the first doubler, so as to avoid the intermixing of f_0 and $2f_0$ components at the second doubler. Furthermore, each transformer is carefully optimized, so that sufficient bandwidth and high harmonic suppression can be ensured.

3.1. Frequency doubler and power amplifier

The push–push topology with cascode device is adopted, as shown in Fig. 7(b). The bias voltage (V_{B1}) is set to 300 mV, as the optimal bias condition discussed in section 2. Therefore, the doublers produce strong harmonics and high conversion gain with low dc current. The two doublers consume 18 mW from a 1.5-V supply at 0 dBm input power. Besides, decoupling capacitors (C_2 and C_3) are implemented at both the gate and the drain terminals of the cascode device, so as to reduce the loss of single-ended-to-differential transformation.

Fig. 7(c) depicts the schematic of the power amplifier. Neutralization technique[18] is applied to build PAs at 38.5 and 77 GHz. The interdigitated metal-oxide-metal capacitor C_{neu} is cross connected between the drain and the gate of

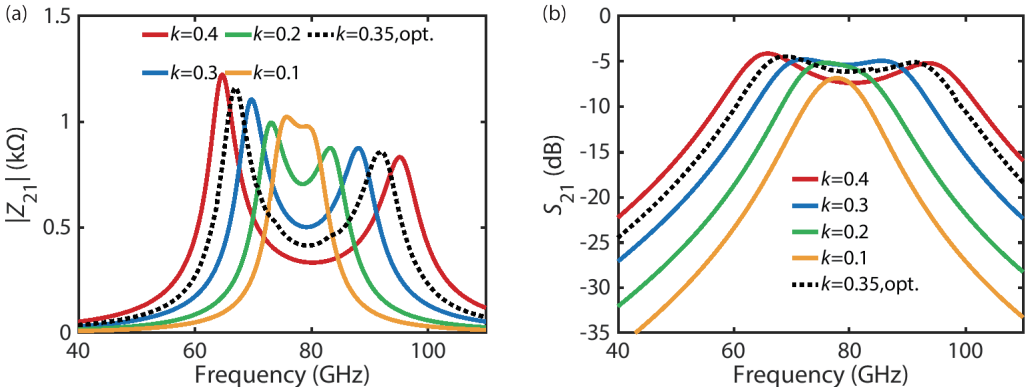


Fig. 8. (Color online) (a) Z_{21} and (b) S_{21} of T_4 with different k.

the differential pair (M_4 and M_5). This method reinforces the unconditional stability and gain without additional cost of power dissipation. With a 7.4-fF neutralization capacitor and a V_{B2} of 550 mV, the two PAs consume 16 mW from a 1-V supply at 0 dBm input power. Moreover, impedance matching is performed in this work, which provides higher gain and further enhances power efficiency. The two single-stage PAs offer a power gain of 13 and 8 dB, respectively.

3.2. Optimization of matching networks

In the proposed circuit, all inter-stage and output matching networks (T_{1-5}) are transformer-based resonators[19]. Meanwhile, the transformer can be used as a balun to covert a single-ended signal to a differential one. Ultra-thick metal M8 and M9 are used to form all the transformers. As a trade-off among conductor resistance, Q factor and chip area, the coil width of all the transformers is designed between 3 and 4 μm.

Biasing at class-B leads to an input impedance of 432-j×1190 Ω and 133-j×610 Ω of the push–push pairs, respectively. Such a large inductance makes it challenging to perform impedance matching. Direct matching results in large inductance of each coil up to around 2 nH, which brings large insertion loss and occupies sizable area. Therefore, C_1 is added to the input matching network (see Fig. 7(b)). Large C_1 is attractive to reduce the inductance of the coils, but contributes to a narrow matching bandwidth. Thus, a trade-off should be made between conductor resistance and matching bandwidth. After optimization, C_1 is set to 60 and 22 fF for each doubler. Meanwhile, T_1 and T_3 are designed highly symmetrical to ensure odd harmonics cancellation at the combined drain, so as to improve odd harmonic rejection. The secondary coils are center-tapped in order to easily bias the gate of the doublers.

T_2 and T_4 are carefully designed at 38.5 and 77 GHz to ensure low loss and high harmonics suppression simultaneously. The primary coil of the transformer resonates with the drain capacitance of cascade device, while the secondary coil resonates with the differential input capacitance of the following amplifier. Therefore, T_2 and T_4 are used to convert the common-mode second harmonic current of the doubler to the differential output voltage. To reduce fundamental leakage, T_2 is designed narrow-band at 38.5 GHz. Moreover, to cover the whole radar bandwidth (i.e., 76–81 GHz), weakly-coupled transformer is adopted to design T_4. The transformer's coupling coefficient (k) determines the transfer function of the coupled resonators. Fig. 8 depicts the transimpedance Z_{21} and S_{21} of T_4. On the one hand, a lower k flattens the response and in return introduces an insertion loss of over −8 dB. On the other hand, a higher k introduces less insertion loss as the expense of enlarged ripple. To guarantee wideband matching and strong output power of 4th harmonic, a k of 0.35 was chosen. Based on EM simulation, T_2 is implemented as a two-turn transformer with 28.1- and 23.5-μm inner radius, realizing 581 and 525 pH at 38.5 GHz. T_4 is implemented as a center-tapped one-turn transformer with 31- and 23.5-μm inner radius, realizing 164 and 152 pH at 77 GHz. Fig. 9 depicts the layout of the two transformers.

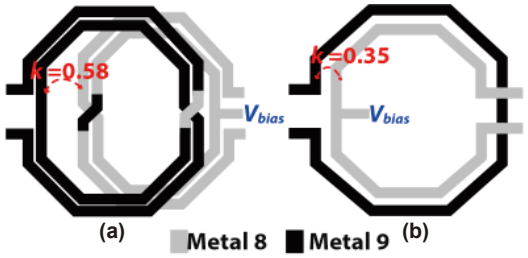
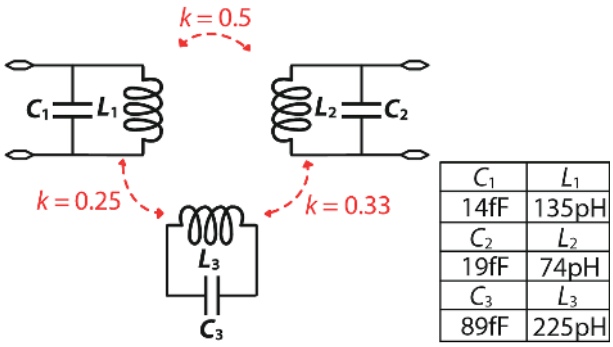


Fig. 9. The layouts of (a) T_2 and (b) T_4.



C_1	L_1
14fF	135pH
C_2	L_2
19fF	74pH
C_3	L_3
89fF	225pH

Fig. 10. The equivalent circuit model of T_5.

To further enhance harmonic suppression, T_5 is designed as a bandpass filter, especially to suppress the $2f_0$ component. Fig. 10 depicts the equivalent circuit model of T_5. L_1 and L_2 form a strongly-coupled center-tapped transformer, which ensures high output power of the 4th-harmonic element. The insertion of C_1 and C_2 adjusts the passband region, while minimizing transformer insertion loss. Finally, T_5 realizes a k of 0.5. L_3 and C_3 are implemented to form a transmission zero around the 2nd harmonic. After EM simulation, T_5

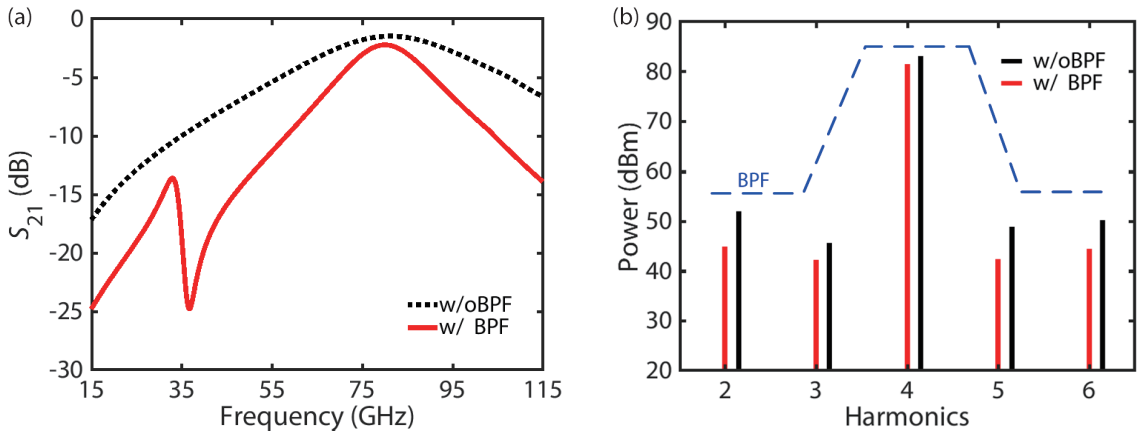


Fig. 11. (Color online) Simulated (a) S_{21} of T_5 and (b) harmonics at the output node with and without the bandpass filter.

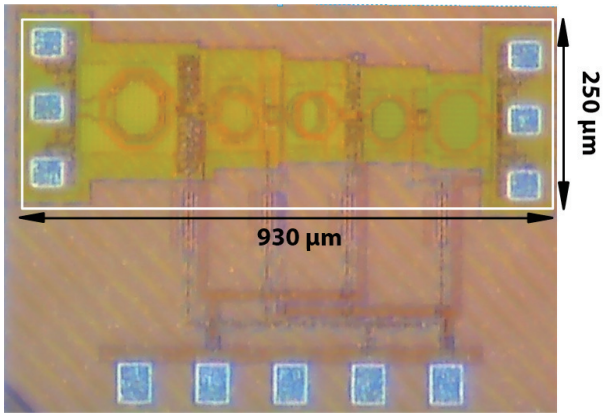


Fig. 12. (Color online) Chip micrograph.

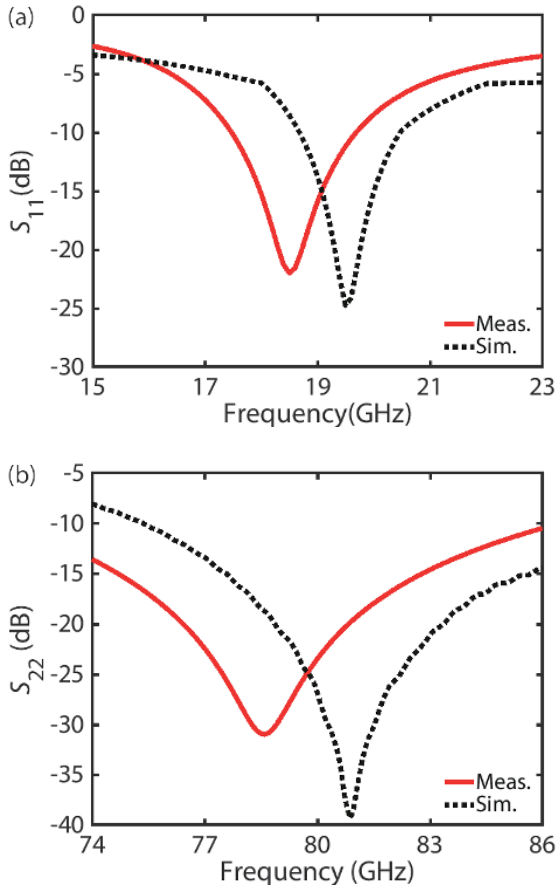


Fig. 13. (Color online) Measured *S*-parameters: (a) S_{11} and (b) S_{22}.

realizes a frequency response as a third-order two-pole/one-zero bandpass filter, as indicated in Fig. 11(a). Note that a sharp rejection around $2f_0$ occurs and the higher frequency is shaped in order to reduce the intermixed product of $5f_0$ and $6f_0$ components. With a input signal of 19.25 GHz, the simulated harmonics with and without the bandpass filter at the output of the proposed quadrupler is presented in Fig. 11(b). As expected, the filter reduces $2f_0$ harmonic by 7 dB. It has little effect on $3f_0$ harmonic but still helps in harmonic suppression for $5f_0$ and $6f_0$ components by 5 dB.

4. Measurement results

The frequency quadrupler is implemented in 40-nm CMOS technology. The chip microphotograph of the E-band frequency quadrupler is shown in Fig. 12. It consumes 34 mW with 1.5-V supply for the doublers and 1-V supply for the PAs. The core chip size is 930 × 250 μm^2, including G–S–G pads. The chip has been measured on a high-frequency probe station. The *S*-parameters are measured by a vector network analyzer operating up to 86 GHz.

As depicted in Fig. 13, the measured S_{11} maintains less than −10 dB across 17.5–19.7 GHz and S_{22} is below −10 dB across 75–86 GHz, indicting good impedance matching across the automotive radar band (i.e., 76–81 GHz). In Fig. 14, the simulated and measured output power and conversion gain are plotted. The measured saturated output power is around 1.7 dBm from 76 to 78 GHz (see Fig. 14(a)) with a peak conversion gain of 3.4 dB at 76 GHz (see Fig. 14(b)). Fig. 15 presents the frequency response of the quadrupler with a 1-dBm input. As revealed by the 4th harmonic, the quadrupler has a 1.5-dB bandwidth of more than 6 GHz (74–80 GHz). Note that the quadrupler achieves a fundamental and 2nd-harmonic suppression above 45 and 20 dB, respectively, over the measured band.

In further research, an VCO and frequency quadrupler link is designed. In Fig. 16, the measured phase noise spectrum of the multiplier output at 77 GHz and the VCO output at 19.25 GHz are depicted. As expected, the phase noise increases by 12 dB, which matches the theoretical result well. It proves that the proposed multiplier does not introduce significant noise penalties. Therefore, it is suitable as a building block of the automotive radar systems.

In Table 1, the performance of the proposed frequency quadrupler is summarized and compared with prior-art designs. Occupying a competitive core chip area, this work ex-

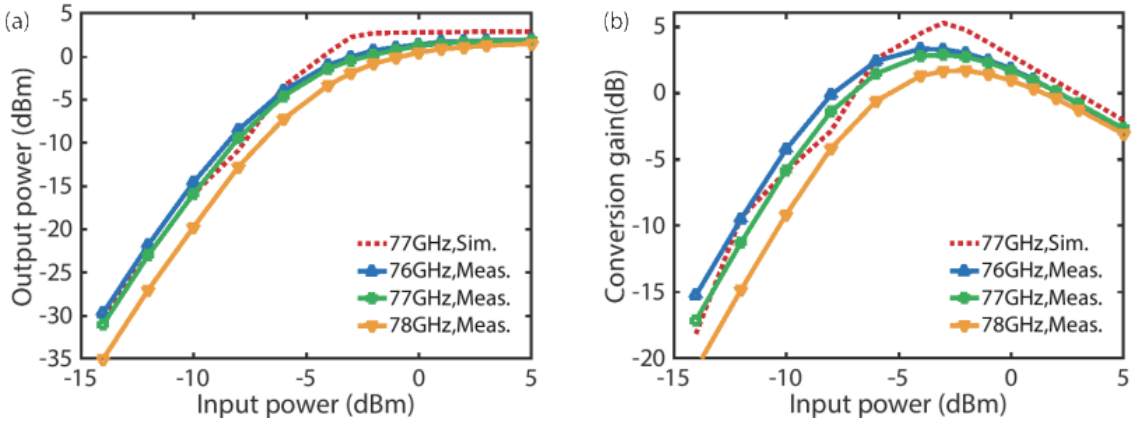


Fig. 14. (Color online) Measurement results of (a) output power and (b) conversion gain.

Table 1. Performance comparison.

Parameter	MWCL 2020[20]	MWCL 2021[21]	TMTT 2020[22]	This work
Technology	90 nm CMOS	40 nm CMOS	120 nm SiGe	40 nm CMOS
Output frequency (GHz)	71–81	65.6–75.2	70–110	74–82
Output power (dBm)	3.1	–0.2	3	1.7
Conversion gain (dB)	N/A	–8.9	–1.5	3.4
Fundamental suppression (dB)	>36	>33	>30	>45
P_{DC} (mW)	70	11.3	240	34
Core area (mm^2)	0.52	0.1	1.9	0.23

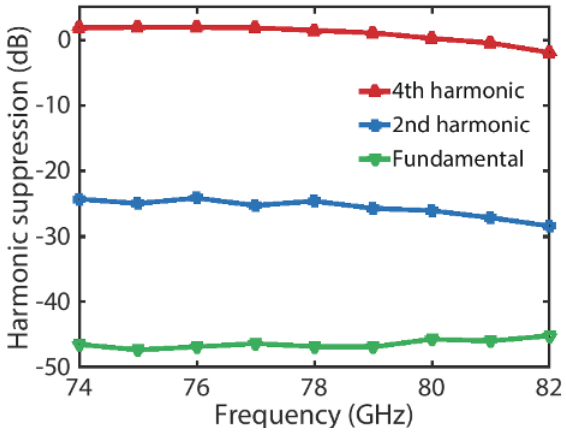


Fig. 15. (Color online) Measured output power of the E-band quadrupler.

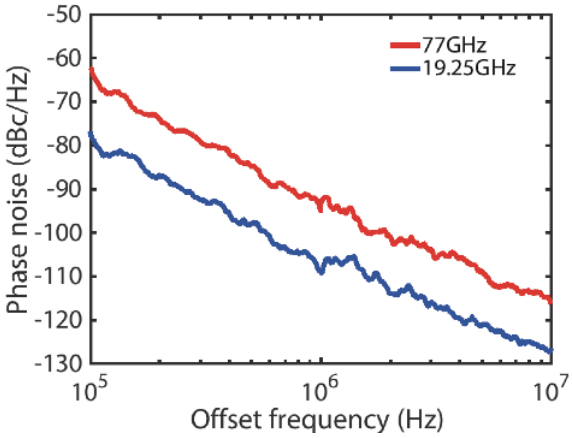


Fig. 16. (Color online) Measured phase noise at 77 GHz (red) and VCO phase noise at 19.25 GHz (blue).

hibits sufficient output power and conversion gain with the highest fundamental suppression and relatively low power dissipation.

5. Conclusion

An E-band CMOS frequency quadrupler with 1.7 dBm output power and 3.4 dB conversion gain has been demonstrated in a 40-nm CMOS process. The chip consumes 34 mW and occupies 0.23 mm^2 silicon area. This design utilizes two push-push cascode frequency doublers and two single-stage power amplifiers with well-optimized transformer-based matching networks. Besides, it achieves compelling conversion gain (3.4 dB) and excellent fundamental and 2nd-harmonic suppression over the spectrum from 74 to 82 GHz.

Acknowledgements

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