

Influence of epitaxial layer structure and cell structure on electrical performance of 6.5 kV SiC MOSFET

Lixin Tian^{1,†}, Zechen Du¹, Rui Liu¹, Xiping Niu¹, Wenting Zhang¹, Yunlai An¹, Zhanwei Shen², Fei Yang^{1,†}, and Xiaoguang Wei¹

¹State Key Laboratory of Advanced Power Transmission Technology, Global Energy Interconnection Research Institute Co., Ltd., Beijing 102209, China

²Key Laboratory of Semiconductor Material Sciences, Institute of Semiconductors, Chinese Academy of Sciences, Beijing 100083, China

Abstract: Silicon carbide (SiC) material features a wide bandgap and high critical breakdown field intensity. It also plays an important role in the high efficiency and miniaturization of power electronic equipment. It is an ideal choice for new power electronic devices, especially in smart grids and high-speed trains. In the medium and high voltage fields, SiC devices with a blocking voltage of more than 6.5 kV will have a wide range of applications. In this paper, we study the influence of epitaxial material properties on the static characteristics of 6.5 kV SiC MOSFET. 6.5 kV SiC MOSFETs with different channel lengths and JFET region widths are manufactured on three wafers and analyzed. The FN tunneling of gate oxide, HTGB and HTRB tests are performed and provide data support for the industrialization process for medium/high voltage SiC MOSFETs.

Key words: silicon carbide; epitaxial layer; channel length; JFET region width; FN tunneling; HTGB

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1. Introduction

Silicon carbide (SiC) is a typical representative of the wide bandgap of semiconductors, due to its bandgap, strong critical breakdown field and high thermal conductivity. SiC materials and devices have been included in the National 14th Five-Year Plan for Science and Technology^[1, 2]. In the past two decades, SiC power devices have been widely used in low-voltage applications. Companies such as CREE^[3], Rohm^[4], and Infineon^[5] have dominated the market. In high-voltage applications, SiC devices have been used in high-speed motor drives, solid-state transformers, railway traction and fast chargers for electric vehicles^[6–8]. In traditional silicon-based power converters, high-voltage silicon IGBTs are usually connected in parallel and in series to meet the needs of high voltage and high current. However, series and parallel connections will introduce voltage imbalance and current imbalance, respectively.

High voltage devices play a significant role in improving device performance and equipment reliability^[9]. Silicon carbide metal–oxide–semiconductor field effect transistors (SiC MOSFETs) have the advantages of high voltage, low loss, high temperature operation, and so on^[10]. They are also highly efficient and miniaturized for power electronic equipment. In addition, they play an important role and are an ideal choice for new power electronic devices^[11].

In this paper, the influence of epitaxial properties on the static properties of 6.5 kV SiC MOSFETs is studied. Five types

of SiC MOSFETs with different channel lengths and JFET region widths are developed on three wafers and analyzed in detail. Finally, the gate oxide characteristics of the device were analyzed.

2. Epitaxial layer design and device preparation

2.1. 6.5 kV MOSFET epitaxial layer design

The slope of the electric field in the drift region is determined by the doping concentration of the drift region, which can be obtained according to the Poisson equation:

$$\frac{dE_x}{dx} = -\frac{d^2\psi}{dx^2} = \frac{qN_d}{\epsilon_s}. \quad (1)$$

In the formula: N_d is the doping concentration of the drift region, and ϵ_s is the dielectric constant of SiC.

From formula (1), the device blocking voltage V_R can be related to the breakdown critical electric field E_m of the drift region as follows:

$$V_R = \left(E_m - \frac{qN_d w}{2\epsilon_s} \right) w. \quad (2)$$

Therefore, only by deriving the relationship between E_m and the doping concentration N_d of the drift region and the thickness w of the drift region can the relationship between the blocking voltage V_R and the parameters of the drift layer be obtained. From Ref. [12], the relationship between the breakdown critical electric field and the doping concentration of the drift region is as follows:

$$E_m = \frac{2.49 \times 10^6}{1 - \frac{1}{4} \lg(N_d/10^{16})}. \quad (3)$$

Correspondence to: L X Tian, tianlixin0526@163.com; F Yang, yangsenji@163.com

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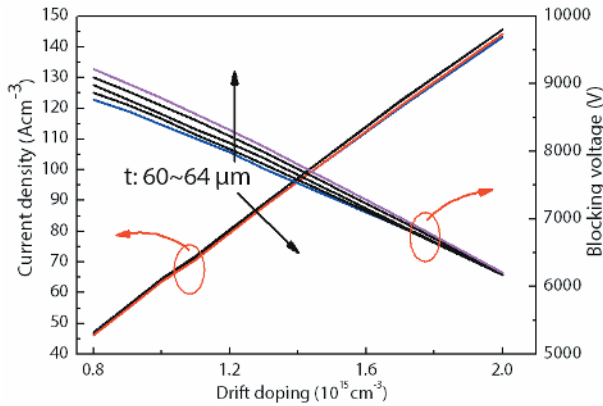


Fig. 1. (Color online) Current density and blocking voltage variation with doping concentration and thickness of epitaxial layer.

From Eqs. (2) and (3), the relationship between the device breakdown voltage V_R and the doping concentration N_d under different drift layer widths w can be obtained. The greater the thickness, the greater the blocking voltage that the epitaxial layer can bear; and the greater the doping, the smaller the blocking voltage that the epitaxial layer can bear.

Considering the specific on-resistance R_{sp} of the epitaxial layer as:

$$R_{sp} = \frac{w}{q\mu_n N_d}. \quad (4)$$

There is a trade-off relationship between the specific on-resistance and the blocking voltage of the epitaxial layer. It is necessary to combine formula calculation and TCAD simulation to determine the thickness and concentration of the epitaxial layer. In this paper, Sentaurus TCAD is used to simulate the characteristics of 6.5 kV SiC MOSFET.

Fig. 1 shows the current density and blocking voltage variation with doping concentration and thickness of epitaxial layer. To achieve a blocking voltage of 6.5 kV, it is determined that the blocking voltage of the epitaxial layer is 8.125 kV, leaving a margin of 25%. The thickness of the epitaxial layer is between 60 to 64 μm , and the blocking voltage per micron is about 120 V. Epitaxial doping concentration is about $(1.1\text{--}1.3) \times 10^{15} \text{ cm}^{-3}$. Epitaxial wafer thickness and concentration have inter- and intra-chip inhomogeneities. For high-voltage devices, the epitaxial layer contributes most of the resistance and the blocking voltage, so the intra- and inter-wafer uniformity of epitaxial wafer thickness and concentration has a greater impact on the characteristics of the device.

2.2. 6.5 kV SiC MOSFET device preparation

In this paper, the 6.5 kV SiC MOSFETs were fabricated on a (0001) Si-faced, 4° off-axis toward the $\langle 11\bar{2}0 \rangle$ direction, and N-type 4H-SiC substrate. The nominal voltage was 6.5 kV, and the epitaxial layer ranged from 60 to 65 μm thick with an N-type doping concentration of approximately $1.2 \times 10^{15} \text{ cm}^{-3}$. Due to the intra- and inter-wafer uniformity of epitaxial wafer thickness and concentration, the thickness and concentration has a large range. Fig. 2 shows a schematic diagram of the structure of a 6.5 kV SiC MOSFET.

Al was used as the P-type dopant and N was the N-type dopant. Multiple energy implants of Al and N were implanted to form the P well, P+ body, N+ source and JFET. After all of the ion implantations were made, activation anneal was carried out at 1600–1750 $^\circ\text{C}$ for 30 min with carbon

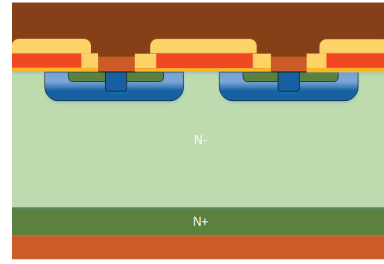


Fig. 2. (Color online) Schematic cross-section of 6.5 kV SiC MOSFET.

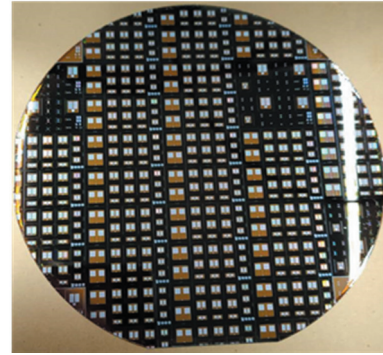


Fig. 3. (Color online) 6.5 kV SiC MOSFET devices on the 6-inch wafer.

cap to maximize lattice recovery and dopant activation. Then, a sacrificial oxidation of 20 nm was conducted to get rid of the surface roughness caused by ion implantation. After that, a 50 nm gate oxide was formed by thermal oxidation followed by NO annealing. Phosphorus-doped polysilicon of 500 nm was then deposited over the gate oxide, followed by gate patterning. 700 nm of inter-layer dielectric was then deposited and patterned to form the ohmic contact window. 150 nm Ni was deposited on the front and backsides of the wafer and rapid thermal annealing (RTP) was carried out at 1000 $^\circ\text{C}$ for 2 min to form the ohmic contacts. The interlayer dielectric on the poly-Si was patterned to expose the gate poly-Si pad to form a gate bus. The top metal stack (Ti/Al) was then deposited and patterned to form the source and gate pads. Then, the passivation layer polyimide was deposited and patterned. Lastly, the metal stack (Ti/Ag) was deposited on the backside. The design structure of a floating guard ring edge termination was used for the 6.5 kV conventional planar-gate power MOSFETs. Fig. 3 shows a wafer photo of a 6.5 kV SiC MOSFET. In this article, we use three epitaxial wafers to develop MOSFETs. The parameters of the epitaxial wafers are shown in Table 1. The specific on-resistances contributed by the three types of epitaxial layers are 34.1, 36.5 and 34.8 $\text{m}\Omega\cdot\text{cm}^2$.

In this paper, five kinds of chips with different channel lengths L_c and JFET region widths W_j were designed on the wafer. The cell structure parameters are shown in Table 2.

3. Results and discussion

3.1. Influence of epitaxial layer parameters on conduction characteristics

As shown in Fig. 4, the output characteristics of 5 cell structures in 3 epitaxial wafers are compared. The gate-source voltage is 20 V, and the drain-source voltage is 4 V. It can be seen from Fig. 4 that the average current of #1 wafer is the largest, the average current of #3 wafer is second, and the

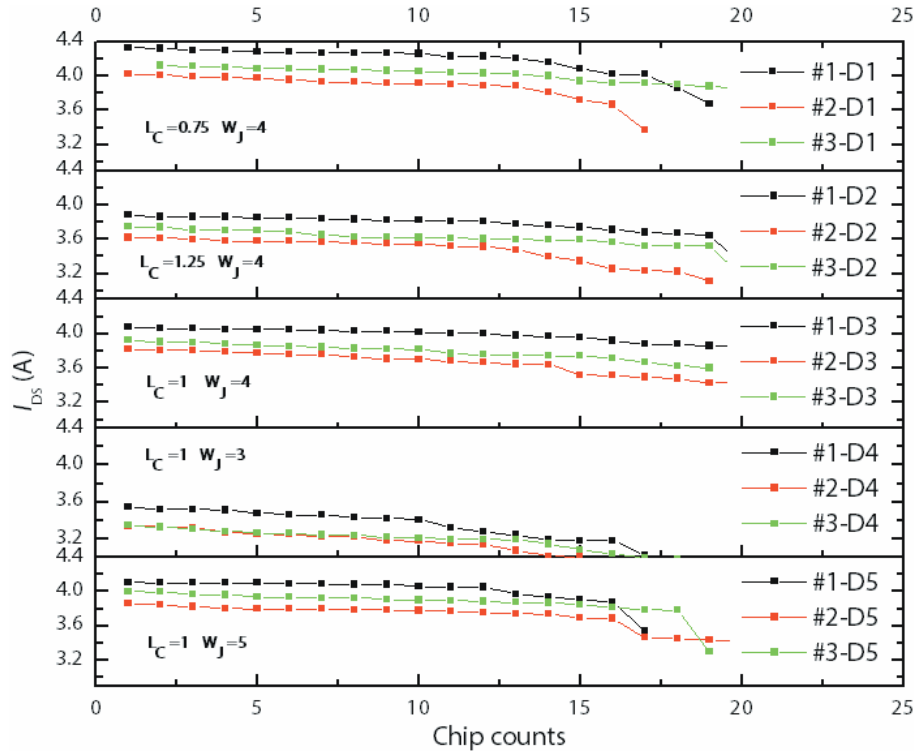


Fig. 4. (Color online) Comparison of output current of five chips on three wafers.

Table 1. Epitaxial layer thickness and doping concentration.

Number	Thickness (μm)	Doping (10^{15}cm^{-3})	$t/(N_d q \mu)$
#1	64.7	1.29	34.1
#2	62.3	1.16	36.5
#3	62.5	1.22	34.8

Table 2. Cell parameter table.

Cell number	Channel length (μm)	Width of JFET region (μm)
C1	0.75	4
C2	1.25	4
C3	1	4
C4	1	3
C5	1	5

average current of #2 wafer is the smallest. The wafer output current has the same law in the five types of cells. The active area of the five chips is the same, which is 4.7 mm^2 . Due to the different chip pitches, the edges and corners of the active area of the chip are different, there will be a slight difference in the total cell area but the overall can be ignored. The specific on-resistance of C1 device on the wafer #1 is $44 \text{ m}\Omega\text{-cm}^2$. The resistance of SiC MOSFET consists of substrate resistance, drift region resistance, JFET resistance, accumulation region resistance, channel resistance, source region resistance and ohmic contact resistance. In the case of the same cell structure, the epitaxial layer parameters (i.e., the doping concentration and thickness of the epitaxial wafer) are important factors affecting the conduction characteristics. The greater the thickness w of the epitaxial wafer, the greater the resistance; and the smaller the doping concentration N_d , the higher the resistance. The specific on-resistance contributed by the epitaxial layer is $t/(N_d q \mu)$, where μ is the SiC bulk

mobility.

The current difference between #1 wafer and #2 wafer is 0.3 A . According to the I_D - V_{DS} characteristics of the chip and the chip area, the specific on-resistance difference of #1 wafer and #2 wafer is $0.38 \text{ m}\Omega\text{-cm}^2$ which is similar to epitaxial wafer specific on-resistance difference. For the C4 device, when the JFET width is $3 \mu\text{m}$, the proportion of JFET resistance increases, and the effect of epitaxial wafer differences on device conduction is weakened. So the output currents of #2 and #3 are basically the same.

The current distribution uniformity of the #3 wafer is the best, and #2 wafer is the worst, which is largely due to epitaxial layer thickness and doping concentration inhomogeneity. Therefore, the quality of the epitaxial wafer affects the uniformity of the electrical properties of the chip.

3.2. Influence of cell parameters on conduction characteristics

In this paper, the output curves and transfer curves of the devices with five cell parameters are compared at $V_{GS} = 20 \text{ V}$, which are shown in Fig. 5. The threshold voltage is determined at the drain-source current of 5 mA by sweeping the gate-source voltage with drain electrodes biased of 10 V . With the increasing channel length, the threshold voltage $V_{GS(th)}$ of the device increases. The on-resistance increases, leading to the drop of the output characteristic curve, and so does the transconductance g_{fs} . With the increasing width of the JFET region, the threshold voltage increases, but the on-resistance decreases. The output characteristic curve moves up, and the three transfer curves cross during the gate voltage increase. When the JFET width is $3 \mu\text{m}$, the output curve deviates from the linear region earlier. When V_{DS} is kept constant, the main resistance of the device at low gate voltage comes from channel. The larger the JFET width is, the

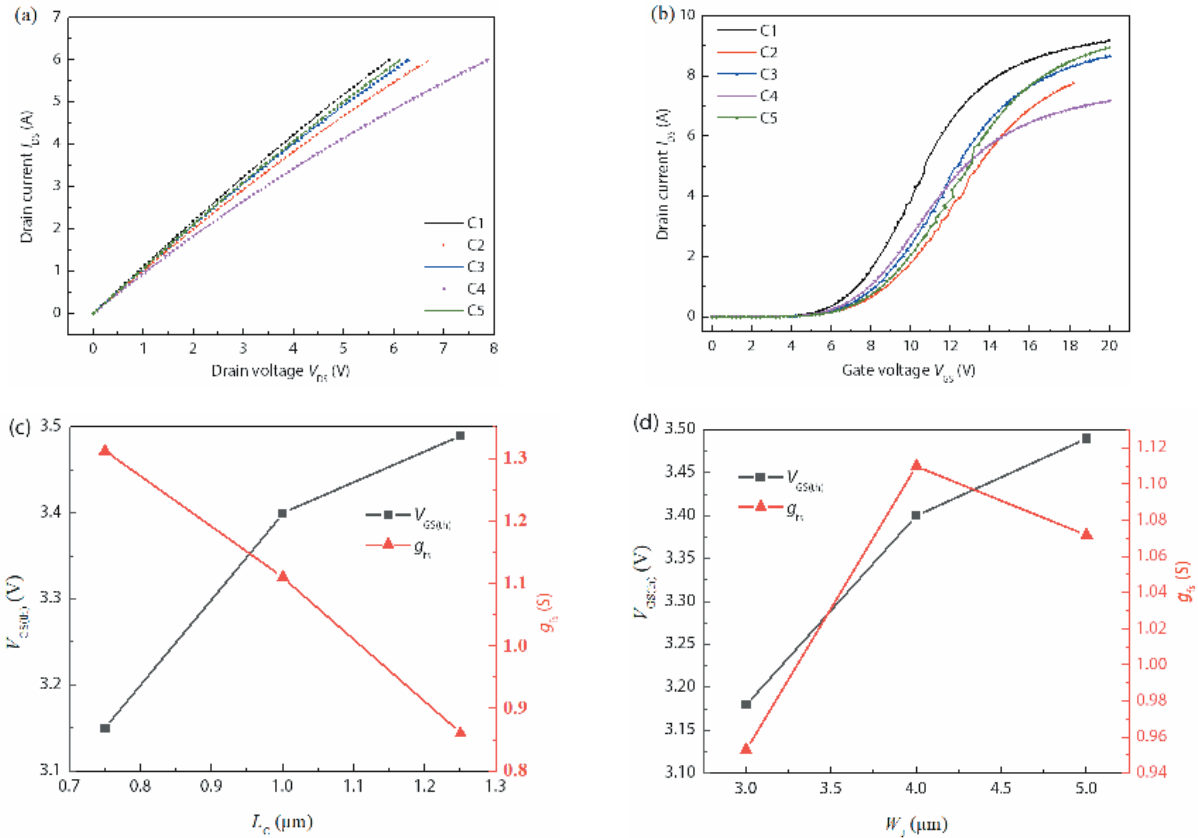


Fig. 5. (Color online) Comparison of output, transfer and derivative parameters of five cell structures. (a) Output characteristic curves. (b) Transfer characteristic curves. (c) Transconductance comparison of different channel lengths. (d) Cell transconductance comparison of different JFET widths.

Table 3. Chip yield of 3 wafers.

	#1	#2	#3
C1	36.36%	54.55%	61.90%
C2	36.36%	54.55%	57.14%
C3	40.91%	54.55%	38.10%
C4	31.82%	50.00%	42.86%
C5	54.55%	63.64%	52.38%

smaller the cell density and the channel density are. Therefore, at low gate voltage, the device resistance increases with the increase of JFET width. To achieve the same current, such as 5 mA, more gate voltage needs to be applied. Therefore, for the same active area, the wider JFET, the greater the threshold voltage. The change of threshold voltage with channel length is the same as the change of threshold voltage with JFET width.

3.3. The device’s yield

This article counts the yield of the chips on each wafer. The overall chip area on the wafer is relatively small, so the gate–source yield and blocking yield of the chip are basically the same. We also make a batch of 6.5 kV large-area chips, with the active area of 37 mm². The gate–source yield and blocking yield are independent of each other^[13]. The yield of 6.5 kV MOSFET in this paper is shown in Table 3. The average yields are 40%, 55% and 50%, for the three wafers, respectively. The yield of high-voltage devices decreases rapidly with the increase of defect density and chip area. Reducing the defects in epitaxial materials and those introduced in processes

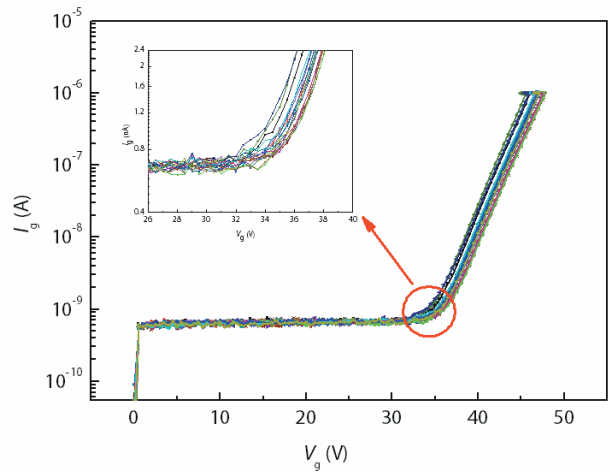


Fig. 6. (Color online) Breakdown characteristics of test pattern gate oxide capacitors.

is an important approach to realize commercialization of high-voltage SiC MOSFET devices.

3.4. Gate oxide characteristics of the device

FN tunneling is also called triangular breakdown^[14–16]. When the electric field is high enough, the gate oxygen energy level bends to form a triangular shape. When the width of the triangular region is small, electrons directly tunnel. The field strength during FN tunneling is an important parameter for evaluating the quality of the gate oxide. During the preparation of the MOSFET device, the breakdown characteristics of the gate oxide can be tested through the patterned

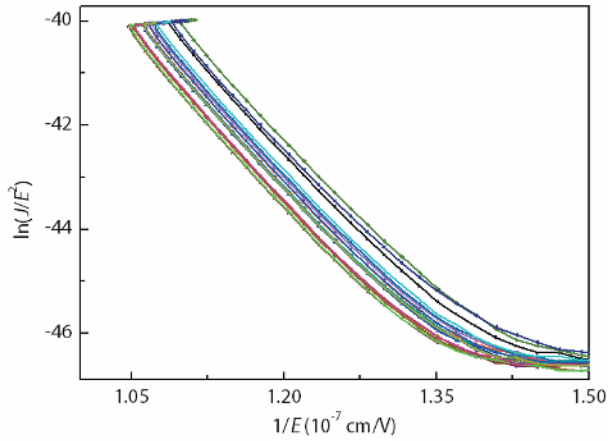


Fig. 7. (Color online) The transforming curves of the gate oxide capacitor I - V curves.

gate oxide capacitor. The I - V curves of gate oxide capacitor are shown in Fig. 6. When V_g is around 35 V, the leakage current of the curve begins to increase rapidly. Therefore, the FN tunneling of this device occurs at an approximate value of 7 MV/cm.

The potential barrier height between the gate oxide and SiC is obtained by transforming the I - V curve^[14]. The transforming curves of the gate oxide capacitor I - V curves are shown in Fig. 7.

$$J_{\text{FN}} = AE^2 \exp\left(\frac{-B}{E}\right), \quad (5)$$

$$\ln\left(\frac{J}{E^2}\right) = \ln A - \frac{B}{E}, \quad (6)$$

$$A = \frac{q^3 m}{8\pi h m_{\text{ox}} \phi_b}, \quad B = \frac{8\pi \sqrt{2m_{\text{ox}} \phi_b}^{3/2}}{3hq}, \quad (7)$$

where m_{ox} is the mass of electrons in the oxide layer, $m_{\text{ox}} = 0.42m = 3.826 \times 10^{-31}$ kg, h is Planck's constant, $h = 6.626 \times 10^{-34}$ J·s.

According to the slopes of the transforming curves, the potential barrier height ϕ_b is:

$$\phi_b = \left(\frac{-B}{4.43 \times 10^7}\right)^{\frac{2}{3}} \text{ eV}. \quad (8)$$

Fig. 8 shows the relationship between barrier height ϕ_b and the slope. In our data, the range of slope B is $(1.987-2.125) \times 10^{-8}$, and the range of ϕ_b is 2.75–2.85 eV. It represents a high barrier height between gate oxide and SiC.

We prepared several 6.5 kV SiC MOSFET modules. Fig. 9 shows 6.5 kV SiC MOSFET package layout and outline. The long-term reliability of the gate oxide were evaluated through high-temperature gate bias tests (HTGB).

Under two conditions of gate-source bias $V_{\text{GS}} = -8$ V and $V_{\text{GS}} = 20$ V, respectively, the HTGB reliability tests were performed for 650 h at the temperature of 150 °C. Fig. 10 shows the results of high temperature gate bias reliability test for forward gate voltage test and reverse gate voltage test. The gate leakage current is below 5 nA. After the reliability test, there is no degradation of static characteristics for 6.5 kV

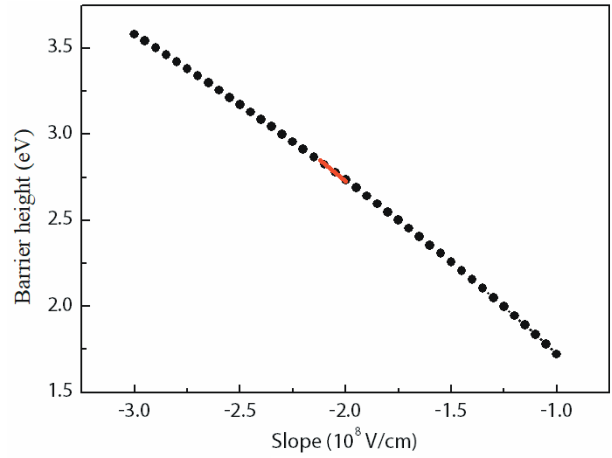


Fig. 8. (Color online) The relationship between barrier height and slope.

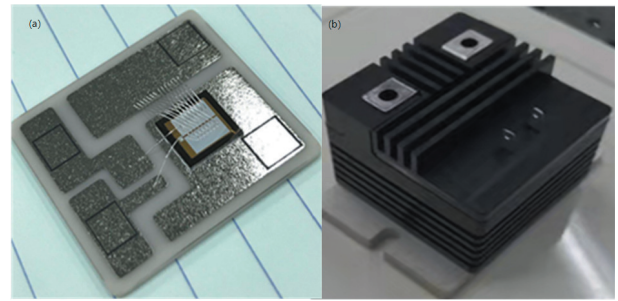


Fig. 9. (Color online) 6.5 kV SiC MOSFET package layout and outline.

SiC MOSFET.

3.5. High temperature reverse bias (HTRB) reliability

The high temperature reverse bias reliability is carried out at 150 °C. The gate and source is short-circuited and grounded. The V_{DS} is set to 5.15 kV, and the leakage is tested every two minutes. Fig. 11 shows the leakage results of the HTRB reliability with a total of 560 h. After the HTRB reliability test is completed, the device is retested again. The retest results prove that the device is intact.

4. Conclusions

The structure of the high-voltage 6.5 kV SiC MOSFET device is optimized and developed through process optimization. Based on the electrical characteristics of the device with different epitaxial structures and cell parameters, the following conclusions are drawn:

The specific on-resistance of C1 device on the wafer #1 is 44 mΩ·cm². The uniformity of the current distribution is large due to inhomogeneity of the epitaxial layer thickness and doping concentration. Therefore, the quality of the epitaxial wafer affects the uniformity of the electrical properties of the chip.

With the decreasing channel length, the threshold voltage $V_{\text{GS(th)}}$ of the device decreases and the transconductance increases. As the width of the JFET region increases, the threshold voltage increases and the transconductance first increases and then decreases.

The FN tunneling of the device is about 7 MV/cm, and the barrier height ϕ_b ranges from 2.75 to 2.85 eV.

The HTGB tests for 650 h respectively indicate that the

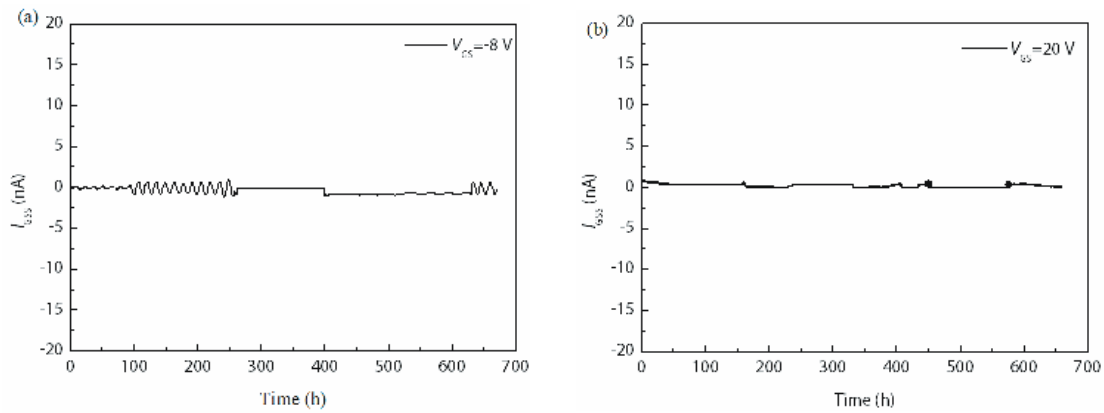


Fig. 10. High temperature gate bias reliability. (a) Forward gate voltage test results. (b) Reverse gate voltage test results.

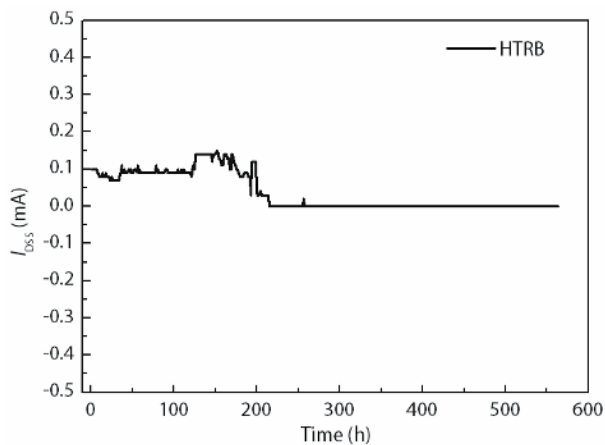


Fig. 11. The results of high temperature reverse bias reliability.

gate oxide has good reliability. The 560 h HTRB also passed.

These results show that the design, fabrication and analysis of the device characteristics of 6.5 kV SiC MOSFET will provide important guiding and significant promotion value for its penetration into the power grid field.

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References

- [1] Sun B X, Xie R B, Yu C, et al. Structural characterization of SiC nanoparticles. *J Semicond*, 2017, 38, 103002
- [2] Zeng C, Deng L F, Li Z J, et al. Experimental comparison of SiC GTO and ETO for pulse power applications. *J Semicond*, 2018, 39, 124017
- [3] Wolfspeed company C4D40120D datasheet [EB/OL] (2019-6-17) [2020-3-2]. <https://www.wolfspeed.com/power/products/sic-schottky-diodes>
- [4] Rohm company SCT2450KEHR datasheet [EB/OL] (2019-2-22). <https://www.rohm.com.cn/products/sic-power-devices/sic-mosfet>
- [5] Infineon company AIMW120R035M1H datasheet [EB/OL] (2019-2-22). <https://www.infineon.com/cms/cn/product/power/mosfet/silicon-carbide/discretes/aimw120r035m1h>
- [6] Mainali K, Wang R X, Sabate J, et al. Current sharing and over-voltage issues of paralleled SiC MOSFET modules. *2019 IEEE Energy Convers Congr Expo ECCE*, 2019, 2413
- [7] Chen J J, Jiang X, Li Z J, et al. Investigation on effects of thermal stress on SiC MOSFET degradation through power cycling tests. *2020 IEEE Applied Power Electronics Conference and Exposition*, 2020, 1106
- [8] Bencherif H, Yousfi A, Dehimi L, et al. Analysis of Al₂O₃ high-k gate dielectric effect on the electrical characteristics of a 4H-SiC low-power MOSFET. *2019 1st International Conference on Sustainable Renewable Energy Systems and Applications*, 2019, 1
- [9] Wirths S, Mihaila A, Romano G, et al. Study of 1.2kV high-k SiC power MOSFETS under harsh repetitive switching conditions. *2021 33rd International Symposium on Power Semiconductor Devices and ICs*, 2021, 107
- [10] Fukunaga S, Takayama H, Hikihara T. A study on switching surge voltage suppression of SiC MOSFET by digital active gate drive. *2021 IEEE 12th Energy Conversion Congress & Exposition*, 2021
- [11] Agarwal A, Baliga B J, Francois M M A, et al. 3.3 kV 4H-SiC planar-gate MOSFETs manufactured using Gen-5 PRESiC™ technology in a 4-inch wafer commercial foundry. *Southeastcon 2021*, 2021, 1
- [12] Konstantinov A O, Wahab Q, Nordell N, et al. Ionization rates and critical fields in 4H silicon carbide. *Appl Phys Lett*, 1997, 71, 90
- [13] Tian L X, Yang F, Niu X P, et al. Development and analysis of 6500V SiC power MOSFET. *2021 18th China International Forum on Solid State Lighting & 2021 7th International Forum on Wide Bandgap Semiconductors*, 2021, 6
- [14] Chanana R K, McDonald K, di Ventra M, et al. Fowler-Nordheim hole tunneling in p-SiC/SiO₂ structures. *Appl Phys Lett*, 2000, 77, 2560
- [15] Fiorenza P, Frazzetto A, Guarnera A, et al. Fowler-Nordheim tunneling at SiO₂/4H-SiC interfaces in metal-oxide-semiconductor field effect transistors. *Appl Phys Lett*, 2014, 105, 142108
- [16] Karki U, Peng F Z. Precursors of gate-oxide degradation in silicon carbide MOSFETs. *2018 IEEE Energy Conversion Congress and Exposition*, 2018, 857



Lixin Tian received her PhD from Institute of Semiconductors, Chinese Academy of Sciences in 2017. She then joined Global Energy Interconnection Research Institute Co., Ltd. She is a senior engineer now. Her research focuses on high voltage silicon carbide power electronics devices.



Zechen Du received his master's degree from North China Electric Power University in 2021. He is now a research and development engineer of Smart Grid Research Institute Co., Ltd. The main research direction is the simulation and testing of high-voltage silicon carbide devices.



Fei Yang received his PhD from Institute of Semiconductors, Chinese Academy of Sciences in 2006. In 2011, he joined the Global Energy Interconnection Research Institute as professor. His research focuses on high voltage silicon carbide power electronic devices.