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Demonstration of 4H-SiC CMOS digital IC gates based on the mainstream 6-inch wafer processing technique

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Abstract: In this article, the design, fabrication and characterization of silicon carbide (SiC) complementary-metal-oxide-semiconductor (CMOS)-based integrated circuits (ICs) are presented. A metal interconnect strategy is proposed to fabricate the fundamental N-channel MOS (NMOS) and P-channel MOS (PMOS) devices that are required for the CMOS circuit configuration. Based on the mainstream 6-inch SiC wafer processing technology, the simultaneous fabrication of SiC CMOS ICs and power MOSFET is realized. Fundamental gates, such as inverter and NAND gates, are fabricated and tested. The measurement results show that the inverter and NAND gates function well. The calculated low-to-high delay (low-to-high output transition) and high-to-low delay (high-to-low output transition) are 49.9 and 90 ns, respectively.

Key words: SiC; CMOS; integrated circuit; inverter; NAND; metal interconnect

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1. Introduction

Although silicon carbide (SiC) power devices have been proven to be stable and reliable for high temperature operation, the present control and drive circuits are based on silicon material, which restricts the maximum operating temperature of the power electronics system[1]. Developing SiC integrated circuits (ICs) is beneficial for realizing the full potential of SiC material in high temperature applications[2–6]. Compared with other technology, the complementary-metal-oxide-semiconductor (CMOS) technology could achieve full rail-to-rail output voltage switching, low power losses and temperature-independent logic levels[7, 8]. Unfortunately, the reported SiC CMOS ICs in the literature are fabricated using specially developed technology, which is not compatible with the mainstream 4H-SiC power device processing technology.

Motivated by developing 4H-SiC based power ICs which integrates the control circuits and power device in a single chip, this article reports the implementation of fundamental CMOS-based digital gates based on 6-inch SiC wafer processing technology, in which the digital gates and power devices are fabricated simultaneously. The fundamental characteristics of the inverter and NAND gates are characterized and analyzed. The experimental results that are obtained by this work will serve as useful guides for driving the development of SiC-based power ICs.

2. Device fabrication

The CMOS circuit requires both N-channel MOS (NMOS) and P-channel MOS (PMOS) devices. To implement the SiC NMOS and PMOS while ensuring compatibility with the SiC power device processing technology, the CMOS configuration in Fig. 1 is adopted [7, 8]. The PMOS is formed directly in the drift layer, while the NMOS is fabricated in a P-well. The P-well also functions as a base layer for the SiC power MOSFET.

In fabricating the SiC power MOSFET, only one thick metal is used for the cell interconnect [9]. In this work, a metal interconnect strategy is proposed to implement the CMOS circuits. The proposed metal interconnect strategy is shown in Fig. 2. The polysilicon acts as the gate (G) and the ohmic metal is extended to the other side to form the source (S), as shown in Figs. 2(a) and 2(b), respectively. After depositing the interlayer dielectric, contact holes are etched, as shown in Fig. 2(c). After sputtering the thick Aluminum metal, the wet etching technique is used to form the three electrodes, as shown in Fig. 2(d). The fabrications of SiC NMOS and PMOS are thus finished. The channel length for both NMOS and PMOS is 2 μm. The gate oxide thickness is 50 nm.

High temperature and high energy aluminum implantations and nitrogen implantations are used to form the P-wells, P+ regions and N+ regions, respectively. The process conditions for the implantations are summarized in Table 1. The obtained doping profiles for these regions are shown in Fig. 3. The depth of P-well should be larger than that of N+ region because the NMOS is located in the P-well.

3. Results and discussions

Based on the mainstream 6-inch SiC wafer processing

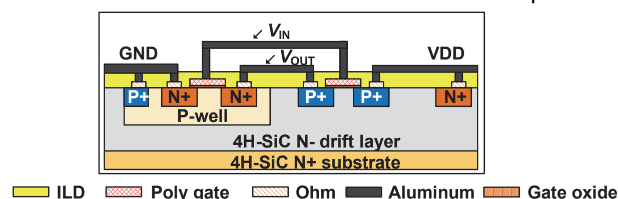

Fig. 1. (Color online) The CMOS circuit configuration that is used in this work

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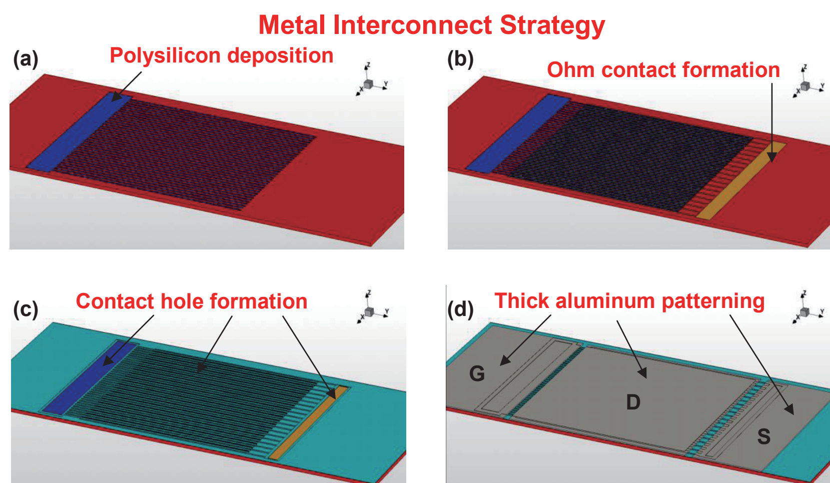

Fig. 2. (Color online) The proposed metal interconnect strategy for fabricating the SiC NMOS and PMOS devices.

Table 1. The temperature, dose and energy used in the fabrications for P-well, P+ region and N+ regions.

Item	Temperature (°C)	Energy (keV)
P-well	500	550
	500	360
	500	200
P+	500	320
	500	200
	500	40
N+	500	160
	500	130
	500	40

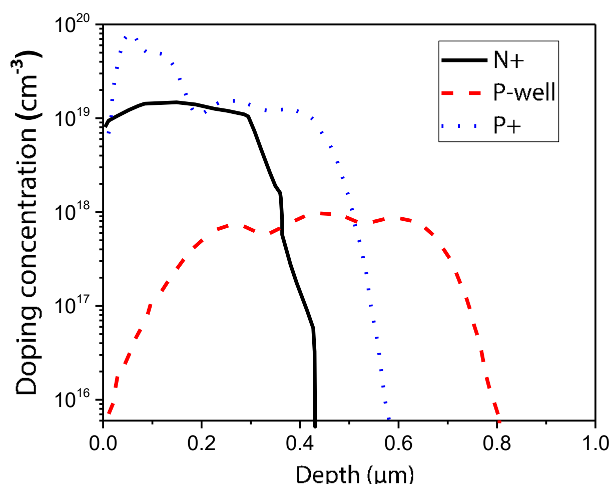

Fig. 3. (Color online) The doping profiles of N+, P-well and P+ regions obtained by process simulations through Synopsys Sentaurus.

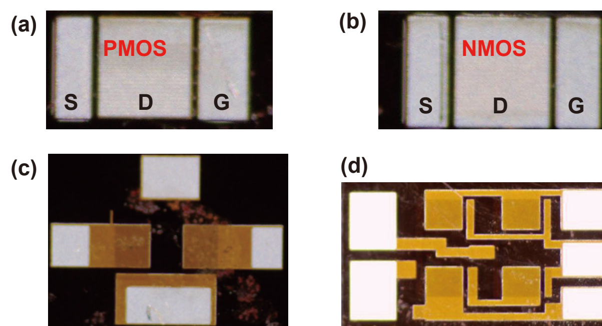

Fig. 4. (Color online) The fabricated SiC NMOS, PMOS and CMOS gates. (a) PMOS. (b) NMOS. (c) Inverter gate. (d) NAND gate.

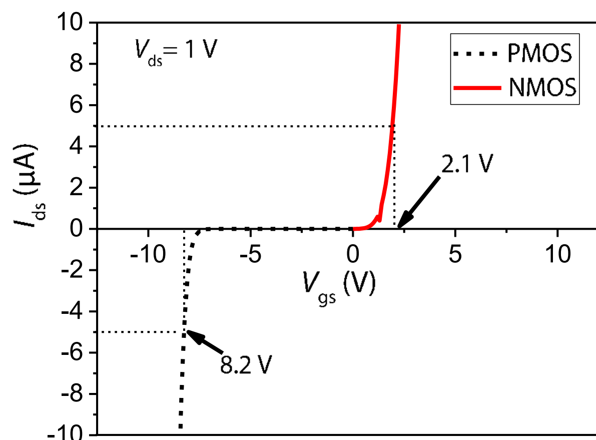

Fig. 5. (Color online) The measured transfer characteristics of the PMOS and NMOS.

technology, we realized the simultaneous fabrication of SiC digital gates and a SiC power MOSFET. Fig. 4 gives the photos of the fabricated SiC NMOS, PMOS and the CMOS gates. As shown in Figs. 4(a) and 4(b), the drain (D), gate (G) and source (S) of the NMOS and PMOS are clearly distinguished. The Inverter gate shown in Fig. 4(c) contains both PMOS and NMOS device, and the NAND gate in Fig. 4(d) integrates four devices. The measured transfer characteristics of the PMOS and NMOS are shown in Fig. 5. The typical threshold voltage V_{th} of the PMOS is 8.2 V while that of the NMOS is only 2.1 V. The asymmetry of V_{th} between PMOS and NMOS should be attributed to the unavoidable fixed charges located at the interface of SiC and SiO_2[10].

After bonding the fabricated inverter and NAND gates, the functions of the two gates are evaluated. The measured voltage transfer curves of the inverter gate at various V_{DD}s are shown in Fig. 6(a). The inverter gate functions are as expected. We also extract the inverter gain from the voltage transfer curves and the results are shown in Fig. 6(b). It is found that the inverter gain increases with V_{DD}. At a V_{DD} of 15 V, the inverter gain is larger than 50, which is beneficial for fabricating more complex integrated circuits, such as a multi-stage ring oscillator.

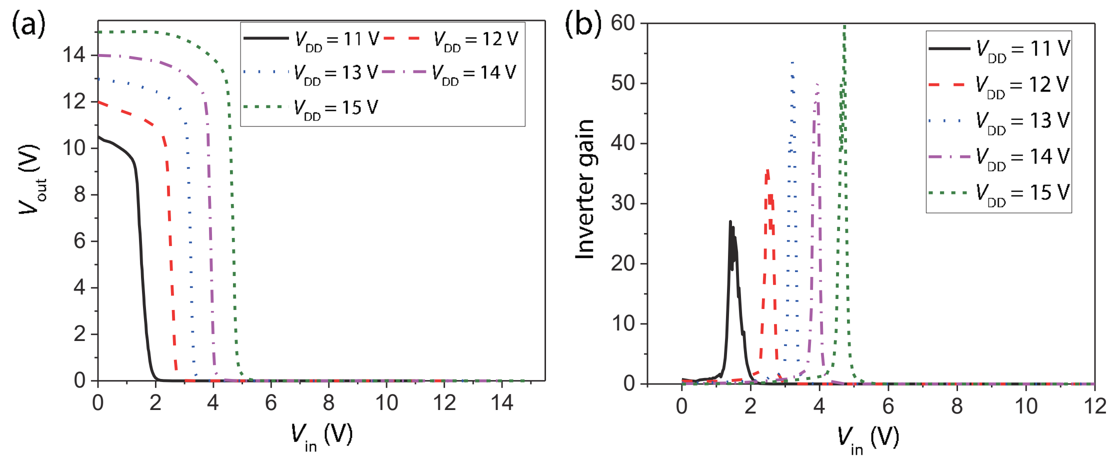

Fig. 6. (Color online) (a) The typical measured voltage transfer curves and (b) the extracted inverter gain of the fabricated Inverter gate.

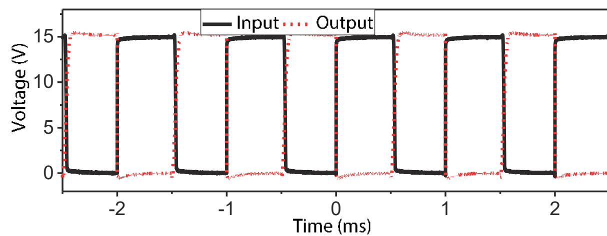

Fig. 7. (Color online) The measured switching input-output characteristics of the fabricated SiC Inverter gate.

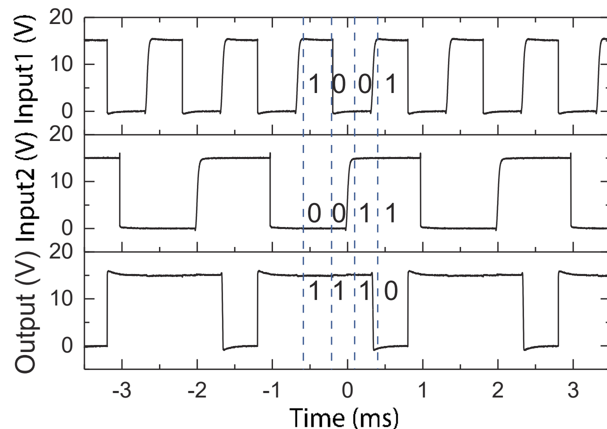

Fig. 8. (Color online) The measured switching input-output characteristics of the fabricated SiC NAND gate.

Fig. 7 give the typical measured input-output voltage curves of the inverter gate. The obtained waveform demonstrates that the inverter gate functions well. In addition, from the voltage curves, the calculated low-to-high delay t_{pLH} (low-to-high output transition) and high-to-low delay t_{pHL} (high-to-low output transition) are 49.9 and 90 ns, respectively. The measured dynamic switching characteristic of the NAND gate is shown in Fig. 8. Obviously, the obtained results verify the normal operation of the NAND gate.

The fabricated SiC power MOSFET is of a trench structure. The related experimental results have been reported in Ref. [11]. Based on the proposed metal interconnect strategy, the SiC IC gates and trench power MOSFET are fabricated on the same wafer. It is expected that SiC power ICs which integrate the SiC ICs and a power MOSFET will be realized in future work.

4. Conclusion

In this article, 4H-SiC CMOS digital gates are successfully fabricated based on the mainstream SiC processing technology. The functions of the inverter and NAND gate are verified through experimental measurements. Based on these fundamental gates, more complex SiC CMOS based integrated circuits can be fabricated. Moreover, the simultaneous fabrication of the SiC CMOS circuits and power MOSFET can be realized. Therefore, the results of this research can provide valuable guides for the future fabrication of power integrated circuits to realize the full potential of SiC power devices in high temperature applications.

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