

# A low-power high-quality CMOS image sensor using 1.5 V 4T pinned photodiode and dual-CDS column-parallel single-slope ADC

Wenjing Xu<sup>1,2</sup>, Jie Chen<sup>1,†</sup>, Zhangqu Kuang<sup>3</sup>, Li Zhou<sup>1</sup>, Ming Chen<sup>1</sup>, and Chengbin Zhang<sup>1</sup>

<sup>1</sup>Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China

<sup>2</sup>University of Chinese Academy of Sciences, Beijing 100049, China

<sup>3</sup>Will Semiconductor Co. Ltd., Shanghai 201210, China

**Abstract:** This paper presents a low-power high-quality CMOS image sensor (CIS) using 1.5 V 4T pinned photodiode (4T-PPD) and dual correlated double sampling (dual-CDS) column-parallel single-slope ADC. A five-finger shaped pixel layer is proposed to solve image lag caused by low-voltage 4T-PPD. Dual-CDS is used to reduce random noise and the nonuniformity between columns. Dual-mode counting method is proposed to improve circuit robustness. A prototype sensor was fabricated using a 0.11  $\mu\text{m}$  CMOS process. Measurement results show that the lag of the five-finger shaped pixel is reduced by 80% compared with the conventional rectangular pixel, the chip power consumption is only 36 mW, the dynamic range is 67.3 dB, the random noise is only  $1.55 e^{-}_{\text{rms}}$ , and the figure-of-merit is only  $1.98 e^{-}\cdot\text{nJ}$ , thus realizing low-power and high-quality imaging.

**Key words:** CMOS image sensor; 4T pinned photodiode; single-slope ADC; correlated double sample; counting method

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## 1. Introduction

CMOS image sensors (CISs) have been widely used in many application fields such as mobile phones and wearable devices. In recent years, the application of CIS has gradually expanded to the internet of things (IoT) and artificial intelligence (AI) fields. On the one hand, IoT and AI devices only have small batteries for energy support, yet they are expected to last weeks on a single charge. On the other hand, CIS serves as the eyes of the machine to see the world, which leads an increasing demand for high-quality imaging. Therefore, it is crucial to design both low-power and high-performance CISs<sup>[1, 2]</sup>.

The basic idea to reduce power consumption is to lower the supply voltage. The supply voltage of the CIS readout circuit is limited by the voltage of the pixels. Digital pixels are usually used to reduce the pixel voltage. In 2010 JSSC<sup>[3]</sup>, a digital pixel that works under 0.5 V was proposed but its dynamic range was only 21.3 dB. Later in 2015 JSSC<sup>[4]</sup> and 2021 JSSC<sup>[2]</sup>, although the dynamic range has been increased to 42 and 52 dB, respectively, there was still a gap compared with high-quality imaging.

High-quality imaging usually requires the use of active pixels. 1.5 V 3T pixel has been proposed in 2003 TED<sup>[5]</sup>. But compared with 4T pixel, 3T pixel cannot achieve true correlated double sampling, and thus the random noise is larger. The 4T pinned photodiode (4T-PPD) active pixel is the most

commonly used pixel structure for high-performance CIS. Traditionally, the supply voltage of 4T-PPD is greater than 2.8 V. When the voltage drops, the electrons far away from the transfer gate lack lateral electric field and stay in the pixel, causing image lag. In 2016 JSSC<sup>[6]</sup>, 4T-PPD active pixel was designed to work at 0.9 V by improving the pixel timing; however, the random noise was as high as  $83 e^{-}_{\text{rms}}$ , and the dynamic range was only 50 dB.

Therefore, how to realize low-voltage 4T-PPD while maintaining high image quality is a critical issue. In this work, a low-power high-quality CIS using 1.5 V 4T-PPD and dual correlated double sampling (dual-CDS) column-parallel single-slope ADC (SS-ADC) is proposed. A five-finger shaped pixel layer instead of traditional rectangular shape is used to solve image lag caused by low-voltage 4T-PPD. Dual-CDS is used to reduce the random noise and the nonuniformity between columns. The dual-mode counting method is used to improve the circuit's robustness.

## 2. Overall architecture

Among several types of column-parallel ADCs, SS-ADC<sup>[7-10]</sup> is clearly the most widely used because a SS-ADC can be implemented using a very simple column circuit, which mainly consists of a single comparator and a counter. Moreover, this simple column circuit also makes it relatively easy to ensure uniformity between columns, and thus minimizes the readout noise.

Fig. 1 shows the architecture of the proposed CIS. The pixel array is  $1288 \times 728$  and the pixel pitch is  $2.8 \mu\text{m}$ . The Row-decoder sequentially selects a single row line for signal readout processing. The signal charges generated at the PPD

Correspondence to: J Chen, [jchen@ime.ac.cn](mailto:jchen@ime.ac.cn)

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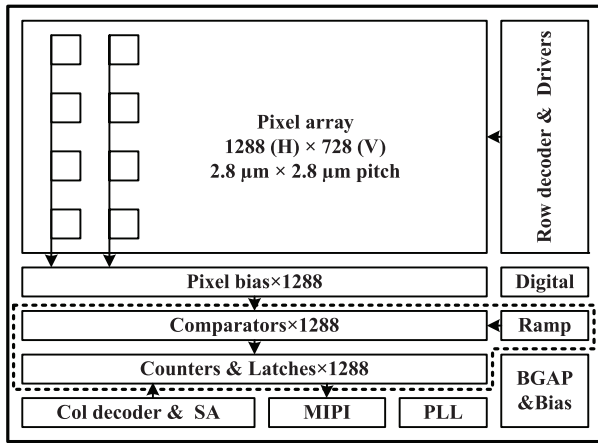


Fig. 1. Block diagram of the overall architecture.

are converted to the signal voltage on the vertical signal lines. The comparator array compares the readout signals with the ramp generator output. The comparator changes at the timing when the ramp voltage reaches the signal voltages. Then, the counter stops counting and the latch array latches the counter outputs. The Col-decoder sequentially selects latched ADC value, and the sense amplifier (SA) outputs 10 b straight binary data to MIPI interface. PLL provides high-speed clock for digital control circuit and MIPI circuit.

### 3. Design of the five-finger shaped 1.5 V 4T-PPD

A typical 4T-PPD active pixel<sup>[10]</sup> is shown in Fig. 2. The 4T-PPD consists of the PPD, transfer gate (TG), floating diffusion (FD) and three transistors. A PPD is a device made by a n-well buried in a p-substrate, and a thin p+ layer covers the n-well. The pinned photodiode has no contacts, and the photo-generated electrons are transferred to the FD node by the operation of the TG. Due to physic limitations of the PPD and the TG structure, transferring all of the electrons completely from the photodiode is very hard, especially for low-voltage PPD.

The dotted line in Fig. 2 is the charge transfer path when a high voltage is applied to the  $V_{TG}$ . Traditionally,  $V_{TG}$  is greater than 2.8 V, so that a fringe field from the edge of the PPD (marked as A) to TG (marked as C) is formed, pushing the electrons to TG completely. When  $V_{TG}$  drops, due to the absence of the fringe field, the electrons moving from A to B mainly rely on thermal diffusion and self-induced drift, which takes a long time. Finally, the electrons are left behind in the PPD, and these remaining electrons create image lag.

To reduce the image lag caused by low-voltage PPD, 2.8  $\mu\text{m}$  small pixel pitch is used to reduce the electron diffusion distance. To further accelerate the movement of photo-generated charges without changing the process steps and conditions, the shape of the PPD layer might be changed to create an electric field from the edge of PPD to TG. In previous studies<sup>[11–15]</sup>, triangle, W-shape, trapezoid, and L-shape PPD have been reportedly, but all these designs aim at large-sized pixels. For small-sized pixels, the PPD layer should not be cut too much; otherwise, it would affect the full-well capacity and reduce the dynamic range.

Therefore, for the small pixel design in this paper, the tradi-

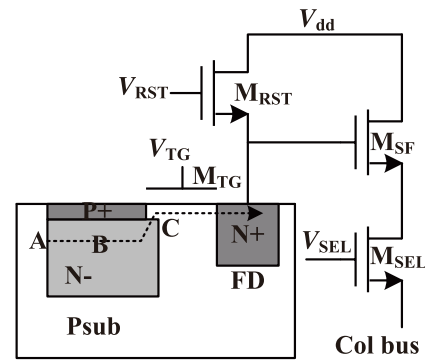


Fig. 2. 4T-PPD architecture.

tional rectangular PPD layer shown in Fig. 3(a) is improved into a five-finger PPD layer, which can be seen in Fig. 3(b). The number five is the result of a balance between full-well capacity and the transfer speed. If the number of fingers is too small, then too much of the photosensitive area will be cut, which will greatly reduce the full well capacity. In contrast, if the number of fingers is too large, then the inclination angle of each finger will not be enough, which will decrease the charge transfer speed. The cutting method is as follows. First, the center of the TG is marked as point C, the black rectangular frame is the farthest area from point C, and thus the area is cut out. Then, the four arrow lines divide 90° into five equal parts, and the length of each arrow line is basically the same. This design is developed to ensure that the time for the photo-generated charges in each area to move to the TG is nearly the same. The angles of the five fingers are almost 110°, based on the experiment results reported in Ref. [12]. The area of the PPD layer that is finally cut off accounts for 14% of the total rectangular area of 4.27  $\mu\text{m}^2$ .

Compared with the conventional rectangle shaped PPD shown in Fig. 3(a), the width of the photodiode becomes narrower the farther away from transfer gate. The five-finger shaped PPD utilizes the narrow width effect to create the extra electrical field in the direction of the charge transfer. This causes more electrons to be pulled out of the PPD. The potential profile of a rectangular PPD is shown in Fig. 3(a). There is no potential gradient forcing electrons because there is no narrow channel effect. A potential gradient is formed in the five-finger shaped PPD as shown in Fig. 3(b). The proposed five-finger shaped PPD can not only accelerate the electrons transfer from PPD to TG but can also meet the requirements of full-well capacity and dynamic range due to the small cropped area.

### 4. Design of the column-parallel SS-ADC

The column circuit of the SS-ADC is shown in Fig. 4. To further reduce power consumption, the comparator is implemented by a two-stage comparator. The pixel output signal  $V_{\text{pixel}}$  and ramp signal  $V_{\text{ramp}}$  are, respectively, connected to the negative and positive input terminals of the first-stage comparator through capacitors C1A and C1B. In this way, both  $V_{\text{pixel}}$  and  $V_{\text{ramp}}$  are ac-coupled, thus voltages of  $V_{\text{pixel}}$  and  $V_{\text{ramp}}$  are not limited by the first-stage input common mode voltage. Moreover, a fully differential first stage can avoid systematic offset. A capacitor C2 is added between the first-stage and the second-stage to eliminate the offset of the first-stage.

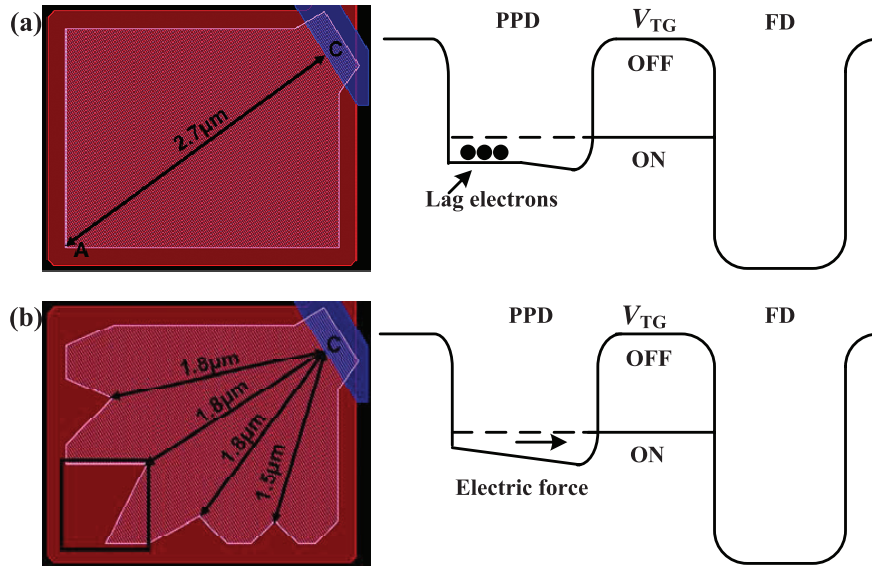


Fig. 3. (Color online) PPD shape and potential profile: (a) conventional rectangle shaped, (b) proposed five-finger shaped.

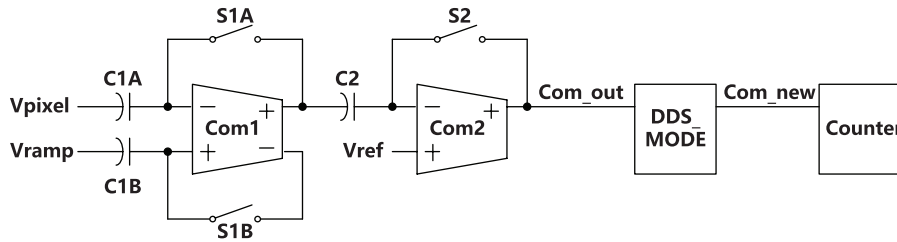


Fig. 4. Column circuit of the SS-ADC.

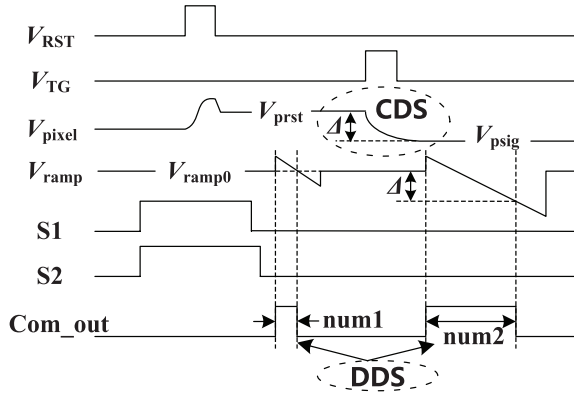


Fig. 5. Timing diagram for dual correlated double sampling.

The output signal of comparator Com<sub>out</sub> becomes Com<sub>new</sub> after passing the DDS<sub>MODE</sub> module. The column counter, composed of ripple counter, performs the A/D conversion by counting the number of clocks until the comparator output changes. A ripple counter has the advantage of not needing to be synchronized with the high-speed clock.

#### 4.1. Dual correlated double sampling

To reduce random noise and the nonuniformity between columns, dual-CDS which includes analog correlated double sampling and digital double sampling is used. Fig. 5 shows the timing diagram for the dual-CDS operation.

The dual-CDS operation is as follows. 1) Switches S1 and S2 are turned on, the comparator is reset. When the control signal V<sub>RST</sub> is high, the pixel reset level V<sub>prst</sub> appears at the pixel output. Then S1 and S2 are turned off. Non-overlap S1

and S2 are designed to reduce non-idealities introduced by clock feedthrough and charge injection. At this time, the voltages of the negative and positive input terminals of the comparator can be expressed as

$$V_{\text{com,inn}} = V_{\text{cm}}, \quad (1)$$

$$V_{\text{com,inp}} = V_{\text{cm}} + V_{\text{os}}, \quad (2)$$

where  $V_{\text{cm}}$  is the common-mode voltage of the comparator, and  $V_{\text{os}}$  is the comparator offset. 2) Then, V<sub>ramp</sub> starts to change near V<sub>ramp0</sub>, the positive input terminal of the comparator can be expressed as

$$V_{\text{com,inp}} = V_{\text{cm}} + V_{\text{os}} - (V_{\text{ramp0}} - V_{\text{ramp}}). \quad (3)$$

The difference between the two ends of the comparator is derived by Eq. (3) minus Eq. (1) as

$$\Delta V_{\text{com1}} = V_{\text{com,inp}} - V_{\text{com,inn}} = V_{\text{os}} - (V_{\text{ramp0}} - V_{\text{ramp}}). \quad (4)$$

When  $\Delta V_{\text{com1}} > 0$ , the comparator flips, the ripple counter stops counting, and the count value is num1. 3) When the control signal V<sub>TG</sub> is high, the pixel signal level V<sub>psig</sub> appears at the pixel output. And the negative input terminal of the comparator can be expressed as

$$V_{\text{com,inn}} = V_{\text{cm}} - (V_{\text{prst}} - V_{\text{psig}}). \quad (5)$$

The difference between the two ends of the comparator is derived by Eq. (3) minus Eq. (5) as

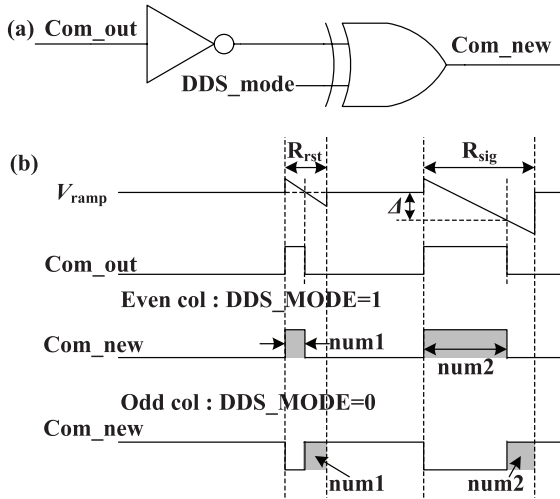


Fig. 6. Dual-mode counting method: (a) circuit, (b) timing diagram.

$$\begin{aligned} \Delta V_{com2} &= V_{com,inp} - V_{com,inn} \\ &= V_{os} + (V_{prst} - V_{psig}) - (V_{ramp0} - V_{ramp}). \end{aligned} \quad (6)$$

When  $\Delta V_{com2} > 0$ , the comparator flips, the ripple counter stops counting, and the count value is  $num2$ . The final 10-bit counting number  $D_{out}$  is given as

$$D_{out} = num2 - num1. \quad (7)$$

Analog CDS is used to eliminate the offset of the pixel. The offset of the comparator and counter variations that cause A/D conversion error are corrected by digital CDS. Due to the use of the digital CDS method, the conversion time is increased by 20% because of the time for  $num1$  counting. To achieve 30 fps at  $1288 \times 728$ , the clock frequency of the ripple counter is 72 MHz. After dual-CDS subtraction, the system non-idealities are well canceled.

#### 4.2. Dual-mode counting method

The total number of counts directly relates to the difference between the pixel reset level and signal level. In extreme cases, when the scene is complete bright, all column-parallel counters start counting at the same time and do not stop until they are all full. On one hand, this introduces a lot of spikes in the substrate, resulting in supply noises. On the other hand, the high-power current flows from the ADC supply may pull down the supply level significantly due to parasitic resistance of the chip and package, which causes the chip to fail.

To solve the problem, a dual-mode counting method is proposed (i.e., even-column and odd-column counters start and stop counting at different times). As shown in Fig. 4, the output of the comparator connects to the counter through the DDS\_MODE module, and the circuit of the DDS\_MODE module is shown in Fig. 6(a). The proposed counting algorithm is illustrated in Fig. 6(b). When  $DDS\_MODE = 1$ ,  $Com\_new$  is the same as  $Com\_out$ , and the final  $D_{out}$  expression of even columns is the same as Eq. (8). When  $DDS\_MODE = 0$ ,  $Com\_new$  is the opposite of  $Com\_out$ , the odd columns start counting when the even columns stop, and stop counting when the  $V_{ramp}$  stops changing. The final  $D_{out}$  expression of the odd columns is given as

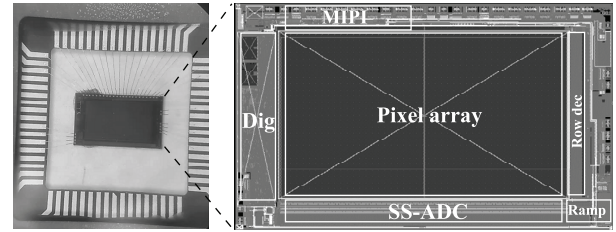


Fig. 7. Chip photograph and layout.

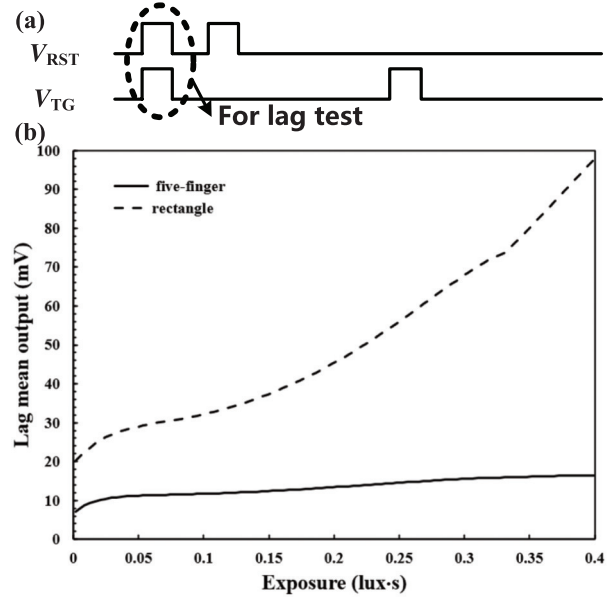


Fig. 8. (a) Timing diagram for lag test. (b) Measured lag curves with different shaped PPD.

$$D_{out} = (R_{sig} - num2) - (R_{rst} - num1). \quad (8)$$

With this counting method, whether the scene is complete dark or bright, the digital power supply level and ground level variation are almost the same, and thus circuit robustness is improved.

#### 5. Measurement results

A prototype sensor was fabricated using a  $0.11 \mu\text{m}$  1P3M CMOS process. Fig. 7 shows a photograph and layout of the chip. The size of the whole chip is  $4.8 \text{ mm (H)} \times 2.9 \text{ mm (V)}$ . The pixel array is  $1288 \times 728$  and the pixel pitch is  $2.8 \mu\text{m}$ .

The test pixel in chip3 is rectangle shaped, as shown in Fig. 3(a), while the test pixel in chip4 is five-finger shaped as shown in Fig. 3(b). The doping profiles of chip3 and chip4 are the same. Fig. 8 compares the measured lag performance of two different pixel designs. It can be seen that the lag of the rectangle shaped pixel gradually increases with the increase of light intensity, while the lag of the improved five-finger shaped pixel almost does not change. At the maximum exposure, the lag of the five-finger shaped pixel is reduced by 80% compared with the conventional rectangle shaped pixel.

In the high-light region, the full-well capacity of the five-finger PPD decreases from  $647 \text{ mV}$  ( $5119 e^-$ ) to  $623 \text{ mV}$  ( $4928 e^-$ ) compared with the rectangle shaped pixel because the area of the PPD layer is reduced by 14%. However, CIS only works in the linear region of the photoelectric response curve, so a slight decrease in the full-well capacity will not af-



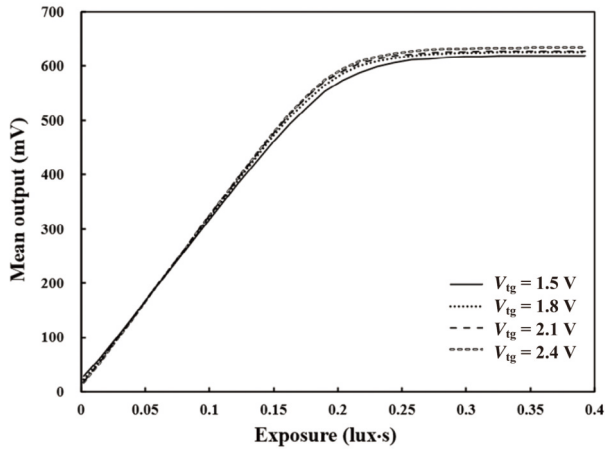


Fig. 9. Measured photo response curves of five-finger shaped PPD with different transfer gate voltage.

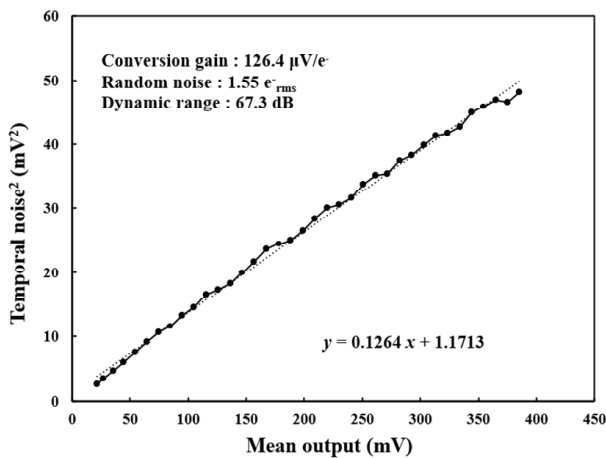


Fig. 10. Measured photon transfer curve.

fect the CIS. The dark current values for five-finger and rectangle shaped pixels are 5.01 and 5.06 mV/s respectively.

Fig. 9 shows the measured photo response curves of five-finger shaped PPD with different transfer gate voltage. The photo response curves are nearly the same by changing  $V_{TG}$ . This is because the five-finger shaped pixel improves the electrons transfer efficiency, thus almost complete transfer can be realized (even at a low voltage of 1.5 V).

Fig. 10 shows the measured photon transfer curve versus input light intensity. A dark random noise of  $1.55 e^-_{rms}$  is achieved with a pixel conversion gain of  $126.4 \mu V/e^-$ . This chip achieves a dynamic range of 67.3 dB.

A sample image taken with the CIS at 1.5 V analog and 1.2 V digital supply voltage is shown in Fig. 11. Image lag due to the 1.5 V 4T-PPD is negligible at 30 fps.

To verify the validity of the dual-mode counting method, the test is carried out as follows. The entire chip is illuminated by a parallel light source, while the lower left-hand and lower right-hand corners of the photosensitive area are covered with insulating black tape. The pixel arrays covered by black tape are both  $472 \times 345$ . The measured digital codes of the 644th column with or without dual-mode counting is shown in Fig. 12. When dual-counting method is off, the quantization environments between the first 383 lines and the last 345 lines of the 644th column are inconsistent, so the code values have a minimum deviation of 2 LSB. When



Fig. 11. Captured image from the fabricated sensor.

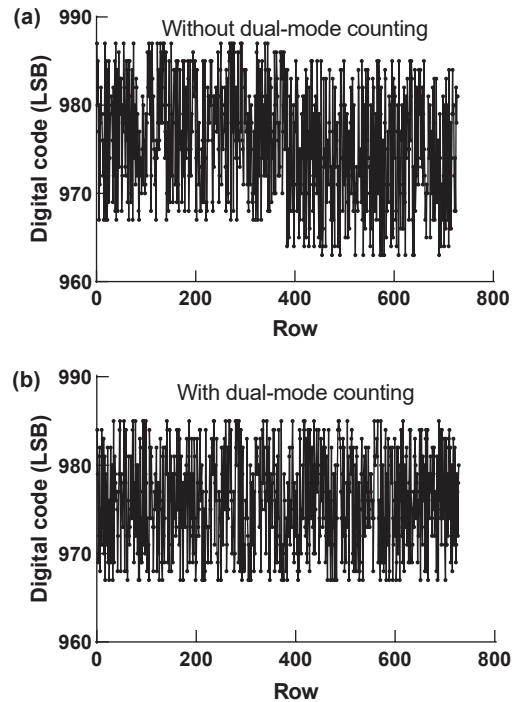


Fig. 12. (a) Measured Digital codes of the 644th column without dual-mode counting. (b) Measured Digital codes of the 644th column with dual-mode counting.

dual-counting method is on, the code value consistency between the first 383 lines and the last 345 lines of the column 644th is better.

Table 1 shows the measured power consumption at 30 fps. Because a low-voltage 1.5 V 4T-PPD is used, the supply voltage of the subsequent analog readout circuit can also be 1.5 V, which greatly reduces the power consumption of the whole chip. To further reduce power consumption, the supply voltage of the digital circuit is 1.2 V, and the I/O PAD supply is 1.8 V. The measured total power consumption is only 36 mW.

Table 2 shows a performance summary of the proposed CIS and a comparison with other works. To evaluate the energy efficiency of an image sensor, FoM can be calculated as follows<sup>[16]</sup>:

$$\text{FoM} = \frac{\text{Power} \times \text{Noise}}{\text{Frame rate} \times \text{Total pixel number}} \quad (9)$$

Table 1. Chip power consumption.

Parameter	Voltage (V)	Current (A)	Power consumption (mW)
Pixel and analog	1.5	10.35	15.525
Digital	1.2	16.96	20.352
I/O	1.8	0.03	0.054
Sum			35.931

Table 2. Comparison with other published CIS.

Parameter	This work	JSSC <sup>[6]</sup>	TCASI <sup>[17]</sup>	Sensor <sup>[18]</sup>	JSSC <sup>[4]</sup>	
Process (nm)	110	110	110	90	65	
Pixel pitch ( $\mu\text{m}$ )	2.8	5.0	6.5	5.6	4.0	
Pixel type	4T PPD	4T PPD	4T PPD	4T PPD	Digital	
Pixel resolution	1288 $\times$ 728	640 $\times$ 480	320 $\times$ 240	128 $\times$ 128	960 $\times$ 720	128 $\times$ 128
Frame rate (fps)	30	15	15	228	35	32
Power supply (V)	1.5/1.2	3.3/1.8	0.9	3.3/1.5	2.8/1.5	0.5
Dynamic range (dB)	67.3	69	50	68.9	66.7	42
Power consumption (mW)	36	2.28	0.0455	40	28	0.0088
Random noise ( $e^-_{\text{rms}}$ )	1.55	5.5	83.7	3.25*	3.73*	416
FoM ( $e^- \cdot \text{nJ}$ )	1.98	2.72	3.31	34.8	4.32	6.98

\* For fair comparison, conversion gain is assumed by  $126.4 \mu\text{V}/e^-$ .

This work achieves a FoM of  $1.98 e^- \cdot \text{nJ}$ . Compared with previous works, the proposed CIS realizes low-power by using 1.5 V 4T-PPD, while maintaining high image quality.

## 6. Conclusion

This work presents a low-power high-quality CIS using 1.5 V 4T-PPD and column-parallel SS-ADC. A five-finger shaped pixel layer is proposed to solve image lag caused by low-voltage 4T-PPD. Dual correlated double sampling is used to reduce random noise and the nonuniformity between columns. To improve circuit robustness, dual-mode counting method is proposed. Measurement results show that the lag of the five-finger shaped pixel is reduced by 80% compared with the conventional rectangular pixel, the chip power consumption is only 36 mW, the dynamic range is 67.3 dB, the random noise is only  $1.55 e^-_{\text{rms}}$ , and the FoM is only  $1.98 e^- \cdot \text{nJ}$ . The proposed CIS realizes low-power by using 1.5 V 4T-PPD while maintaining high image quality, which is suitable for IoT and AI applications.

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**Wenjing Xu** received her B.E. and M.E. from Tianjin University, China, in 2010 and 2013, respectively. She is currently working towards a PhD at the Institute of Microelectronics of Chinese Academy of Science. Her research interests are CMOS image sensors and analog circuit design.



**Jie Chen** received his B.E. degree from the Harbin Engineering University, Harbin, China in 1986, and the M.E. and PhD degrees from the University of Electro-Communications (UEC), Tokyo, Japan in 1991 and 1994, respectively. In 2001, he was selected as a scientist of “100 Talents Program” by Chinese Academy of Sciences (CAS). He is now a Director Professor of the Institute of Analog Integrated Circuits and Signal Processing Microelectronics, CAS and a Professor of the Graduate School of CAS. His current research interests include SOC design for software-defined-radio (SDR), digital communications (CDMA and OFDM) and data compression.