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Simulation of MoS_2 stacked nanosheet field effect transistor

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Abstract: Transition metal dichalcogenides are nowadays appealing to researchers for their excellent electronic properties. Vertical stacked nanosheet FET (NSFET) based on MoS_2 are proposed and studied by Poisson equation solver coupled with semi-classical quantum correction model implemented in Sentaurus workbench. It is found that, the 2D stacked NSFET can largely suppress short channel effects with improved subthreshold swing and drain induced barrier lowering, due to the excellent electrostatics of 2D MoS_2. In addition, small-signal capacitance is extracted and analyzed. The MoS_2 based NSFET shows great potential to enable next generation electronics.

Key words: MoS_2; stacked nanosheet GAA; TCAD simulation

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1. Introduction

According to the 2021 International Roadmap for Devices and Systems (IRDS), gate-all-around (GAA) transistor will replace FinFET from 3 nm technology node, and it will apply to 1 nm technology node. In the next step, the goal of scaling down will be not only the decreased leakage but also the decreased power. And the 3D vertical architectures including 3D heterogeneous integration will become the mainstream technology to reduce power consumption. To continue Moore's law, not only increasing circuit integration degree through device scaling down, but also power scaling and switching speed improvement, are necessary. Stacked NSFET is a promising candidate for future sub-3nm technology node because of better electrostatic integrity, short channel immunity and therefore better power scaling performance[1–3].

However, it is projected that, physical channel length, i.e., gate length (L_G), would saturate around 12 nm due to worsening electrostatics. It can be inferred that planar size scaling by GAA structure is not able to sustain available performance. Accordingly, 2D semiconductors such as MoS_2 has nowadays been regarded as promising alternative option for next generation semiconductor, for their excellent electronic properties[4–7] and regarded she promising candidate.

There are abundant researches on 2D MoS_2 in recent years, due to its low dielectric constant, large band gap, valuable effective mass and dangling bond free surface[8]. These benefits can help achieve small leakage current and great switching characteristics. MoS_2 transistors with ultra-scaled physical gate lengths and channel lengths realized by various cleverly designed experiments have been demonstrated and studied, exhibiting short channel effects (SCEs) more or less respectively. The inevitable degraded performances also emerge in MoS_2 FET when device sizes scale down to nanometers[9, 10]. Contacts with 2D semiconductors fabricated by normal metal deposition process normally suffer from large contact resistance due to Fermi-level pinning effect, and experimental contaminations could also induce reduced 2D material quality in transfer process at the same time[11–14]. To investigate the potential advantages of MoS_2 over bulk silicon (Si), keeping intrinsic material properties and assuming ideal contact are needed.

In the following, to capture the ideal ultimate performance of MoS_2 FET, we will proceed as follows: First, we will begin with first-principle calculation for monolayer MoS_2; then, the obtained physical parameters will be delivered to Sentaurus to replace original values in parameter file; finally, the comparison between the bulk and 2D materials is fully conducted and results are concluded.

2. Method

It has been reported that exporting physical parameters calculated by density functional theory (DFT) into Sentaurus tool is an effective method to match quantum approach while computational cost can be largely reduced[15]. Thus, DFT calculations based on Perdew-Burke-Ernzerhof (PBE) and generalized gradient approximation (GGA) functionals are conducted in the Quantum ATK 2020 code, to obtain reliable physical results. The real-space mesh cutoff is set at 55 Hartree, while the k-points sampling is set as 20 × 20 × 1. As in Fig. 1, the K and Q conduction band valleys with an energy difference can be observed. Then band gap (E_G) of 1.78 eV, electron effective mass (m_e*) of 0.501 eV and hole effective mass (m_h*) of 0.588 eV are extracted from the conduction band minimum (CBM) and valence band maximum (VBM).

Fig. 2(a) shows the schematic structure of NSFET. Corresponding device structure is built in Sentaurus Structure Editor (Fig. 2(b)). The width of nanosheet is set as 10 nm in all conditions, and channel thickness is 5 nm for Si and 0.65 nm for MoS_2. To focus on the material itself, heavily doped source

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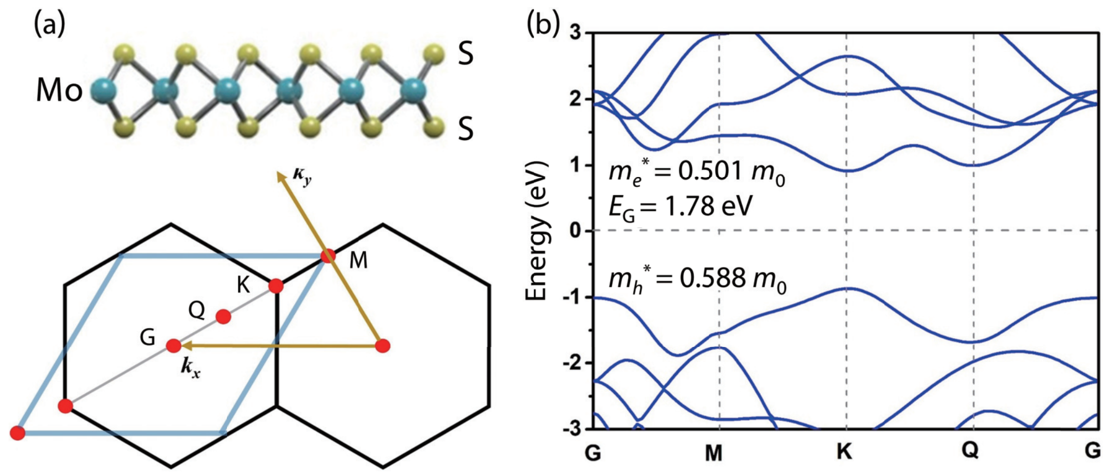

Fig. 1. (Color online) Energy band structures of MoS_2 unit cell simulated with DFT showing the high symmetry points and a band gap E_G = 1.78 eV.

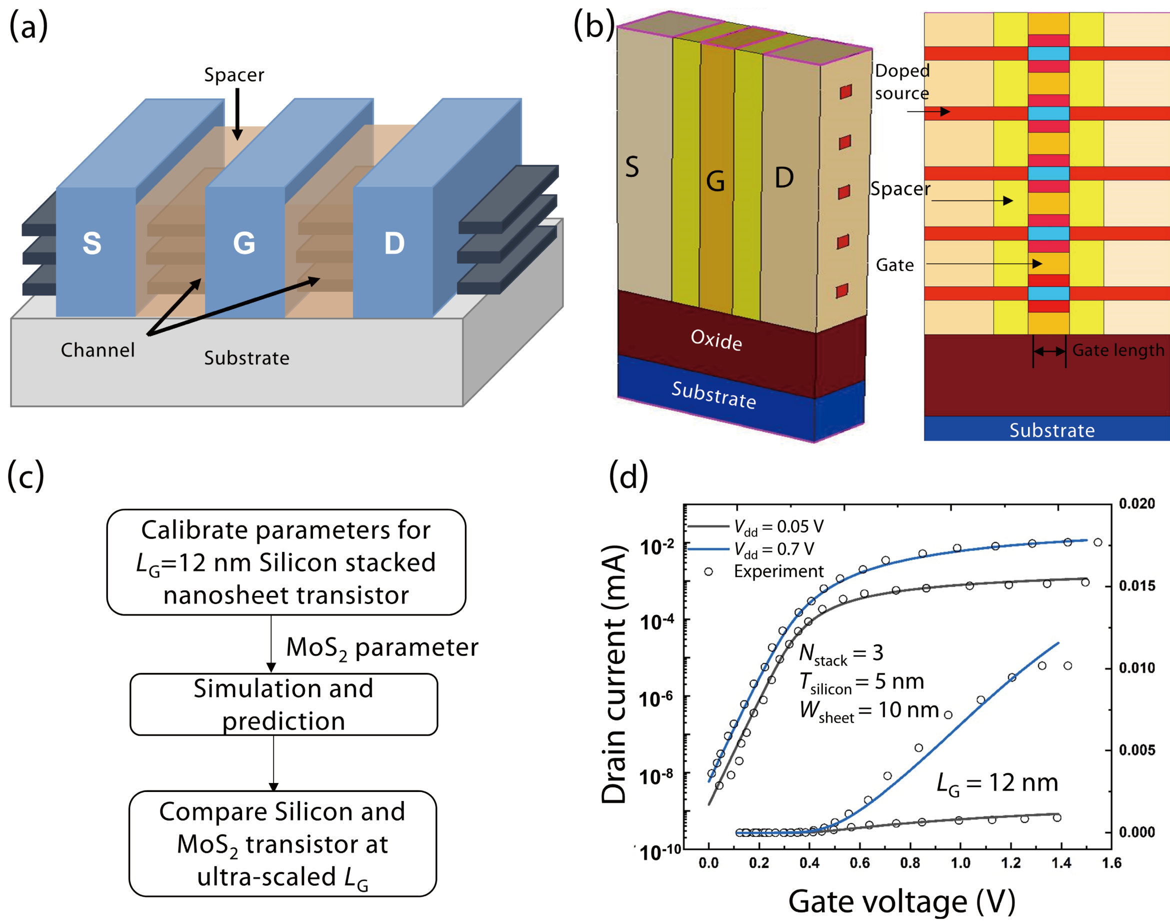

Fig. 2. (Color online) (a) Schematic diagram of a 3-stacked NSFET. (b) Bird eye view and cross-sectional view along the channel of simulated structure in Sentaurus. (c) Simulation framework of this work. (d) Calibration of transfer curves to experimental data in log and linear form. Experimental data are from a 3-stacked NSFET (L_G = 10 nm).

and drain in MoS_2 are defined, and then the devices work in inversion mode. The underlap region and spacer retain the same for both scenarios.

The considered material properties contain the value of bandgap (E_G), affinity (χ), mobility (μ), dielectric constant (ε), and the effective mass of hole (m_h^*) and electron (m_e^*). These material physical parameters are delivered to the parameter file to simulate the transport characteristics (Fig. 2(c)).

Calibration to experimental Si-based 3-stacked NSFET with 12 nm L_G was conducted at first by including Density Gradient model, Shockley Read Hall model and Oldslotboom model, as well as mobility models of High Field Saturation and Enormal[2, 16]. The transfer curves are then fitted with experimental data (Fig. 2(d)). Leveraging the calibrated physical model parameters, we studied the 2D MoS_2 stacked NSFET and try to figure out the improvement brought by using the material parameters of MoS_2. Table 1 summarizes the parameters used in this work.

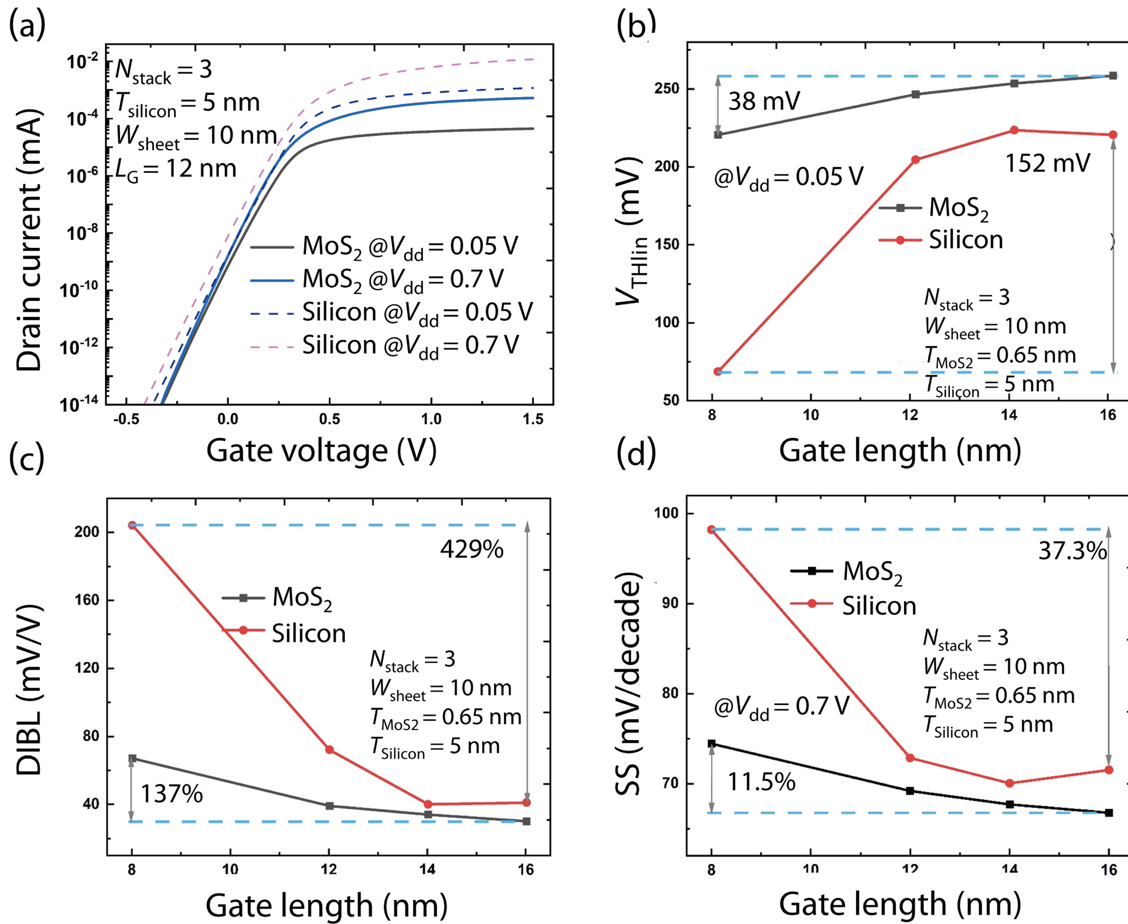

Fig. 3. (Color online) Electrostatic performance comparison of Si and MoS_2 based 3-stacked NSFET. (a) Transfer characteristics. (b) Roll-off. (c) DIBL. (d) SS.

Table 1. Parameters used in this work.

E_G (eV)	M (cm²/(V·s))	m_e^*	m_h^*	T (nm)	χ (eV)	ε
1.78	100	~0.501m_0	~0.588m_0	0.65	4.2	4

3. Results and discussion

With the imported physical parameters of MoS_2 modified, the transfer characteristics are compared in the same structure with channel of Si of 5 nm thickness and monolayer MoS_2 of 0.6 nm thickness. The materials and geometrical parameters remain the same only with the material and geometries of channel changed. The MoS_2 NSFET exhibits two-orders reduced on current, which can be ascribed to the low mobility of MoS_2 and reduced gate capacitance. Large threshold (V_{th}) roll-off can be observed for Si-based NSFET (Fig. 3(b)). Moreover, it is found that subthreshold swing (SS) and drain induced barrier lowering (DIBL) of Si-based 3-stacked NSFETs all rise rapidly at L_G = 8 nm, which make the device not suitable for application (Figs. 3(c) and 3(d)). The SS and DIBL are increased by ~37.3% and ~429% compared to original value when the L_G scales from 16 to 8 nm. Similar phenomena can be found in Refs. [17–19]. However, MoS_2 NSFET shows great short channel immunity, promising for extending the gate length to 8 nm without severe short channel effects.

In a transistor, the intrinsic and parasitic capacitance limit the drive capability and switching speed of the device[19]. Increasing the gate oxide thickness leads to poor electrostatics. Alternatively, the ultra-thin thickness and low dielectric of monolayer MoS_2 are supposed to induce channel capacitance (C_s) reduction[20]. Using similar structure with the same oxide capacitance C_{ox}, the small-signal gate capacitances (C_G) were extracted. As shown in Fig. 4(a), the utilization of monolayer MoS_2 brings about ~20% C_s reduction, which can be mostly attributed to the C_s part. Similarly, C_G increases with NS widths (Fig. 4(b)) and number of stacks (N_{stack}) (Fig. 4(c)). The extracted total C_G at V_{DS} = 0 V is greater than at C_G at V_{DS} > 0 V (Fig. 4(d)). Gate-to-drain capacitance C_{GD} has the similar trend. The results demonstrate the advantages of MoS_2 in high-speed circuits.

4. Conclusion

In this work, we investigated the stacking NS transistors with a MoS_2 channel via a semi-classical simulation. We gave a quantified comparison for MoS_2 and Si in terms of electrostatic integrities and scalability at ultra-scaled gate length. Due to the excellent electronic properties and ultra-thin thickness, 2D semiconducting MoS_2 has high scalability and is promising in high-speed application.

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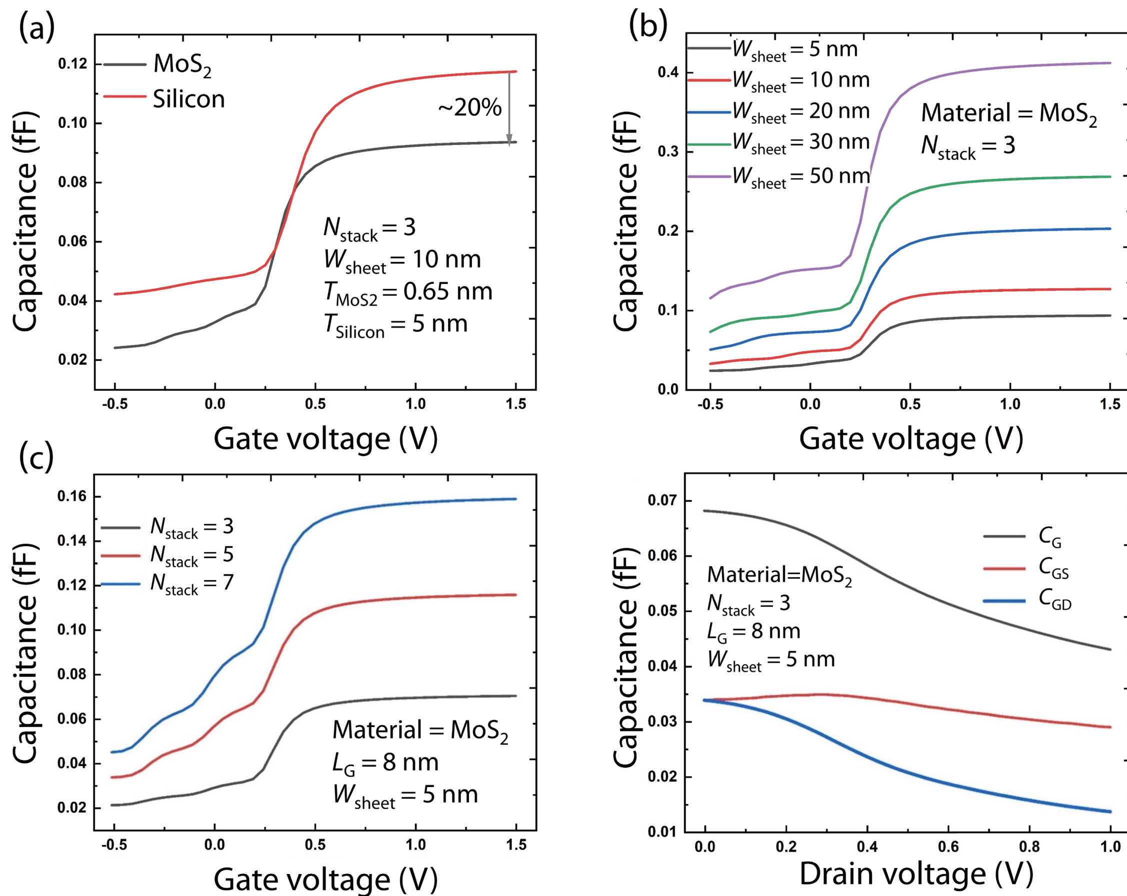

Fig. 4. (Color online) (a) Comparison of Si and MoS_2 based 3-stacked NSFET in terms of C_G– V_G characteristic. (b) C_G vs V_G with different sheet widths. (c) C_G vs V_G with different number of stacks. (d) C_G, C_{GS}, C_{GD} vs V_D, separately.

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