REVIEWS

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Trending IC design directions in 2022

Chi-Hang Chan[1], Lin Cheng[2], Wei Deng[3], Peng Feng[4], Li Geng[5], Mo Huang[1], Haikun Jia[3], Lu Jie[3], Ka-Meng Lei[1], Xihao Liu[5], Xun Liu[6], Yongpan Liu[3], Yan Lu[1, †], Kaiming Nie[7], Dongfang Pan[2], Nan Qi[4], Sai-Weng Sin[1], Nan Sun[3], Wenyu Sun[3], Jiangtao Xu[7], Jinshan Yue[3], Milin Zhang[3], and Zhao Zhang[4]

[1]University of Macau, Macau 999078, China
[2]University of Science and Technology of China, Hefei 230026, China
[3]Tsinghua University, Beijing 100084, China
[4]Institute of Semiconductors, Chinese Academy of Sciences, Beijing 100083, China
[5]Xi'an Jiaotong University, Xi'an 710049, China
[6]Chinese University of Hong Kong, Shenzhen 518172, China
[7]Tianjin University, Tianjin 300072, China
All the Authors contribute equally to this paper, names are listed in alphabetical order.

Abstract: For the non-stop demands for a better and smarter society, the number of electronic devices keeps increasing exponentially; and the computation power, communication data rate, smart sensing capability and intelligence are always not enough. Hardware supports software, while the integrated circuit (IC) is the core of hardware. In this long review paper, we summarize and discuss recent trending IC design directions and challenges, and try to give the readers big/cool pictures on each selected small/hot topics. We divide the trends into the following six categories, namely, 1) machine learning and artificial intelligence (AI) chips, 2) communication ICs, 3) data converters, 4) power converters, 5) imagers and range sensors, 6) emerging directions. Hope you find this paper useful for your future research and works.

Key words: integrated circuit design; artificial intelligence (AI); radio frequency (RF) circuits; data converters; power management; imager; sensor; cryogenic; biomedical

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1. Background

With the emerging applications of artificial intelligence (AI), big data, blockchain, internet-of-things (IoT), autonomous driving, drones/robots, metaverse, etc., and also due to the CoVid-19 pandemic makes people working from home and pushes the companies to setup a blended work model with distributed workforce, the demand for integrated circuits (IC) chips sees an explosive growth in recent two years. Needless to say, a tremendous amount of new circuit design challenges appears along with these new applications. Cutting-edge technologies and circuit innovations are the enablers for satisfying the ever-increasing circuit performance specifications, in terms of data rate, precision, resolution, perception capability, intelligence level, and energy efficiency.

China (the Far-East of the world), as the largest consumer of IC chips in the world, strategically focuses on not only the network infrastructures and the terminal equipment, but also the core hardware component — the chip. Driven by the new waves of technology, both the IC design industry and academia in China are catching up. In particular, it seems that the academia goes a little bit faster, as we can find from the data of the number of published papers on the IEEE International Solid-State Circuits Conference (ISSCC) and the Journal of Solid-State Circuits (JSSC), which are the topmost conference and journal in the field of IC design, respectively. Here in this review paper, we invite the active authors from China to provide their humble opinions on the recent trending IC design directions in 2022.

The following contents are categorized into six sections. Section 2 on machine learning and AI chips introduces AI chips for domain-specific applications, and emerging compute-in-memory circuits. Section 3 on communications IC discusses wireless/wireline transceivers, power amplifiers (PAs), clock generators and frequency synthesizers. Section 4 on analog-to-digital (ADC) data converters covers recent promising hybrid ADC architectures, and high-resolution ADCs. Section 5 on integrated power converters focuses on the topology and controller design of switched-inductor-capacitor hybrid power converters, isolated power, and the supply modulator

Correspondence to: Y Lu, yanlu@um.edu.mo
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for PA in 5G communication. Section 6 on CMOS imagers and range sensors talks about event-based and high dynamic range image sensors, as well as the time-of-flight (ToF) range sensors. Last but not least, Section 7 on emerging directions leads us to the cryogenic CMOS for qubit and biomedical frontiers. Finally, we draw conclusions in Section 8.

2. Machine learning and artificial intelligence chips

When people nowadays are working towards to metaverse or the “Matrix”, the first trending direction has to be AI chips. Besides the conventional general AI computer systems, custom processors are becoming more ubiquitous in the machine learning space, motivating the chip design for domain-specific applications, which include voice, image, and some other emerging directions. Meanwhile, computing-in-memory chips, at both the macro-level and system-level, have become an important technical approach for energy-efficient or high-performance AI chips.

2.1. AI chips for domain-specific applications

Custom processors are becoming more ubiquitous in the machine learning (ML) space, motivating the chip design for domain-specific applications (DSA). Through the methodology of hardware-software co-optimization, the DSA chips can bring a great leap of performance for target applications. Reviewing the ISSCC publications in recent three years, AI chips for DSA have drawn extensive attention for various applications, including voice, image, and some other emerging directions.

2.1.1. AI chips for voice applications

For voice applications, keyword spotting (KWS) and automatic speech recognition (ASR) can be widely applied to various wearable or mobile devices. For such battery-powered applications, ultra-low power is a strong requirement for voice processing chips. Typically, a KWS or ASR system is composed by the feature extractor and the AI signal processing, and recent works aims at optimizing the power of such two modules in circuit and system level.

Shan[1] implements a sub-μW KWS chip in ISSCC’20, aiming for 1–2 keywords spotting. To extract the voice feature of mel frequency cepstrum coefficient (MFCC), they designed a specific serial-pipeline fast fourier transformation (FFT) circuit with compressed on-chip memory. In AI processing, the depthwise-separable CNN is adopted with binarized activations, which reduces the storage and computation by 7× compared with normal CNN model. Different from traditional method to use the whole word for KWS, they eliminate the redundant computations and data storage coming from similar adjacent inputs. As a result, the chip achieves 94.6% accuracy for two-word spotting with only 0.51 μW power and 2 KB on-chip memory.

Although the chip in Ref. [1] achieves ultra-low-power (ULP) consumption, it adopts the noise-dependent training so the accuracy will degrade in low signal-to-noise (SNR) level. To achieve high robustness KWS, one method is to include all the possible SNR levels and noise types in the AI model training, which causes the increasing of model size and is challenging for ultra-low-power applications. To overcome the noise problem in KWS, Wang[2] employed a simpler voice extracting method called divisive energy normalization (DN), and developed a normalized acoustic feature extractor chip (NAFE) for analog signal processing. The frontend of NAFE is composed by a low-noise amplifier (LNA), a bandpass filter (BFP), a half-wave rectifier (HWR) and an integrate-and-fire (IAF) encoder, and extract the pre-normalized features (preNF). Then, the DN model is performed in preNF to estimate the background noise level by converting background noise to white noise, and produces post-normalized features (postNF). In AI signal processing, they use a well-developed spiking neural network (SNN) classifier chip and combine it with NAFE to realize an end-to-end KWS. The overall KWS system is robust for noisy condition and achieves an average accuracy of 92.8% in different SNR level.

Different from KWS that only needs to implement small-vocabulary tasks (1–2 words), ASR has to deal with large-vocabular tasks of more than 10^5 words. As a result, models with bidirectional recurrent neural network (RNN) and attention mechanism are necessary for improving the ASR accuracy. To accelerating ASR, Tambe[3] presents a 16-nm SoC that executes a full speech-enhancing pipeline in ISSCC’21. The chip is composed by a markov source separation engine (MSSE), for feature extracting, an Arm Cortex-A53 CPU for signal pre-processing, and a reconfigurable accelerator (FlexASR) for AI processing. In feature extractor, the MSSE uses bayesian algorithm and can make a binary label to distinguish noise and speech, which realize unsupervised speech denoising. Then the FlexASR, which comprises 4 processing elements and a multi-function global buffer, works to accelerate the bidirectional attention-based speech-to-text model. It supports most of the operations in seq2seq models, such as attention mechanism, mean/max pooling, and normalization. For attention computing, FlexASR is optimized to gate and skip computations in null states. The chip can achieve 2.25 mJ of energy per frame with real-time 18 ms latency, and is the first to demonstrate on-chip support for denoised, large-vocabulary ASR for bidirectional attention-based speech recognition.

To further reduce the power for IoT platforms, the technology of voice activity detection (VAD) that can gain attention on events-of-interest and is becoming an interesting topic. In such system, the always-on acoustic wakeup detector dominates the overall power consumption since the remainder of the VAD system is power-gated during sleeping time. As a result, an ultra-low-power and wide bandwidth feature extractor with wakeup detection is more important for VAD. Although achieves μW-level power, traditional analog-domain feature extraction-based VADs often adopt a simple decision tree or a fixed neural network for detection, and can only be applied to limited acoustic event targets. In ISSCC’19, Cho[4] adopts the time-interleaved mixer-based architecture to present a neural network NN-based acoustic sensing system for both VAD and non-voice event detection. In analog frontend, it has two signal chains: a 142 nW ULP chain which is always on for wakeup detection, and an 18 μW high performance (HP) chain which is used when system is waked up. For the ULP chain, the time-interleaved mixer-based architecture sequentially scans and down-converts the 4 kHz bandwidth signal to less than 500 Hz passband, which reduce the power consumption of amplifier, ADC and DSP by 4 times. In the digital backend, the power optimization of leakage power is important for the always on circuits. In their chip, thick oxide I/O devices are used to implement the always-on modules to sup-

press the static leakage power. The NN processor adopts a 16 kB custom ultra-low leakage static random-access memory (SRAM) to store the 4-bit weight. In the ULP mode, the processor runs with a small NN every 512 ms when the feature extraction is complete, and at other times it is power-gated to minimize the leakage power. In the HP mode, the processor computes a FFT and a larger NN for improved 32 ms latency. The chip is also integrated with a MEMS microphone and achieves 91.5%/90% speech/non-speech hit rates at 10 dB SNR with babble noise in the ULP mode. Although the work in Ref. [4] achieved an ultra-low power for the feature extractor, the 512-ms decision latency prevents it from real-time VAD applications.

To realize real-time wakeup decision, Chen[5] adopts the time-domain CNN (TD-CNN) for analog feature extracting in ISSCC'22. Different from previous analog filter-based frontend, the TD-CNN evaluates the signal from LNA buffers by 1-D convolution layer in a temporal manner. As a part of the AI models, the TD-CNN can be trained with the entire network, which permits reprogramming to adapt for various applications with different characteristics. The TD-CNN is realized by an analog circuit with a switched-capacitor (SC) array and adopts a 3-bit sparsified quantization scheme, which shows an accuracy higher than 7-bit binary quantization. After the TD-CNN pre-processing, the extracted features can be concatenated into a 2-D feature map and be further processed for more complex tasks. Compared with Ref. [4], it achieves 50 times higher framerate with similar power budget.

2.1.2. AI chips for image or video processing

For image or video processing, people paid more attentions to improve the energy and frame efficiency for executing the AI models, with the co-optimization technology of algorithm and architecture, low-bit model quantization and sparse model acceleration.

Lu[6] proposes a low-power and real-time vision-based hand-gesture recognition (HGR) system in ISSCC'21. The overall architecture is mainly composed by a pre-processing unit, a recognition core and a sequence analyzer (SA). First, the pre-processing unit helps to segment the hand region from color image. Second, a motion detection unit, a hand localization unit, and a feature extraction unit in the recognition core work together to generate the input feature data for two customized classifiers: the edge-CNN core (ECCNC) and the decision tree core (DTC). Finally, the SA integrates the decision of ECNNC and DTC to improve the accuracy and robustness of HGR system. To optimize the computing efficiency, this work explores the data reuse space of ECCNC. The 2-layer edge-CNN model shows a 32× space of weight reusing for the first layer and a 6× space of feature reuse for both layers. To maximize the data reusing, ECCNC employs the shared-link connection between multiple PEs so that the feature and weight data can be reused by different PEs. Such flexible data scheduling reduces 27% memory access. Besides the ECCNC, the DTC works to improve the system's error tolerance. The SA analyzes the results from ECCNC and DTC to judge the specific gesture type, and helps the system to achieve 92.6% accuracy and 30-fps real-time recognition with only 184-μW power consumption.

Im[7] aims at accelerating the depth image processing for 3D bounding box extraction, and propose the depth signal processing unit (DSPU) in ISSCC'22. The overall flow for 3D extraction includes many modules, such as depth CNN, neighbor search, point sampling (UDS), point grouping (BQ), and point CNN. To reduce the area overhead, DSPU develop a unified matrix-processing unit (UMPU) and a unified point-processing unit (UPPU), where all matrix computations are shared in the UMPU and all point operations are shared in the UUPU. Since the point NN has high sparse input features, the DSPU adopts slice-level-skipping PE for zero input skip. To reduce the redundant computation caused by the max polling layer, the largest values are predicted by 4-b MSB convolution of inputs and weights to skip the non-maximal outputs. By the optimization of sparse acceleration, the total latency of PNN can be reduced by 44.5%. As a result, the DSPU finally achieves 31.9-fps with 281.6-mW to realize end-to-end RGB-D acquisition and 3D BB extraction.

Compared with image data, video has one more dimension of time and provides more design space in algorithm and hardware. Since adjacent frames share similar information, efficiently leverage video temporal correlations to minimize the computing costs for video model is worth exploring. In ISSCC'20, Yuan[8] proposes an inter-frame data-reuse processors for video accelerating. Other than directly inputting the original frames, the work processes the difference feature between two frames in each CNN layer to reduce the redundant computation. The work finds that although typical frames in a period of time are similar, it does not mean they are identical and the diff-feature has limited sparsity. In order to process diff-feature without accuracy loss while improving the computing efficiency, the chip adopts a hybrid-precision inter-frame data-reuse scheme. In hybrid precision coding, low precision 4-b tensor is adopted for relatively small values in the feature map, while 8-b sparse tensor is adopted for the others. The two tensors have separate storages with multiple-type sparse coding methods. With inter-frame data reuse, the off-chip data transmission is significantly reduced by 15%–30% for different datasets. Finally, the 65-nm chip can reduce up to 76.3% power to achieve a 24.7-μJ per frame energy efficiency.

For emerging AI models, transformers have achieved great success in multiple AI fields, from natural language processing (NLP) to computer vision. Compared with CNN models, transformer calls for larger memory storage and different data reusing mechanism. To develop specific architecture for transformer accelerating, two relative chips are presented in ISSCC'22. Wang[9] presents a digital transformer processor to achieve 27.5 TOPS/W energy efficiency by asymptotic sparsity speculating. This work find that the transformer model contains many weakly related tokens with small scores caused by the attention operation. Such weak tokens can take up to 93.1% energy consumption in the whole system, but has limited influence on the model accuracy. Moreover, the softmax function results in many zero data, but the sparsity is irregular and hard to predict. To overcome such problems, the work adopts a big-exact-small-approximate (BESA) PE to gate the computation of LSBs for small values, which saves 1.62× MAC power. To skip the sparse computing, a bidirectional asymptotic speculation unit (BASU) is designed to explore the attention's local properties and exploit the presence of sparsity, which skips 46.7% of the redundant computations. The 28-nm chip uses 27.56 TOPS/W peak energy efficiency to implement the transformer model.

Table 1. Performance summary of AI chips for different DSA.

		ISSCC'20, 14.1, [1]	ISSCC'21, 9.9, [2]	ISSCC'21, 9.8, [3]
Speech (KWS/ASR)	Technology (nm)	28	90	16
	Model	DSCNN	DT	RNN
	Memory	2 KB	–	9.8 MB
	Latency (ms)	64	<100	15–45
	Power (μW)	0.51	6	1.11×10^5
	Word	1–2	1	2×10^5
	Denoising	No	Yes	Yes
		ISSCC'19, 17.2, [4]	ISSCC'22, 22.5, [5]	
Speech (VAD)	Technology (nm)	180	28	
	Feature type	Mixed-signal	TD-CNN	
	Channel number	16–48	60	
	Freq. range (Hz)	75–4000	100–4000	
	VAD power (nW)	142	108	
	VAD accuracy	90% @ nonspeech	94% @ nonspeech	
	Energy/Classification (nJ)	73	1.08	
		ISSCC'21, 9.7, [6]	ISSCC'22, 33.4, [7]	ISSCC'20, 14.2, [8]
Image/Video	Technology (nm)	65	65	65
	Model	Edge CNN (GTR)	Point CNN (3D detection)	MobileNet (Classification)
	Memory (KB)	–	364 KB	196 KB
	Power (mW)	0.184	544–609	7.3–99
	Frame efficiency	30 fps	3.2 mJ/Frame	24.7–183.2 μJ/Frame
		ISSCC'22, 29.2, [9]	ISSCC'22, 29.3, [10]	
Emerging directions	Technology (nm)	28	28	
	App.	Transformer	Transformer	
	Memory (KB)	336	192	
	Energy efficiency (TOPS/W)	1.91–27.56	5.1–20.5	
	Power (mW)	12–272	27–118	

Also in this year, Tu[10] proposes a transformer accelerator TranCIM, but based on computing-in-memory (CIM) architecture. Different from static model, the online generated weights and inputs of attention layers causes redundant off-chip memory access. TransCIM employs a CIM pipeline architecture combined with the bitline-transpose structure to align the directions of input and weight feeding, and allow intermediate data to stream from the first engine to the next. The CIM chip was fabricated in 28-nm CMOS and achieves a 20.5 TOPS/W energy efficiency for INT8 computing.

The DSA chips mentioned above mainly follow the road of algorithm-architecture co-optimization. Aiming at one specific applications, they analyze the demand and develop the high-efficiency analog or digital circuits. Inspired by 2.5D/3D stacked integrating technologies for high bandwidth memory fabrication, the road of monolithic 3D and hybrid bonding techniques are also explored for DSA chips. Eki[11] from Sony presents a stacked CMOS image sensor (CIS) with AI computing ability. The CIS block for sensor is integrated with a digital signal processor (DSP) for CNN computing together through 3D stacking in this work. The top CIS chip is fabricated in a 65-nm process while bottom DSP chip is using a 22-nm process, which shows an attractive solution for intelligent and low-cost vision sensor.

Niu[12] stacks a 25-nm dynamic random-access memory (DRAM) die on top of a 55-nm logic die and gives a near-memory-processing solution for the memory-bound recommendation system. The chip achieves a 307 bandwidth-to-capacity ratio and 0.88 pJ/b energy cost, which outperforms the prior processing-near-memory chips significantly because of the hybrid bonding scheme. It is foreseeable that more DSA chips using monolithic 3D and hybrid bonding technologies (sensor-logic stacking, memory-logic stacking, logic-logic stacking …) will be explored to increase the data transmission speed and efficiency.

Based on the reviews above, we can see that significant progresses have been made in machine learning processor design for specific application acceleration. Table 1 gathers the performances for DSA chips appeared in recent three years of ISSCC. One important trend of DSA processor is designing the computing and storage architectures to match with the specific application's characteristics. Algorithm-architecture co-optimization is adopted by researchers to explore the design space of low-bit quantization, sparse computation, dedicated circuit, and so on. The KWS chips used in wearable devices calls for low-memory hardware architecture and low-complexity AI models to reduce power. Moreover, the problem of background noise needs to be properly solved to improve the speech system's robustness. Thus, analog single processing circuit and unsupervised speech algorithms are under research for denoising. Image or video processing pays more attention to the frame efficiency, which calls for pipelined and sparse computing optimization. As an emerging direction, transformer processors process different model architectures, necessitating innovations in customized hardware design for the attention mechanism. Another trend is

Table 2. Summary of the SRAM-based CIM macros.

Ref.	CIM mode	Tech. (nm)	Macro size	Input precision (bit)	Weight precision (bit)	Output ratio	Performance (TOPS)	Energy efficiency (TOPS/W)	Area efficiency (TOPS/mm^2)	Inference accuracy (Cifar-10)
[13], 2020	Current based	28	64 Kb	4/8	4/8	1 : 1	–	68.44@4b/4b 16.63@8b/8b	–	92.02%
[14], 2020		65	16 Kb	2/4/6/8	4/8	1 : 12	2.0*@2b/4b	158.7*@2b/4b	3.38*@2b/4b	91.74%
[15], 2021		65	64 Kb	2/4/6/8	1–8	1 : 1	3.16*@2b/1b	370*@2b/1b	1.85*@2b/1b	92.65%
[22], 2021	Charge based	28	384 Kb	4/8	4/8	1 : 1	–	94.31@4b/4b	–	–
[23], 2021		16	4.5 Mb	1–8	1–8	1 : 4.5	11.8@4b/4b	121@4b/4b	2.67@4b/4b	91.51%
[16], 2021	All-digital	22	64 Kb	1–8	4/8/12/16	1 : 1	3.3@4b/4b	89*@4b/4b	16.3*@4b/4b	#
[17], 2022		28	32 Kb	1–8	1/4/8	1 : 1	–	27.38@8b/8b	–	#
[20], 2022		5	64 Kb	4	4	1 : 1	2.94@4b/4b	254*@4b/4b	221@4b/4b	#
[21], 2022		28	16 Kb	1	1	1 : 1	20@1b/1b	2219@1b/1b	606@1b/1b	86.9%
[18], 2022	Time based	28	1 Mb	4/8	4/8	1 : 1	4.96@4b/4b	148.1*@4b/4b 37.01*@8b/8b	–	92.08%

*: with sparsity improvement or at 10% input toggle rate. @4b/4b: 4bit input, 4bit weight. #: the same accuracy to the software baseline at the same precision.

monolithic 3D and hybrid bonding that stacks different kinds of chips in one system to offer significant bandwidth and power benefits.

2.2. Computing-in-memory chips

Computing-in-Memory (CIM) chips have become an important technical approach for energy-efficient or high-performance AI chips. The recent CIM chips mainly focus on two design levels: the macro-level and system-level CIM chips.

2.2.1. Macro-level CIM chips

The macro-level CIM chips aim at higher energy efficiency, higher density, better accuracy and higher performance. The current-based, charge-based, all-digital, and time-based CIM macro structures have been proposed. The key design concerns include low-power ADC, high-density CIM cell structure, high accuracy, more functionality, etc.

ADC design is critical for an energy-efficient CIM chip as it occupies the majority of the power consumption. Based on the algorithm analysis, the multiply-accumulate (MAC) values of the ADC input concentrate on low values. Therefore, one reference voltage can be adopted for pre-classification, which reduces the ADC sensing bit of low MAC values[13]. The sparsity technique is adopted to pre-train a whole weight block as zero, so that the corresponding ADC result can be determined as zero by the sparsity index[14], which saves the ADC sensing power for zero results. Furthermore, an ADC with flexible bit-precision is designed, where the 2-bit index can dynamically select the 0-/2-/4-bit ADC sensing modes[15]. In the all-digital CIM structure that does not need the ADCs, the majority of the power consumption comes from the digital adder tree. The interleaved 14T/28T full adder can increase the energy efficiency by 30%[16]. Dynamic logic is also explored for better energy efficiency, which shows no leakage and hazard problems[17]. The evolving time-based CIM structure replaces ADC with time-to-digital converter (TDC)[18, 19]. By eliminating ADC and adopting the dynamic differential-reference TDC, the time-based CIM structure shows 37.1× and 6.18× higher energy efficiency than the current-based and charge-based CIM structure[18]. Besides, the time-space readout can be executed simultaneously to the analog MAC developing operation, which avoids long computing latency due to heavy resistance and capacitance (RC) parameters[19].

Storage density and computation density are also key features for the CIM macro. For higher computation density, several storage cells are grouped together to share the same local-computing-cell for CIM operation[13]. The all-digital CIM structure shows better scaling improvement for higher storage/computation density, which achieves 221 TOPS/mm^2 area efficiency at 5-nm technology node[20]. Approximate circuits for all-digital CIM structure can reduce the transistor quantity. The double approximate compressor shows 56.4% transistor reduction with 2569 F2/b area efficiency[21].

Accuracy is an important concern for CIM macro design. For better accuracy, the output ratio, which is the ratio of the real output resolution and the ideal output resolution, is a key parameter for current/charge-based CIM structures[22]. A higher output ratio improves the accuracy, while requiring higher power consumption. Compared with the current/charge-based CIM structures that are sensitive to process, voltage, and temperature variations, the all-digital CIM structure shows no analog accuracy loss[16, 20]. The charge-based CIM structure shows reasonable accuracy with high parallelism, which can activate 1152 input rows simultaneously[23]. The evolving time-based CIM structure presents better accuracy and lower power consumption[18, 19]. In each delay computing unit, the MAC operation result is converted to the accumulated time delay between the input and output signals[18], which achieves 8× higher normalized signal margin than the previous voltage-domain ADC based CIM structure.

More functionality is also explored on the CIM macro structures. Several works have explored configurable activation/weight bit-precision, among which the 2's/non-2's com plementary ADC is designed to support signed/unsigned MAC operations[14]. To support both inference and training applications, a two-way transpose CIM macro is proposed, which can utilize two directions of CIM operation without weight data transpose operation[24]. Table 2 summarizes the key features of the state-of-the-art SRAM-based CIM macros.

2.2.2. System-level CIM chips

On the other hand, the system-level CIM chips present more sophisticated CIM architecture with more flexible operator support.

Inter/intra-macro data reuse and channel/kernel-order weight mapping strategies are explored on the CIM architec-

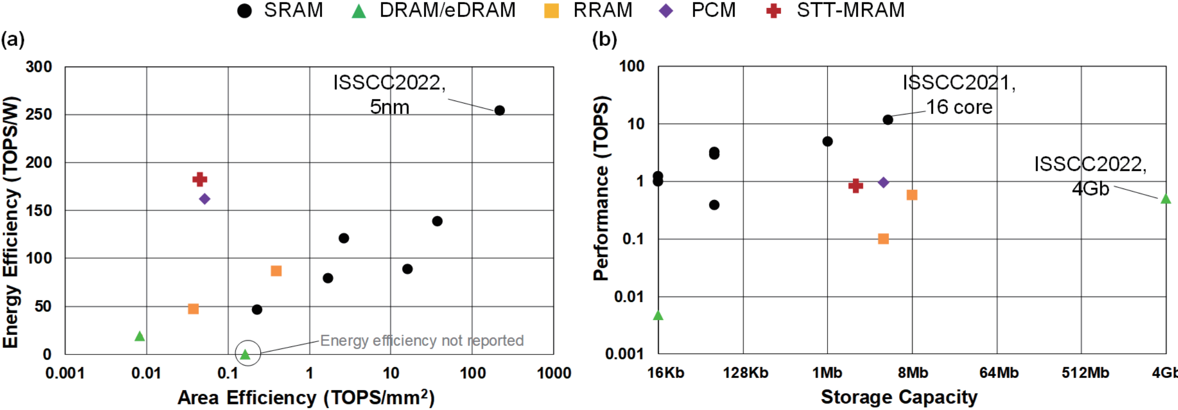


Fig. 1. (Color online) Comparison of the state-of-the-art CIM macros (scaled to 4-bit input, 4-bit weight), with (a) energy efficiency and area efficiency, and (b) performance and storage capacity.

tures for better resource utilization[14]. Multi-core CIM systems are designed to extend the CIM performance and functionality. A 16-core CIM system with programmable single instruction multiple data (SIMD) data path and flexible on-chip network shows 96% bit-cell utilization on Cifar-10 dataset[23]. To utilize both digital and CIM architecture for optimal performance on the various layer characteristics, a low-power SoC, comprising a digital neural network accelerator, an analog CIM core and a RISC-V CPU, is designed to realize simultaneous execution of subsequent layers and high/low precision on corresponding cores[25].

Algorithm-hardware co-design method is utilized for higher energy efficiency. For example, the block-wise weight sparsity and dynamic activation sparsity is proposed to apply sparsity techniques on the regular CIM structure[14]. The set-associate block-wise sparsity, tensor-train compression and bit-wise sparsity are also explored to save execution time or power consumption[15, 26].

To support high-precision training application, a reconfigurable unified floating point or integer (FP/INT) CIM processor is proposed[27]. The activation/weight data are pre-aligned to the local maximum point so that the CIM macro can execution floating-point MAC operation as the same flow of integral MAC operation.

2.2.3. Various devices based CIM chips

SRAM is one of the most popular devices for CIM chip design, while other devices for CIM are also explored, including conventional storage devices such as DRAM or embedded DRAM (eDRAM), and the emerging non-volatile memory (NVM) devices such as resistive RAM (RRAM), spin-transfer torque magneto-resistive RAM (STT-MRAM), phase-change memory (PCM), etc.

DRAM/eDRAM device is adopted for CIM for its high storage density. Xie[28] proposes a 16-Kbit eDRAM-based CIM chip, utilizing the intrinsic charge share operation in eDRAM bitcell to implement the DAC/MAC/ADC circuits. A 4-Gb GDDR6-based CIM accelerator is implemented to support various MAC and activation functions[29]. The fabricated DRAM die has 16 processing units with corresponding storage banks, and a two 2-KByte global buffer. It supports to activate 16/4 banks simultaneously for different parallelism, with flexible dataflow controlled by the newly defined DRAM command set for deep learning operations. It achieves 1 TFLOPS performance (two die per chip) under BF16 precision.

A three-transistor, one-capacitor (3T1C) dynamic analog RAM (DARAM) structure is proposed[30], which features higher density than SRAM, while achieves higher computing parallelism than DRAM. By storing 4-bit weight in one 3T1C cell, it shows 10× less transistor counts compared with the SRAM-based CIM cell.

RRAM is another well-explored device with macro-level and system-level chip verification. From 2020 to 2022, the foremost storage capacity of RRAM-based CIM macro increases from 2, 4, to 8 Mbit[31, 32, 19]. The RRAM-based CIM macros usually adopt current-domain ADCs due to the limited CIM operation voltage[31]. The 2’s complement weight mapping is explored to reduce the cell usage for multi-bit weight data. To meet the accuracy and energy efficiency requirement, the asymmetric group modulated input and hybrid precision readout circuits are proposed, which separates an 8-bit input data into high 2 bit, middle 3 bit and low 3 bit, and adopts full-precision/reduced-precision for the most/least significant bits[32]. The time-based CIM structure is adopted in RRAM-based CIM macro, which shows 5.15× average energy reduction, 1.36× latency reduction, and 1.58× time-step sensing margin[19]. The average energy efficiency for 8-bit MAC operation achieves 21.6 TOPS/W. A system-level CIM chip[33] is implemented with two fully-connected layers for the MNIST dataset, which shows 78.4 TOPS/W energy efficiency and 94.4% accuracy. The proposed 2T2R array generates the differential current of the positive and negative RRAM cells, which reduces the accumulated source line current, relieve the IR drop, and decreases corresponding ADC power.

Spin-transfer torque magneto-resistive RAM (STT-MRAM)[34] and phase-change memory (PCM)[35] based CIM macros have also been explored. A 4-Mbit STT-MRAM computing-near-memory macro is fabricated[34], which utilizes a high bit-width of 576 bit organized in bitwise weight-mapping order for near memory partial MAC operation. It also adopts a bidirectional bitline access readout scheme supporting high-to-low and low-to-high voltage sensing, which reduces precharge latency and power consumption. A 25.1 TOPS/W energy efficiency is achieved at 50% input sparsity and 8-bit MAC precision. The PCM device is another resistive memory device that can be configured as 1-bit single-level cell (SLC) or multi-level cell (MLC). A PCM macro with 2-M cells is fabric-

ated. It adopts a hybrid SLC-MLC structure, utilizing five SLC/MLC cell for each part of the [7]/[6]/[5:4]/[3:2]/[1:0] bit of a 8-bit weight data. The hybrid SLC-MLC structure shows slight accuracy loss compared with the pure SLC implementation.

Fig. 1 presents the energy efficiency and area efficiency comparison of the CIM macros with different devices. The energy/area efficiency value are scaled to 4-bit input, 4-bit weight. The SRAM-based CIM macros shows better energy efficiency, area efficiency, and higher performance due to several factors. The first influence factor is the more advanced technology node, such as the 5 nm SRAM CIM chip[20]. The second factor is that the SRAM-based CIM macros focus on high computation/storage ratio (i.e. higher computation parallelism), which benefits the area efficiency and the performance. On the other hand, the emerging NVM devices and DRAM shows higher storage capacity thanks to the higher storage density. Note that the technology and sparsity influences are not scaled since these features are difficult to scale to an accurate value. The area of RRAM/STT-MRAM/PCM-based macros is estimated from the effective area of the test chip photograph. The area efficiency of DRAM only considers the area of processing units since the total area with storage cells is not reported.

In summary, the CIM chip has become an emerging technology route for more energy-efficient computing and high-performance AI applications, which shows competitive or higher energy efficiency compared with the digital NN processor. The macro/system-level CIM chip keeps moving towards better macro metrics (power, area, performance, accuracy, functionality) and sophisticated CIM architecture with more operator support. CIM on various devices and specific applications is also a promising direction.

3. Communication ICs

Telecommunication industry has been growing explosively over the past few decades. Communication ICs, ranging from block-level circuits to system-level transceivers, have attracted intensive attention from both academia and industry. This section covers the latest research trends of communication ICs during the past few years, which includes the following sub-topics: 1) wireless transceivers, 2) wireline and optical communication circuits, 3) phase-locked loops, 4) critical building blocks including power amplifiers, voltage-controlled oscillators, and crystal oscillators.

3.1. Wireless transceiver ICs

Wireless transceivers are central components of wireless systems. For mobile communication applications, the continuous demand for faster wireless data in the context of mobile battery limitations drives the development of high-throughput and energy-efficient wireless transceivers in more carrier aggregation and wider bandwidth per path, as shown in Fig. 2. Due to growing demand for faster data rate in wireless systems, better resolution requirement in radar system, and emerging sensing applications, mm-wave transceivers for radar and communication have become very attractive in recent years. Ultra-low-power radios are the main building blocks of internet-of-everything connectivity. Bluetooth low-energy (BLE) radios are extensively used for wireless connectivity in many small portable devices, where longer battery life

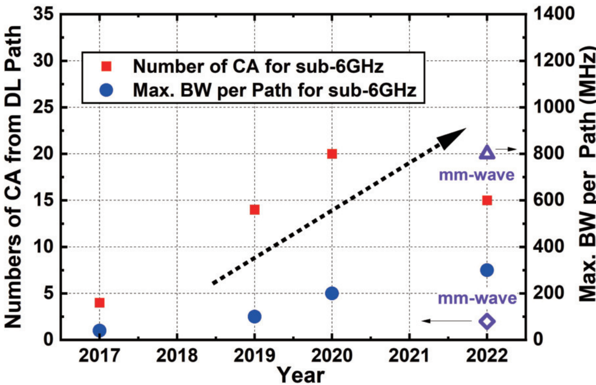


Fig. 2. (Color online) Trends of the number of CA from downlink path and maximum BW per path for recent cellular SoC implementations.

dramatically improves user experience. In this section, we will discuss, in the following, the state-of-the-arts of high data rate wireless transceivers with multiple mobile communication standards, millimeter-wave and radar transceivers, as well as ultra-low-power radios.

5G radio technology promises tens of Gb/s data-rates with a 10× reduction of latency. This will enable applications in enhanced mobile broadband, massive internet of things and mission-critical services. In Ref. [36], MediaTek introduces a 2/3/4/5G compliant transceiver in 12-nm FinFET CMOS supporting 6-carrier aggregation downlink, 2-carrier aggregation uplink, and 4 × 4 MIMO 256-QAM for the first demonstration of 2 × 2 coherent up-link MIMO. Samsung Electronics demonstrates a highly integrated lost-cost, low-power transceiver IC supporting legacy 2G/3G/4G and new-radio frequency range 1 (FR1) communications with dual-mode global navigation satellite system (GNSS)[37]. In this year, Samsung Electronics introduces a digital-IF sub-6GHz FR1 cellular receiver supports up to 15 inter/intra CA by 3 downlink paths with the capability of achieving 300 MHz bandwidth per path in 14-nm FinFET CMOS[38].

Millimeter-wave (mm-wave) wireless communication and radar transceiver systems are the key drivers for cutting-edge integrated circuits design advancement. Mm-wave antenna arrays allow fine beam steering with large radiated power and compact size. Scalability of large-scale arrays to hundreds of elements is necessary to extend the range of mm-wave for 5G and the next-generation radio systems. In Ref. [39], Broadcom presents a 144-element phased-array transceiver using a tiled approach for IEEE 802.11ad. It reports the measured an effective isotropic radiated power (EIRP) of 51 dBm and supports scan angle of ± 60° in azimuth and ± 10° in elevation. Samsung demonstrates a 16-channel, 28/39 GHz dual polarized 5G phased-array transceiver IC with a quad-stream IF transceiver supporting non-contiguous carrier aggregation up to 1.6 GHz bandwidth (BW)[40]. Transitions from phased-arrays to digital beamforming/MIMO arrays allow increased FDD/TDD/Massive MIMO functionality. Researchers from the University of California Berkeley[41] present a 16-element by 16-beam multi-user beamforming integrated receiver with baseband analog BF matrix and on-chip LO generation in 28-nm CMOS technology, which supports up to 2 Gb/s/user wireless links and handles 16 concurrent user streams over the whole band. CMOS radar technologies continue to advance with demonstration of mm-wave MIMO radar, which

leads to improved 3D resolution and object discrimination for automotive radar. The work in Ref. [42] demonstrates a 77/79 GHz MIMO radar SoC with 12 transmitters and 8 × 2 receivers resulting in 192 virtual receivers. The radar system based on the IC achieves 6 cm range resolution, 1° angular resolution, and 0.099 km/h Doppler resolution. In addition, two high-level integration 76–81 GHz FMCW MIMO radar module are demonstrated in Refs. [43, 44]. With the continuing advancements of terahertz (THz) technologies in silicon processes, more and more THz transceivers are demonstrated for spectrum-to-space mapping, wideband communication, high resolution mapping[45, 46].

Advances in the ultra-low-power radio continue the drive towards power-efficiency and high sensitivity wireless nodes. In Ref. [47], researchers from Columbia University describe a wake-up receiver achieving a –78.3/–79.1dBm sensitivity at 151.25/434.4 MHz with a 110 ms latency, while consuming 370/420 pW from 0.4 V. It enables practically unlimited battery lifetime for sensor nodes. UWB radio technology promises high data rate and precise positioning over a small distance, which can be useful in many consumer electronic and brain-computer interface applications. Researchers from Yonsei University introduces an IR-UWB radio[48] with 1.25 Gb/s data rate over 2 m range while only consuming 28 mW, which is the best among state-of-the-art for energy efficiency at 2 m range up until now.

3.2. Wireline and optical communication circuits

With the development of cloud services and mobile computing, the datacenter drives an ever-growing demand for the high-speed and low power interconnects. In the past three years, the wireline I/Os have witnessed a doubled per-channel data-rate, scaling from 112 to 224 Gb/s. The four-level pulse amplitude modulation (PAM-4) has been employed as an enabling technique. To keep the power consumption acceptable, some of the most advanced processes have been utilized, scaling from 7-nm to 5-nm FinFET technology. A universal figure-of-merit factor, pico-Joule-per-bit (pJ/bit), has been widely adopted to evaluate the power efficiency. The trends of wireline communication circuits is briefly summarized in Fig. 3.

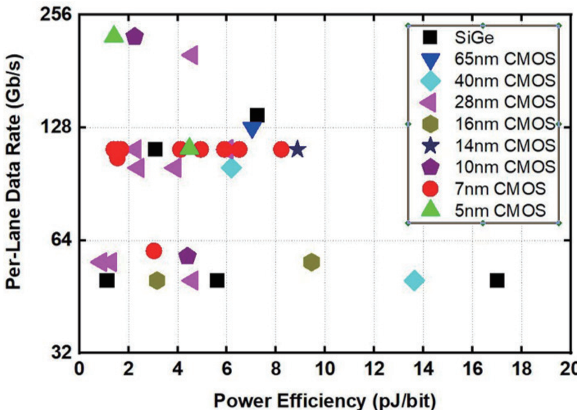


Fig. 3. (Color online) Trends of wireline communication circuits: power efficiency and data rate.

Categorized by the communication distance, wireline transceivers employ different wiring channels (copper or fiber) and circuity topologies. In the past three years, the long-reach (LR) and extra short reach (XSR) serializer/deserializer (SerDes), as well as the co-packaged optics (CPO) have attracted the most research attentions worldwide.

3.2.1. LR and XSR SerDes

The LR Serdes attempts to overcome up to 40-dB channel loss and beyond 112 Gb/s channel speed. State-of-the-art LR receivers have largely converged on an architecture based on time-interleaved SAR ADCs (RX) and multi-bit equalizer embedded DACs (TX). There are two fundamental design challenges need to be addressed in the SerDes transceivers. Firstly, the data path analog bandwidth keeps increasing, while maintaining about 1-Vpp output swing and sufficient linearity for the PAM-4 signaling. Inverter-based analog front-end circuits are widely adopted to accommodate the advanced CMOS technology[49–51]. Hybrid continuous-time linear equalizer (CTLE) architecture with inductive peaking and source degeneration can be used to extend the circuit inherent BW[52]. To improve the TX bandwidth, current mode logic (CML) DAC-based output stage with active inductor peaking pushes the data rate to 112 Gb/s PAM-4. High-order T-coil and π-coil network with precise electromagnetic (EM) modeling can be employed to address the parasitic capacitance from ESD and I/O PADs[53]. Secondly, the SerDes transceiver requires high-frequency clock with precise phase spacing and low jitter to serialize and re-time the symbols up to 112 GBaud. Quarter rate serializer architecture has been widely adopted[49, 54, 55], in which the pulse-based MUX and quadrature clock phase calibration are of great importance[53].

High-performance XSR SerDes with both high area efficiency (mm^2/lane) and energy efficiency (pJ/b) are driven by the interconnects in datacenter, XPU and AI applications. It enables chiplets, multi-die integration for low cost, high yield, and high throughput. The XSR SerDes employs simplified TX DAC and RX DSP functions to save power and area. In Ref. [56], 5-tap TX FIR equalization and a delay-line based continuous-time RX linear equalizer are adopted, realizing 50% power saving and 12% speed improving. Baud-rate PAM-4 CDR instead of multi-bit ADC is utilized to recover the 112 Gb/s data over up to 12 dB loss in an XSR channel. The optimized power efficiency achieves less than 1.5 pJ/bit in a 7-nm process[56].

3.2.2. Optical links and silicon photonics

The datacenter switch throughput has been growing from 12.8 to 25.6 Tb/s. To support inter- and intra-rack interconnects, the optical links are expected to achieve longer reach (<500 m) at higher data rate (>400 Gb/s). Silicon photonics (Si-Ph) solutions are of particular interest to achieve high-density integrated 100+ Gb/s/λ optical transceivers, which would be deployed in the CPO modules[57, 58]. On the TX side, Si-Ph mirroring modulators (MRMs) have the unique feature of high-*Q* resonant filtering that can be utilized for the on-chip wavelength-division multiplexing (WDM) links. To stabilize the resonance wavelength, a hybrid electrical-optical control loop is necessary to be integrated, while an automatic tuning algorithm is also preferred. In Ref. [57], a 28-nm CMOS driver is co-designed and flipped-chip mounted onto the Si-Ph MRM. The optical TX achieves 4 × 112 Gb/s data-rate and 7.5 pJ/bit power efficiency. The integrated temperature control realizes sub-GHz wavelength tuning resolution at temperatures up to 55 °C. On the RX side, original SiGe transimpedance amplifiers (TIA) are expected to be replaced by CMOS

ones for higher integration and lower power. To achieve a comparable sensitivity, digital intensive feedforward equalization (FFE) and decision feedback equalization (DFE) circuits are integrated in the TIA to compensate for the insufficient TIA BW without contributing additional noise[59]. Besides of the intensity modulation direct-decision (IMDD) solution, coherent optical transceivers would have longer reach (>2 km) and higher data rate (>640 Gb/s). The first challenge is to design a high-swing and high-linearity modulator driver in CMOS. In Ref. [60], the distributed multi-peaking using on-chip coils and T-lines could significantly extend the analog BW. In addition, the stacked current re-use topology can be adopted to save power in a high-swing driver with sufficient voltage headroom.

In conclusion, after three years of continuous research, the 112 Gb/s/lane wireline circuits have become mature. To save power and further double the speed, more advanced 5-nm CMOS process starts to be adopted as a mainstream technology, enabling the exploring for 224 Gb/s/channel. The full link (TX+RX) power efficiency of 112G LR SerDes has reached 2.2 pJ/bit, while the 224G is still beyond 3 pJ/bit. Optical links would be utilized to replace the copper-wire for meter-scale connectivity and beyond. By co-packaging electronics and silicon photonics, chip-scale high-BW and high-density throughput would be feasible in the future.

3.3. Low-jitter PLL

Phase-locked loops (PLL) are widely used in modern ultra-high speed wireless/wireline communication circuits and systems, such as 5G transceivers, over-100-Gbps SerDes transceivers, and high sampling rate analog-to-digital converters (ADCs). Fig. 4 summarizes the recently published representative low-jitter PLLs from recent years' ISSCC or JSSC papers. Based on the recently published works shown in Fig. 4, we will give an overview of the PLL development trends, including the trends of PLL architectures, and the performance gap between integer-N PLL and fractional-N PLL.

Among the PLLs shown in Fig. 4, five PLL architectures are widely used, including charge-pump based PLL (CPPLL)[61–63], sampling/sub-sampling PLL (SPLL/SSPLL)[64–71], time-to-digital converter (TDC) based digital PLL (TDC-based DPLL)[72, 73], and digital sampling/sub-sampling PLL (D-SPLL/D-SSPLL)[74–76], injection-locked PLL (ILPLL)[77], and injection-locked clock multiplier (ILCM)[78, 79].

The CPPLL, which adopts a phase/frequency detector (PFD) with unlimited phase and frequency detection range, is simple and robust[80]. Thus, it is widely used especially in industry. However, the low PFD gain, which is only $1/2\pi$, makes the in-band phase noise of CPPLL (mainly contributed by the CP) difficult to be suppressed[80]. Fig. 5 illustrates a simplified linear phase noise model of the PLL with noise transfer function of the PD. It indicates that a low-noise CP with a large CP current is required for the CPPLL to achieve low in-band phase noise and low-jitter performance due to the low gain of PFD. This makes the CPPLL not a suitable choice for low-jitter low-power PLL design. The jitter figure-of-merit $\text{FoM}_{\text{jitter}}$ (the lower the better) of CPPLL, can be improved by newly proposed techniques including the reference frequency multiplier[62] and time-amplifying phase detector (PD)[63]. However, the $\text{FoM}_{\text{jitter}}$ improvement of the CPPLL is still less than that of the other PLL architectures.

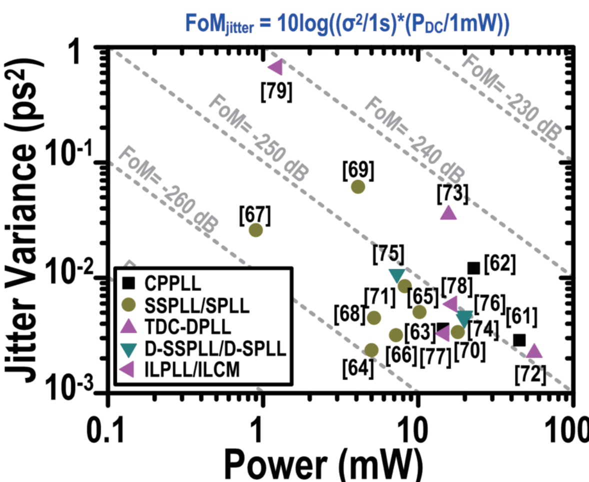


Fig. 4. (Color online) The jitter variance versus power of the recently published PLLs from ISSCC/JSSC.

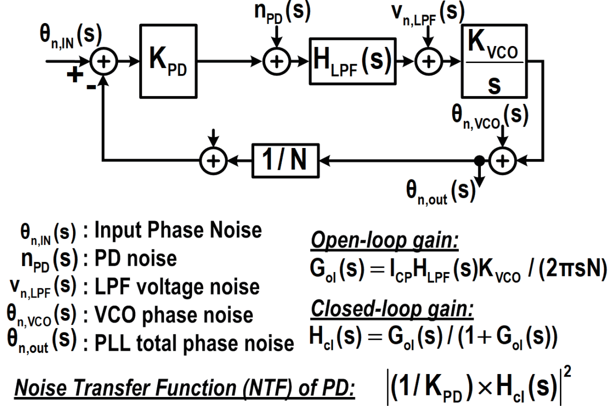


Fig. 5. Simplified PLL linear phase noise model with its noise transfer function of the PD.

As discussed before, it is significant to increase the PD gain so as to suppress the in-band phase noise to achieve low-jitter with low power consumption. The SSPLLs[64–69] adopt a sub-sampling PD (SSPD) to sample the voltage-controlled oscillator (VCO) output signal for phase detection purpose, and thus can achieve high PD gain as the SSPD gain equals the slope of the VCO output signal. Similar to the sub-sampling PD, the sampling PD (SPD) in SPLL[70, 71] achieves similar high PD gain by sampling the sharp edge of the divider output signal for phase detection. In addition, the SPD achieves much higher phase detection range than the SSPD. Thanks to the high PD gain, the SSPLL reported in Ref. [64] achieves the best $\text{FoM}_{\text{jitter}}$ of –259.2 dB with integrated jitter below 50 fs; and several other SSPLLs/SPLLs[66–68] obtain $\text{FoM}_{\text{jitter}}$ below –255 dB, which are obviously better than that of other PLL architectures.

Digital PLL is getting more popular due to its scalability in advanced CMOS technology and the design portability between technologies. TDC-based PLL[72, 73] is a commonly used DPLL architecture. For low-jitter design, a high TDC resolution is required for high PD gain purpose. Recently, Ref. [72] reports the first TDC-based PLL that achieves sub-50-fs integrated jitter with a significantly improved TDC resolution. However, its power consumption of 56 mW is large. Hence, its $\text{FoM}_{\text{jitter}}$ is still higher than –250 dB. This is mainly because that the high resolution TDC with low thermal and flicker

noise is usually power hungry.

To relax the power consumption issue, the D-SSPLL/D-SPLLs[74–76] are proposed. A low-resolution ADC (including 1-bit ADC, which is also called bang-bang PD[74, 76]) with low sampling rate of the reference frequency is used to digitalize the output of SSPD or SPD. Hence, it combines the advantages of SSPLL/SPLL's high PD gain and low jitter with DPLL's small area. As illustrated in Fig. 4, D-SSPLL/D-SPLL can achieve FoM_{jitter} between –250 and –253 dB. This indicates that the D-SSPLL/D-SPLL can reduce the performance gap.

Besides the PLLs introduced above, the ILCM is also a low-cost solution to achieve low-jitter performance by simply injecting a clean pulse to the oscillator to simultaneously suppress the in-band and output phase noise of the PLL[70]. State-of-the-art ILPLLs achieve sub-70-fs integrated jitter and <–250 dB-FoM at the frequency of over-20-GHz[77, 78]. The main drawback of the ILPLL or ILCM is its worse spur level compared with other low-jitter PLLs. Hence, low spur level is also a key research focus for ILPLL or ILCM. Recently, the spur level of state-of-the-art ILCM reaches below –70 dBc[79], which is comparable with other low-jitter PLL with low spur level.

As discussed above, the SSPLL/SPLL (including analog and digital architectures) and the ILPLL/ILCM, achieve better performance than the CPPLLs in terms of jitter and FoM_{jitter}. However, actually, the CPPLL is still the most widely used architecture in the industry. The main reason is that the unlimited locking range makes the CPPLL robust to maintain its locking state over any disturbance[80]; whereas other PLL architectures are more vulnerable to the disturbance because they suffer from the risk of losing lock due to their limited locking range, and thus requires additional settling process for frequency relocking with the help of auxiliary building blocks. However, recently, more and more efforts are made to develop the fast relock technique (e.g. the technique proposed in Ref. [65]) for these PLL architecture to mitigate this issue. This will make these low-jitter PLL architectures more robust and attractive for the industry.

In summary, both analog and digital sampling/sub-sampling PLLs are popular for low-jitter low-power PLL design, because the analog SSPLL/SPLL achieves the best FoM_{jitter} of –259.2 dB and lowest integrated jitter of sub-50 fs, and also dominate the state-of-the-art PLL performance; the digital sampling/sub-sampling PLLs can effectively reduce the performance gap between analog and digital PLLs with the advantage of smaller area. In addition, the development of spur reduction technique makes the ILPLL or ILCM become attractive as a low-cost low-jitter clock generation solution; and the continuous research on the fast relock technique is improving the robustness of the SSPLL/SPLL and ILPLL/ILCM.

3.4. Critical building blocks in communication system

In this subsection, we are going to discuss some commonly used critical building blocks in communication systems, including power amplifiers, voltage-controlled oscillators, and crystal oscillators.

3.4.1. Power amplifiers

Power amplifiers (PAs) are still one of the most important building blocks in wireless transceivers since it dominates the power consumption of transmitters. Therefore, PA is currently a very active research area. Various PAs spanning from RF bands to terahertz bands towards higher efficiency, higher output power, more compact chip area, and so on are published in recent year's ISSCC and JSSC, including millimeter-wave (mm-wave) CMOS PAs with Watts-level output power, both digital and analog PAs with back-off efficiency enhancement, large-scale power-combining CMOS PA, wideband PAs, and mm-wave PA in GaN HEMT process and in CMOS FinFET process. Fig. 6 surveys the state-of-the-art PAs in different process. Particularly, the frontier mm-wave CMOS PAs have close to 50% peak power added efficiency (PAE) and near 30 dBm saturated output power (P_{sat}). Among those works, the major research efforts have been focused on improving the deep back-off efficiency of the PAs, including linear PAs and digital PAs, to support advanced modulation. The most recently published linear PAs work at the millimeter-wave (mm-wave) frequency range, driven by the rapid development of 5G mm-wave communications, where the huge power consumption is still the bottleneck. On the other hand, most digital PAs work at a frequency below 10 GHz due to the degraded transistor switching performance at a higher frequency range.

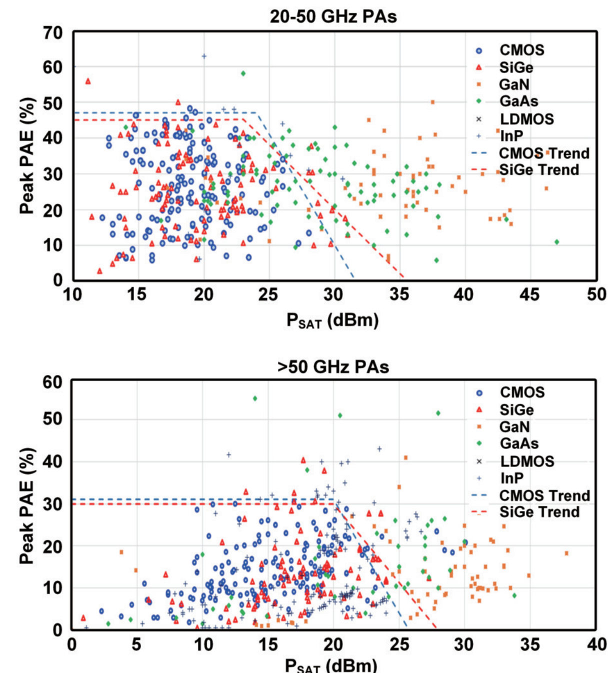


Fig. 6. (Color online) The state-of-the-art PA peak PAE and P_{sat} performance in different processes[90].

For mm-wave linear PAs, the Doherty architecture, been invented in 1936 and hot for several decades, is still the most popular technique to improve the back-off efficiency nowadays. Various Doherty PA implementations on silicon have been demonstrated[81–84]. In Ref. [81], a mixed-signal Doherty PA composed of an analog main path and a digital auxiliary path is proposed to create multiple back-off efficiency enhance points with a small power step. However, the digital auxiliary path control is complicated, limiting the modulation symbol rates. The textbook Doherty PA uses a quarter wavelength transmission line as the impedance inverter, which is not suitable for on-chip implementation due to the area and insertion loss of long transmission lines. Various on-chip lumped element networks have been proposed to re-

place the transmission lines for compact chip area and low insertion loss[82–84]. At a low mm-wave frequency range, transformers are proven to be one of the optimal choices. A parallel-series 3-way transformer-based Doherty PA in 55-nm bulk CMOS is reported in Ref. [82], achieving 20.4% and 14.2% PAE at 6 and 12-dB back-off at 28 GHz. Marchand balun like coupler has also been used in the Doherty PA for wideband back-off efficiency in Ref. [83]. At frequencies higher than 100 GHz, on-chip transformers face degraded performance due to the small diameter, increased parasitics, and reduced port balance. The slotline-based technique proposed in Ref. [84] provides attractive method to realize the on-chip power combining and Doherty operation above 100 GHz. The slotline-based Doherty PA reported in Ref. [84] has 22.7 dBm saturated power (P_{sat}) and 12.1% PAE at 6-dB back-off at 110 GHz. Besides Doherty PA, the recently emerging load-modulated balanced amplifier (LMBA) can also improve the back-off efficiency by modulating the impedance from the isolation port of a hybrid coupler. As demonstrated in Ref. [85], LMBA has the potential for wideband operation. Regarding higher output power, massive-scale power-combining technique has been demonstrated in Ref. [86]. Using 128-to-1 power-combing architecture, the CMOS PA achieves a 1.6 W output power above 100 GHz, which established a new benchmark for CMOS PA.

For digital PAs, the switched-capacitor PA (SCPA) has been the dominated architecture due to its easy implementation, well matching, and flexibility. Recent researches about the SCPA focus on the back-off efficiency enhancement method such as Doherty power-combining, subharmonic switching, and floated-capacitor techniques. Transformer-based power-combining networks introduces Doherty-like operation into SCPAs[87–89]. In Ref. [87], an eight-way power-combining transformer enhances the deep back-off efficiency of a 1.5 GHz SCPA. At 6/12/18-dB back-off, the efficiency is enhanced by 1.77/2.12/1.97 times compared with a class-B PA. In Ref. [88], the back-off efficiency is enhanced by reducing the switching frequency of the SCPA in the power back-off region. In Ref. [89], the transformer-based Doherty power-combining together with the floated-capacitor techniques have been used in a 2.4 GHz Watts-level quadrature PA, the power back-off PAE 6-dB of which is 29.1%.

3.4.2. Voltage-controlled oscillators

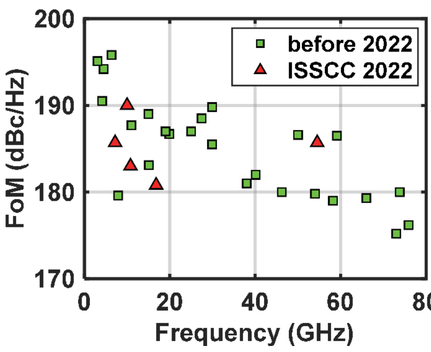
The emerging 5G communication sets a stringent requirement for the phase noise of the local oscillator (LO). As calculated in Ref. [91], the phase noise requirement for 64 QAM at 80 GHz is –102 dBc/Hz at 1 MHz offset frequency. Recently, the effort has been made to improve the phase noise from three directions: the harmonic tuning, the multi-core, and the series-resonant techniques. Fig. 7 summarizes the state-of-the-art oscillator FoM and the FoM with tuning range (FoM_T) at 1 MHz offset versus frequency.

Harmonic tuning techniques such as class-F, tail filtering, and implicit common-mode resonance have already been proven to be efficient in phase noise improvement, which has been further exploited in recent years[92, 93]. In Ref. [92], a single-turn multi-tap inductor is employed in a 25.5-to-29.9 GHz and 191.6 dBc/Hz FoM VCO to create high Q high impedance resonances at the 1st, 2nd, and 3rd harmonic frequencies. The single-turn multi-tap inductor has the advantage of higher Q in the mm-wave frequency range over conventional multi-turn transformers. In harmonic tuning VCOs, the harmonic peak impedance frequency misalignment degrades the phase noise. In Ref. [93], a head-resonator consisting of two inductors and one capacitor is added to a 5.0-to-6.36 GHz VCO to create a wideband 2nd harmonic response, eliminating the need for dedicated 2nd harmonic capacitor tuning, and suppressing the flicker noise over the whole oscillation frequency range.

It is well known that an N core oscillator can improve the phase noise by 10log(N) times. In Ref. [94], a 3.09-to-4.04 GHz quad-core oscillator using distributed-boosting transformers is proposed. The high-order distributed-boosting transformer network provides the freedom to implement harmonic tuning and impedance expanding in addition to the multi-core, which significantly improves the phase noise and FoM. The proposed oscillator achieves excellent –138.9 dBc/Hz phase noise and 195.1 dBc/Hz FoM at 1 MHz offset. The authors in Refs. [95, 96] show that a mode-rejected multi-core topology favors the mm-wave operation compared with resistance-coupled multi-core because the slab topology inductors in the mode-rejected topology can achieve a very small inductor (~20 pH) with considerably high Q (>25). The reported phase noise and FoM of the 60 GHz quad-core[95] and 16-core[96] oscillators are –104.7 and 186.5 dBc/Hz, and –111.1 and 185.7 dBc/Hz at 1 MHz offset, respectively. The multi-core oscillator draws more current from the power supply, thus lowering the phase noise. It has an inevitable chip area overhead, although not significant in the millimeter frequency range.

This year, the series resonance VCO presented in Ref. [97] emerges, providing an interesting alternative method that is to draw more current to trade for phase noise. In this work, the LC tank is arranged in a series-connected form, therefore creating a near-short path at the resonance frequency, and drawing a great amount of current from the source using only one single inductor. The VCO reports a phase noise of –138 dBc/Hz and FoM of –190 dBc/Hz at 1 MHz offset from 10 GHz. The series-resonance is a promising low-phase-noise technique with unsettling challenges. The first challenge is the suitable negative resistance in the CMOS process. The second challenge is the frequency tuning range (FTR). To protect the variable capacitance for the boosted voltage swing in the series-resonance VCOs, the efficient max-to-min capacitance ratio is sacrificed through a voltage divider.

Besides low-phase noise, very wide FTR VCOs are also attractive to support the widely distributed frequency bands allocated for 5G communication. Usually one octave FTR is considered sufficient since all lower frequencies can be generated by cascaded frequency dividers, whose design cost is low. The most straightforward way to improve the FTR of an LC oscillator is to scale up the size of the switched-capacitor arrays to improve the max-to-min capacitance ratio. However, this solution faces the fundamental trade-off between the on-resistance and off-capacitance of the transistor switches, which translates to the trade-off between the max-to-min capacitance ratio and the tank Q and the trade-off between the FTR and phase noise. On the other hand, the mode-switching technique[98–100] has shown superior performance on improving the FTR while less affecting the phase noise, which is still a very active research area. In Ref. [98], a dual-mode dual-core VCO using a 4-port resonator exhibits a



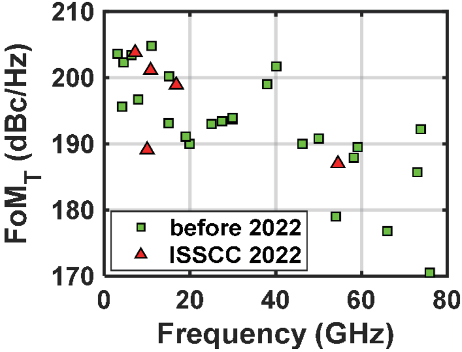


Fig. 7. (Color online) The state-of-the-art oscillator FoM and FoM_T at 1MHz offset versus frequency.

41.3% FTR from 25 to 38 GHz, corresponding to 195 dBc/Hz FoM_T. To further extend the FTR, a quad-mode quad-core VCO using EM mixed coupling and a triple-mode dual-core VCO using 4-port resonator are proposed in Refs. [99, 100], respectively, which achieve 73.2% FTR from 18.6 to 40.1 GHz with 201.7 dBc/Hz FoM_T and 80.6% FTR from 7.1 to 16.8 GHz with 204.4 dBc/Hz FoM_T, respectively.

The mode-switching technique has been proven to be successful in wide FTR VCOs. However, two major design challenges remain. The first is to further reduce the parasitic capacitance introduced by the mode-switching technique, such as the coupling capacitors in Ref. [99] and the off-state cross-coupled pairs in Ref. [100]. The second is to suppress the flicker noise over the more than octave FTR, especially in advanced process nodes, the satisfied solution to which is still missing in literature.

3.4.3. Crystal oscillators for IoT devices

Lowering the startup time (t_s) and energy (E_s) of the crystal oscillator (XO) for the IoT devices has been an emerging and popular trend in recent years[101]. Fueled by the demands on extending the battery lifetime of the IoT devices, or eventually culminating in perpetual operation with energy harvesters, duty-cycling the power-hungry transceivers becomes a popular approach. It effectively reduces the overall power consumption by putting the transceivers into sleep mode for a prolonged period. As an indispensable part of the radio transceiver, the XO is praised for its excellent frequency stability and spectral purity. Yet, these advantages come at the expense of a long t_s due to the high quality factor (Q) of the quartz crystal; the MHz-range XO takes a matter of milliseconds to start if no startup technique is presented. This long t_s hampers the duty-cycling operation. Further, the requisite energy to start the XO remains a bottleneck to the power reduction efficacy of the IoT radio brought by the duty-cycling technique.

In this regard, there is a thrust to radically improve the t_s and E_s of the XO, as shown in Figs. 8(a) and 8(b), such that the IoT transceivers can be duty-cycled efficiently to reduce the average power consumption. Essentially, the fast startup techniques of the XO can be categorized into negative resistance boosting and energy injection. The negative resistance boosting technique boosted the negative resistance (R_N) of the amplifier sensed by the crystal[102–111]. A negative resistance is compulsory to compensate for the resistive loss of the crystal unit and fulfill the Barkhausen stability criterion to support the oscillation of the XO. Besides, the R_N is also influential to the t_s. In the beginning, the XO builds up its amplitude from the thermal noise that existed in the circuit. The growing rate of the XO's amplitude is proportionate to the R_N. Hence, a high R_N effectively shortens the t_s by promoting the exponential growth of the XO's amplitude. As no extra oscillator or sensing circuit is necessary, the hardware overhead for the negative resistance boosting technique is minimized.

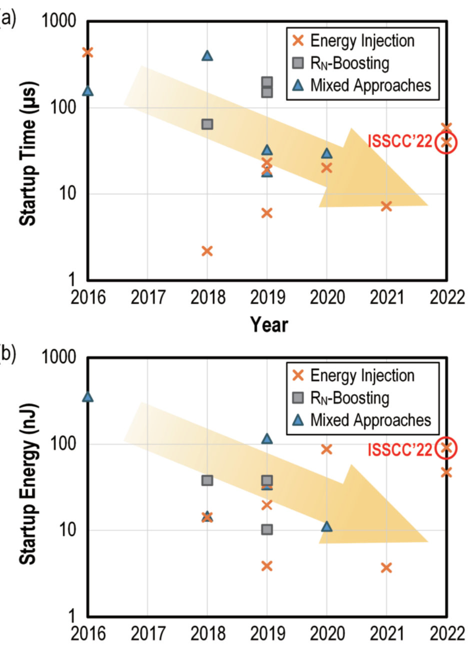


Fig. 8. (Color online) The trends of (a) startup time and (b) startup energy of the MHz-range fast startup XO.

Instead of waiting for the crystal to accumulate its amplitude, the quintessence of energy injection technique is to pour energy into the crystal by exciting it with an auxiliary signal[102, 105, 107, 110–120]. Although its foundation is relatively straightforward, the injection source must have frequency content in close proximity to the resonant frequency of the crystal ($\Delta f < 5000$ ppm, depending on the final XO-swing and the injection duration) to excite the crystal effectively due to its high-Q bandpass nature. To this end, substantial endeavors have been invested in recent years to properly inject energy to the crystal, such as dithering, two-step injection, signal synchronization, etc. At ISSCC 2022, a fast startup XO based on the energy injection method is proposed[119]. The startup of the XO is expedited by the initial dithering and a sampling

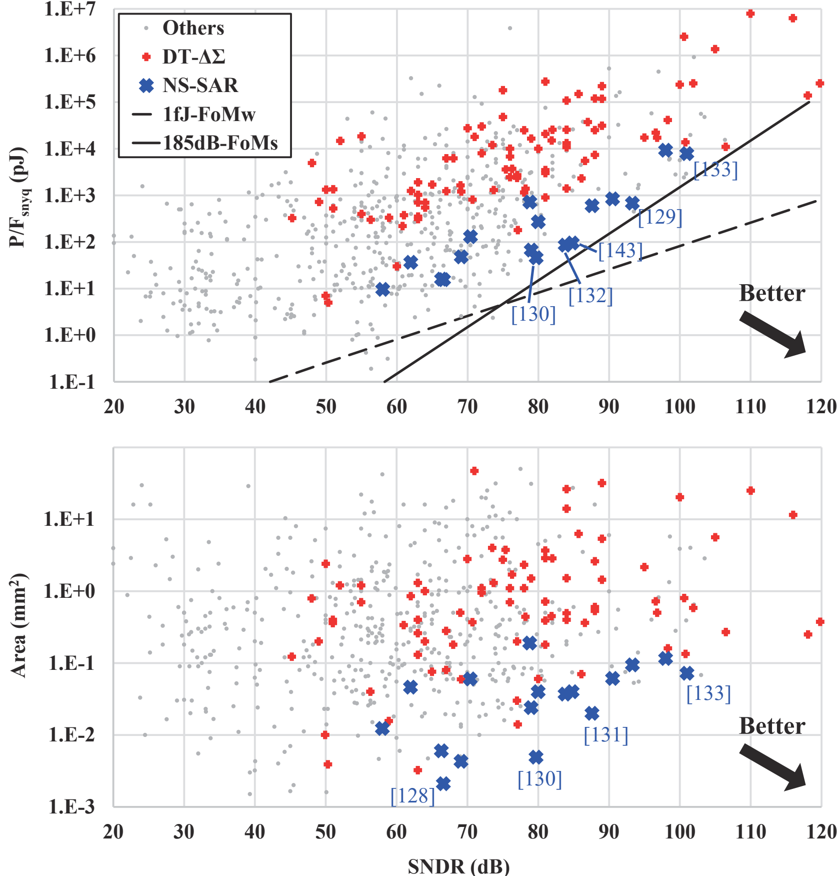


Fig. 9. (Color online) Comparison between NS-SAR and conventional architectures.

phase-locked loop (S-PLL). The initial dithering signal generated by the injection voltage-controlled oscillator (i-VCO) is injected into the crystal at the beginning to produce a 0.2-V XO-swing robustly. The frequency of the i-VCO is then locked onto this XO signal by the S-PLL in 8 μs. Finally, the accurately locked signal is re-injected to the crystal for another 12 μs to yield an XO-swing of 1.2 V. It achieves a t_s of 39.6 μs and E_s of 92.8 nJ, attaining 18.2× and 6.4× reductions compared to that without startup technique, respectively.

Stimulated by the expansion of the ultra-low-power IoT market, we expect that the research on the fast startup technique for the XO will continue to be active in 2022 and beyond. Even though the t_s of the fast startup XOs implemented recently are close to the theoretical minimum, for instance, a mere 17% of the E_s is delivered to the core of the crystal[118]. Hence, there is still significant room to improve the energy efficiency of the startup scheme. On top of this, the energy injection technique requires a precise source signal. Consequently, we expect this will also prompt the research on the fully-integrated low-power oscillators[121, 122] and associated calibration methods, especially using the signal from the XO itself[119].

4. Data converters

There have been significant advances in the design of data converters over the past decade. This review article covers three major directions as demonstrated in latest ISSCC works. The first one is a novel hybrid architecture called noise-shaping successive approximation register (SAR) ADCs. The second is high-resolution incremental ADC. Last but not least, state-of-the-art pipelined ADC developments will also be reviewed.

4.1. Noise-shaping SAR ADCs

The noise-shaping SAR (NS-SAR) is a promising hybrid architecture emerged in past few years. NS-SAR is a hybridization of the SAR and the delta-sigma (DS) architectures, and it benefits from the both side: it is low-power and area-efficient like SAR, and provides high SNR as DS ADCs. NS-SAR is also easy to down-scale and good for advanced CMOS processes. Fig. 9 shows a power and area comparison between NS-SAR and other architectures[123], where NS-SAR exhibits significant advantages over discrete-time DS ADCs. Therefore, NS-SAR is getting more and more interest from the ADC community recently. Various techniques are proposed and steadily improving the performance of NS-SAR in all aspects. Fig. 10 plots the Schreier figure of merit (FoMs) and bandwidth (BW) of NS-SAR over years. Roughly, FoMs increases by 6.4 dB, and BW increases by 8.4× per decade.

Fig. 11(a) shows a basic framework of NS-SAR, which is modified from SAR ADC[124]. Generally, an NS-SAR consists of three parts: 1) A SAR ADC core that samples and quantizes the input signal. In most designs it is a capacitive digital-to-analog converter (CDAC) based one, and a residue voltage (V_{RES}) left on the CDAC at the end of conversion; 2) A loop filter (H_{EF} and/or H_{CIFF}, depends on architecture) that processes the residue, which is also highly efficient and scaling-friendly; 3) A signal adder that feeds back the loop filter's output. Fig. 11(b) shows the signal model of the NS-SAR in Fig. 11(a), where E_S is the errors and noise added by samp-

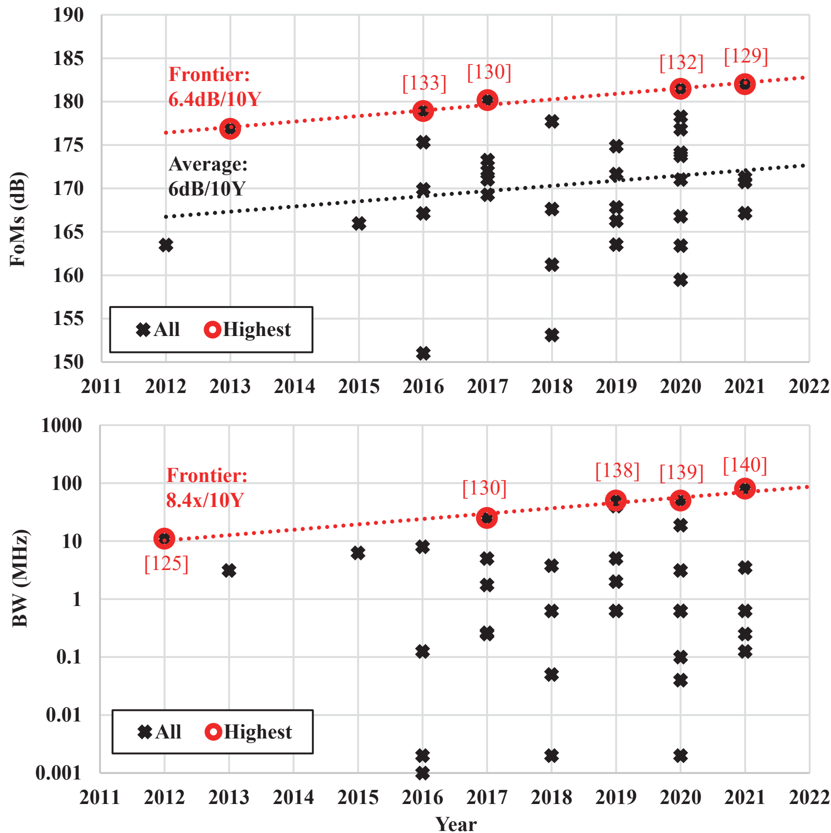


Fig. 10. (Color online) Schreier figure-of-merit (FoMs) and bandwidth (BW) of NS-SAR over years.

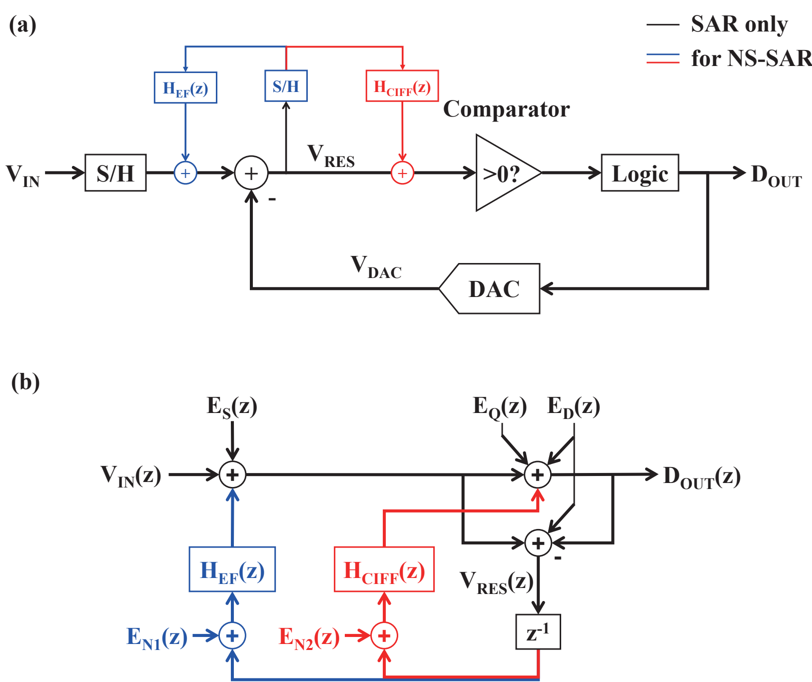


Fig. 11. (Color online) (a) The basic framework of NS-SAR, and (b) its signal model.

ling (e.g., kT/C noise), E_Q is the quantization error including comparator noise, and E_D is DAC mismatch errors. Loop filter H_{CIFF} forms the cascaded-integrator feed-forward (CIFF) structure[125] and H_{EF} forms the error-feedback (EF) structure[126]. E_{N1} and E_{N2} are the input-referred noise of the two filters. z^{-1} is the delay from residue sampling, which is the minimum loop delay in NS-SAR. We can derive the signal transfer function (STF) and noise transfer function (NTF) as:

$$\mathrm{STF}(z) = \frac{D_{OUT}(z)}{V_{IN}(z)} = 1,$$

$$\mathrm{NTF}(z) = \frac{D_{OUT}(z)}{E_Q(z)} = \frac{1 - H_{EF}(z)z^{-1}}{1 + H_{CIFF}(z)z^{-1}}. \tag{1}$$

However, in NS-SAR, E_{N1}, E_D and E_S are not suppressed, and E_{N2} is only suppressed by the EF loop. Since H_{EF} is on the numerator of the NTF, a simple FIR H_{EF} can implement the zeros in NTF, making EF-NS-SAR simple in implementation. H_{CIFF} is on the denominator of the NTF and it needs high gain integrators to suppress E_Q. However, EF-NS-SAR is more sensitive to filter-gain because H_{EF} should be close to 1 in the signal band. CIFF-NS-SAR is more tolerant to variation as long as H_{CIFF} is large enough.

Despite the advantages over DS ADC, NS-SAR also has various challenges, which are the main focus of current research. The main challenges in NS-SAR architecture are in four aspects: loop filter, DAC mismatch, bandwidth limitations, and kT/C noise.

4.1.1. Loop filter

The loop filter is the most critical analog block in NS-SAR, and it dominates the SNR and power efficiency. For efficiency and scaling purpose, the loop filter in NS-SAR is usually opamp-free and uses simpler alternative schemes. Many recent NS-SAR designs adopt passive switched-capacitor loop filters as they are simple, linear, PVT robust, efficient, and scaling-friendly. But passive filter is not able to provide sufficient loop gain, and thus additional active gain is usually necessary for high performance noise-shaping, including: 1) Opamp is used in some early NS-SARs[125] but is known to be less efficient. 2) Multi-input comparator with different input differential-pair sizing[127] can provide a moderate gain and signal summation. It is simple and dynamic, and is thus popular in some early designs. However, it can only implement the CI-FF structure, and it is noisier due to the extra input pairs. Thus it is hard to achieve high SNR by using a multi-input comparator. 3) Capacitor stacking[128] provides mild gain by first charging two capacitors and then connecting them in series. It is fully passive, highly linear, and low noise. It can also provide a free gain of 2× and eliminate the common mode by using differential sampling[128]. The main drawback of capacitor stacking is that it can hardly drive any resistance load, and it is highly sensitive to parasitic capacitances, but these can be solved by adding an active amplifier or buffer[129]. This is one of the most popular schemes in recent NS-SAR.

Another popular scheme is using optimized active amplifiers, such as dynamic gm-C amplifiers[130] and open-loop gm-R amplifiers[131]. They are more power-efficient and are more scaling-friendly than op-amps, however at the cost of higher sensitivity to PVT and timing variations. Recent amplifiers, such as floating inverter amplifier (FIA) and closed-loop dynamic amplifier[132], achieve a better balance between performance and robustness, and push the FoMs of NS-SAR to over 180 dB without compromising PVT robustness. On the other hands, cascaded NS-SAR architecture[131] addresses amplifier's variation by placing NS-SAR in a nested structure and forming a cascaded NTF. It has much better tolerance to the variations in NTF coefficients, especially for high order NTFs. Besides, it shapes the thermal noise of the former stages and improves power efficiency. This method enables NS-SARs with aggressive 4th-order NTF[131].

4.1.2. DAC mismatch

DAC mismatch causes significant accuracy degradation in NS-SAR and it cannot be suppressed by noise shaping. A direct scheme of reducing the DAC mismatch is enlarging the DAC. But it is too costly and is rarely practical. Another popular method is digital calibration, either in foreground or background. However, foreground calibration takes extra testing cost and cannot deal with real-time variations; background calibration can track variations in real-time, but it is much more complicated and converges slower.

Mismatch-shaping (MS) is another solution to DAC mismatch for oversampled ADCs such as NS-SAR. It does not rely on the prior knowledge or measurement of the mismatch. There are two popular MS schemes: dynamic element matching (DEM) and mismatch error shaping (MES)[133].

DEM is based on an element selection logic (ESL) that activates the DAC elements in a certain pattern, such that the mismatch error is irrelevant to the DAC code and suppressed in-band. Data weighted averaging (DWA) is one of the most popular ESL that 1st-order shapes the mismatch error, and some advanced ESL techniques[134] can achieve higher-order shaping with more complicated logic. The main drawback of DEM is that it uses unary DAC, which makes circuit cost exponentially glowing as the DAC resolution increases. Therefore, most NS-SARs apply MES to only a few MSBs, limiting its effectiveness.

In contrast, MES captures the mismatch error in the analog domain and feeds it back for noise-shaping. Specifically, we can preset the CDAC's least significant bits (LSBs) before sampling, such that the mismatch error from the previous conversion is captured and subtracted in the current conversion, and the preset LSBs are then subtracted from the current digital output. Compared to DEM, MES is relatively simple and works for binary DAC. The main drawback of MES is that the presetting of the CDAC also feeds back the previous input signal, which occupies a part of the input range. This issue can be mitigated by using larger bits of MSB[133], digital prediction[135], or pre-comparison[136].

4.1.3. Bandwidth limitation

Due to oversampling and the multi-cycle SAR conversion, NS-SAR trends to be limited in bandwidth. Time-interleaving (TI) is a common solution to increase the sampling rate, but TI is not compatible with noise-shaping ADC because of the memory effect in them. Some early examples of interleaved noise-shaping ADC[137] pass the residue between channels to keep noise-shaping property. But the inter-channel feedback stalls the quantizers, and makes them effectively running at the full rate. Therefore the designs achieve 2-way interleaved only and show limited advantages. On the contrast, NS-SAR is more suitable for time interleaving because SAR conversion can accept feedback signals during the multi-cycle conversion process. TI-NS-SARs thus do not need to run the SAR quantizer faster and can preserve the efficiency advantage.

TI-NS-SARs can be implemented in EF form[138] and CIFF form[139]. TI-NS-SAR in EF form feeds the residue between channels, and TI-NS-SAR in CIFF form shares a global loop filter between channels. TI-NS-SAR has lower sensitivity to channel mismatch because most errors from channel mismatch are at high frequency and are out-of-band, if the oversampling ratio (OSR) is larger than the channel numbers. Recently, TI-NS-SAR (in CIFF form) can achieve 80 MHz bandwidth with 66 dB signal to noise and distortion ratio (SNDR)[140].

4.1.4. kT/C noise

Another challenge in NS-SAR is the input sampling. Since

Fig. 12. (Color online) Block diagram of DT-Slicing IADC in Ref. [150].

the kT/C noise is not shaped, a large CDAC is necessary in high-resolution ADCs, which brings a large burden on the input driver. Oversampling reduces kT/C noise by the OSR, thus the sampling capacitor can be OSR-times smaller. But as the sampling frequency increased, the input driver has to charge the capacitor faster and is not fully relaxed.

There are two techniques to reduce the kT/C noise[141]. Firstly, we can decouple the noise source impedance and the noise bandwidth by a feedback circuit. A SAR ADC[142] achieves 3.5× kT/C noise reduction by this method. Secondly, we can use an extra amplifier and a sampler to capture the kT/C noise and then cancel it out in a later phase. In an ideal case, this technique completely removes kT/C noise at the cost of introducing amplifier noise and power. This method will also limit the input bandwidth and thus is very suitable for NS-SAR. An NS-SAR[143] achieve 87 dB DR with only a 0.8 pF sampling capacitance by this method. Essentially both techniques trade sampling capacitance for amplifier cost. The amplifiers in these techniques process only small signals and thus they can be less costly than the input drivers that need to process large signals.

4.1.5. NS-SAR directions

There still remain many interests in NS-SAR research regarding the following topics: 1) Higher speed, 2) higher resolution, 3) reference buffer, and 4) further hybridization.

1) The highest reported NS-SAR BW is only 80 MHz (with interleaving)[144]. There are two possible directions to further increase BW: a) Speedup SAR conversion by using some existing techniques in conventional high-speed SAR ADCs, such as multi-bit-per-cycle conversion[145], loop-unrolling[146], and ping-pong comparator operation. b) Optimize the loop filter with advanced filtering methods, such as continuous-time (CT) filters.

2) For higher resolution, few published NS-SARs can achieve >100 dB SNDR so far, but many applications, such as audio and sensing, requires dynamic range over 120 dB. Advanced mismatch-shaping or low-cost background calibration is the key to this goal.

3) Most NS-SAR design relies on massive reference decoupling capacitors and rarely discuss practical reference generation. It remains chances to co-design a reference buffer optimized for NS-SAR, which might be beneficial as NS-SAR emphasizes an accurate residue at the end of conversion, and has a higher tolerance to the reference error during conversion.

4) NS-SAR can be further hybridized with other architectures. NS-pipeline-SAR[147] and CT ADC with NS-SAR[148, 149] are two good examples. Possible choices are the incremental and zoom architectures, as both offer high resolution but are not very scalable, which are going to be discussed next.

4.2. High resolution incremental ADCs

In recent research developments of high-resolution data converters, the incremental converter (IADC) is one of the excellent candidates to achieve high resolution with the trade-off of reduced bandwidth. Also, different from its delta–sigma counterparts, the IADC incorporates a reset operation in its analog integrators and digital decimators. It exhibits a Nyquist ADC property in terms of out-of-band noise processing, allows multiplexing, and leads to a simple decimation filter and thus significantly reducing the latency in digital post-processing. The recent development trend of IADCs will be qualitatively discussed below.

4.2.1. Slicing or reconfigurable IADCs

In the delta-sigma modulators or IADCs, the first integrators occupied the most power consumption because of the thermal noise considerations. The later stages' performance were benefited from the gain of the first stage, and their capacitors can be selected with a small size. As a result, reconfigurations of the loop filters are proposed in works[150, 151] to dynamically decrease the power consumption of the first integrator.

Fig. 12 depicts the simplified schematic of a 3rd-order IADC with the slicing integrator by utilizing the property of the non-uniform input weighting function[150]. The first integrator is split into four identical slices, which can be independently activated for $k_{1,2,3,4}$ = 40, 30, 10, 70 cycles, and the power consumption can be reduced in the latter cycles. A minor penalty is a result of only 0.7 dB/0.8 dB loss in SNR/SNDR due to the signal loss. Another similar implementation is presented in Ref. [151] with reconfigurable capacitor scaling along with the accumulation. However, the 3rd order loop filter suffers from thermal noise and mismatch averaging penalty (a penalty factor of 1.8 in 3rd-order[152]). Thus, Ref. [150] uses a single-bit quantizer to keep the linearity.

4.2.2. Exponential IADCs

The resolution of traditional incremental ADCs can be improved by cascading the integrators with increasing orders, resulting in a faster accumulation. The modulator accu-

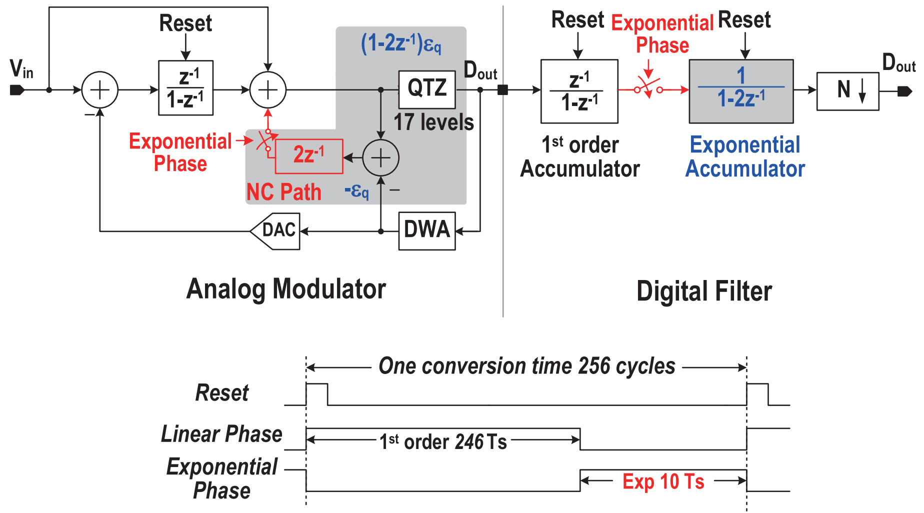


Fig. 13. (Color online) Block diagram of DT Linear-Exponential IADC in Ref. [152].

mulates from linearly to bi-quadratically with increasing oversampling ratio (OSR) from 1st- to 4th-order IADCs. Straightforwardly, one can build an exponential growth of accumulation (instead of order-based accumulation), which is the fastest way by nature. However, the exponential accumulation dramatically reduced the required OSR by emphasizing the strong accumulation weights at the beginning of the accumulation cycles, causing penalties in the thermal noise and mismatch averaging efforts in DWA. As a result, the fast exponential accumulation simultaneously served as the pros and cons for such architecture at the same time. The noise and mismatch averaging penalty factors range from 1 to 2.3 from 1st- to 4th-order IADCs, and for the exponential accumulation, the effort of oversampling is completely killed[152].

Indeed, for high-resolution IADCs, there are two kinds of fundamental noises required to be suppressed during the conversion: the smaller thermal noise and the larger quantization noise. The oversampling ratio can only reduce the thermal noise (given a fixed capacitance), while a faster accumulation growth can suppress the quantization noise. As illustrated in Fig. 13, Ref. [152] proposed a single-loop IADC combining a 1st-order integrator for the linear accumulation in 246-cycle, and during the latter 10-cycle, the integrator is reused with the noise-coupling quantizer to generate exponential accumulation. With such a combination, the noise and mismatch penalty factor of this work is 1.03, very close to the baseline in 1st-order IADC.

4.2.3. Hybrid IADCs

High-order incremental ADCs provide faster accumulation but induce thermal noise penalty. On the other hand, hybrid architectures are developed to overcome the long conversion time of low-order (⩽2) IADCs. The basic concept of the hybrid IADC is to digitalize the residue of the coarse ADC further to reduce the final quantization noise in the output of the ADC. The residue estimation will combine with the decimated output bit-stream in the digital domain, canceling the quantization error. In a work[153], a multi-step incremental ADC with a single op-amp uses multi-slope extended counting to achieve 16-bit resolution with 320 (256-32-32) clock cycles. The residue voltage of the coarse quantization is canceled and passed to the next step by reconfiguring the switched-capacitor array in the integrator. Thus, it is more robust than the traditional extended counting ADC because of the smaller residue, which is less sensitive to non-ideal effects.

Zoom IADCs[154–156] are another typical example of hybrid IADCs. The hybrid uses a SAR ADC initially to make a coarse conversion, and the preliminary digitalization would be used to adjust (or "zoom") the reference of the fine IADC. Recently Ref. [155] (Fig. 14) proposed using a self-timed dynamic amplifier in the integrators, allowing the fully autonomous operation of the complete zoom ADC without using an oversampling clock. A self-time common-mode detector within the dynamic amplifier is proposed. When the discharging of the common-mode voltage of the amplifier reaches the target threshold, the amplifier generates a ready time signal for the next asynchronous operation. Another example of a CT-Zoom-IADC is presented in Ref. [156], where a counting ADC is used in combination with continuous-time incremental zoom to achieve excellent power efficiency.

4.2.4. Continuous-time IADCs

Continuous-time (CT) IADCs have attracted attention for circuit implementation for their simple driving circuitry and low power consumption. Thanks to the resistive input impedance, the front-end preceding driver does not need to drive the switched-capacitor load. Moreover, the integrators in CT consume lower power than the discrete-time (DT) counterpart.

Its resetting operation is one of the largest differences between the CT IADC and the CT delta-sigma ADC (CTDSM). This results in reduced anti-aliasing performance and the resettling of the FIR DACs. In CTDSM, since the converter is free-running, the loop filter can be designed and considered as an IIR filter, setting up a satisfactory anti-aliasing rejection. If the FIR DACs are used, the free-running operation of the DAC in CTDSM will perform well in steady-state also. While for the cases of CT-IADCs, the resetting operation causes two issues: 1) the integrator memory is reset, which effectively translate the loop filter as an FIR filter, degrading its anti-aliasing performance; 2) the resetting operation of the FIR-DAC feedback induces a long settling behavior at the beginning of the incremental accumulation. In Ref. [157], a careful reset

Fig. 14. (Color online) Block diagram of DT-Zoom IADC in Ref. [155].

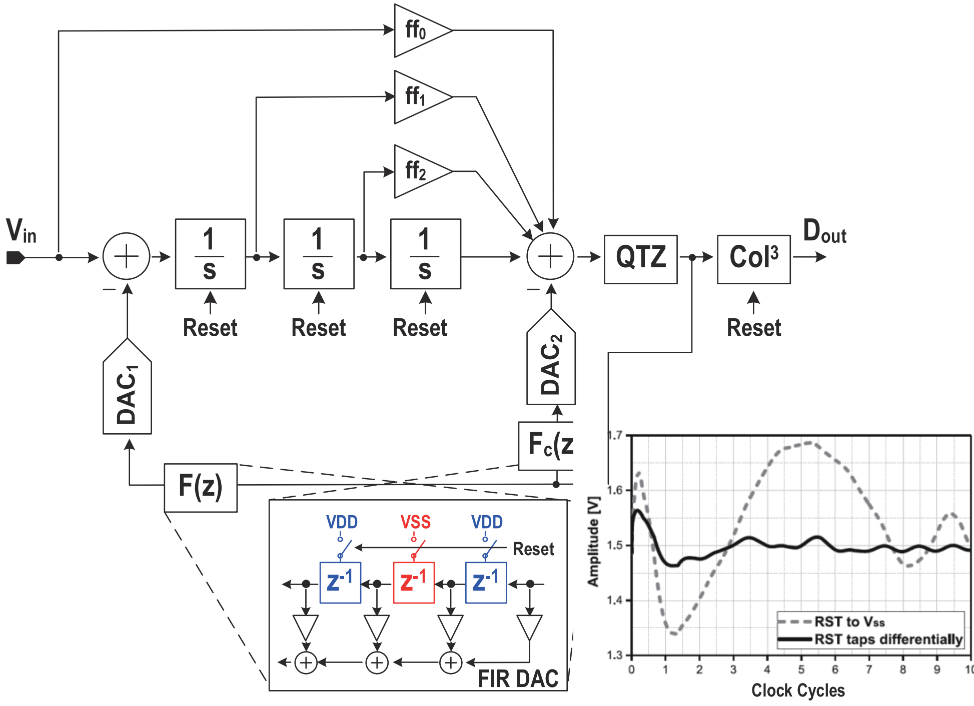


Fig. 15. (Color online) Block diagram of CT IADC in Ref. [157].

of the FIR DAC register is required (by resetting their registers alternatively to 0 and 1), as shown in Fig. 15. While in Ref. [158], a presetting implementation is utilized.

The loop filters in CTDSM can also be effectively used in the CT IADCs. For example, Ref. [159] proposed a CT-IADC based on a 3-0 Study-MASH CTDSM in Ref. [160]. With the utilization of the unique non-uniform weighting property in the 3rd-order IADCs, the use of combinations of single-bit/multi-bit DAC feedbacks allows the calibration-free DWA-free multi-bit IADC.

4.2.5. Incremental ADCs comparison and discussion

Table 3 summarizes the above-discussed IADCs and compares their performance. They are power efficient, achieving >160 dB FoM_S (SNDR) for wider bandwidth and >175 dB for lower bandwidth. Fig. 16 also shows a state-of-the-art comparison chart for the Nyquist ADCs published in ISSCC and VLSI so far. It is worth noting that most published Nyquist ADCs reach performance bottleneck as highlighted by the "Nyquist gap"[161] in Fig. 16 (all data points sourced from B. Murmann[123]), and IADCs strongly show their roles in filling the performance of Nyquist converters within the gap, compared with the other types of Nyquist converters.

4.3. Pipeline hybrid ADCs

The pipelined concept in analog-to-digital converter can be traced back to the 1960s when Servin from Texas Instruments presented a 1 b/stage pipelined ADC in a patent[162], as captured in Fig. 17. Due to the appearance of fast BiCMOS and CMOS processes, pipelined ADCs were widely adopted starting from the 1990s and replaced bipolar/CMOS flash topology in moderate resolution designs.

Table 3. Performance comparison of IADCs.

	P. Vogelmann	S. Mohammad	B. Wang	Y. Liu	L. Jie	M. Mokhtar	M. Mokhtar
	ISSCC'18, JSSC'19, [150]	JSSC'20, [151]	VLSI'18, JSSC'19, [152]	ISSCC'22, [155]	ISSCC'22, [156]	ESSCIRC'19, SSCL'19, [157]	CICC'21, [159]
Architecture	DT Slicing	DT IADC+SAR, cap scaling	DT Linear-Exp	DT Zoom	CT-Zoom-Counting	CT	CTI-SMASH
Tech. (nm)	180	180	65	55	28	180	28
Supply (V)	3	1.8	1.2	1	1.2	3	0.9
Active area (mm^2)	0.363	0.66	0.13	0.23	0.014	0.175	0.125
OSR	150	98	256	128	8192	160	60
Bandwidth (kHz)	100	2.04	20	1.35	25	100	1000
Power (μW)	1098	25.4	550	4.96	590	1270	3600
SNDR (dB)	86.6	95.5	100.8	93*	100.1	83	81.2
SFDR (dB)	101.3	106	121	N/A	113.7	94.3	97
FoM_S (SNDR)	166.2	175	176.4	177.3*	176.4	161.9	165.6

* Only SNR is available for FoMS calculation.

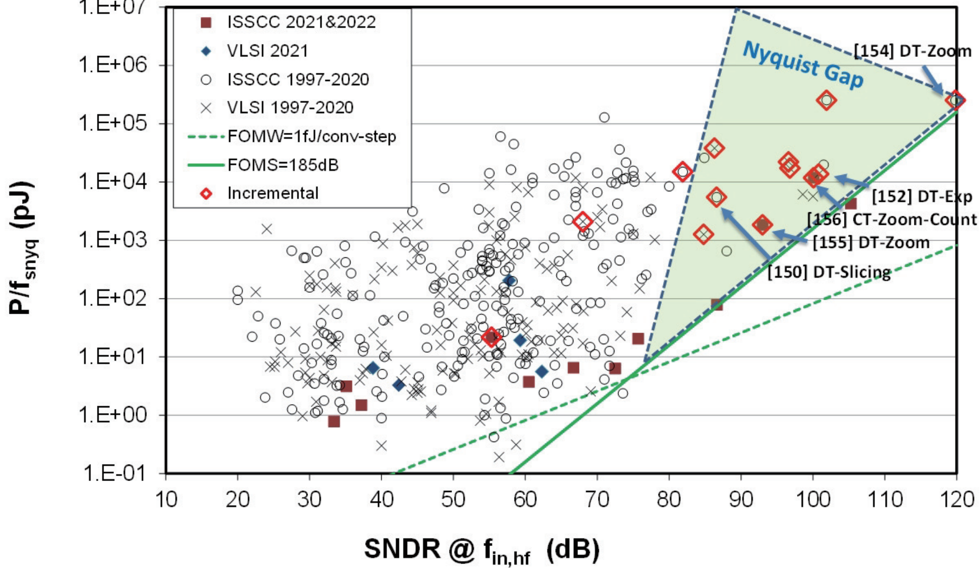


Fig. 16. (Color online) State-of-the-art Nyquist ADCs survey published in ISSCC and VLSI[123, 161].

Through the ADC performance survey done by Boris Murmann[123], it can clearly be observed that the pipelined architecture thrives thereafter in various dimensions, including resolution (SNDR), speed (sampling rate) and energy efficiency (FoM_S). The pipelined technique breaks the conversion into multiple steps (two or more) which speeds up the conversion (when allowing latency) and simultaneously relaxes the requirement of the sub-quantizer with inter-stage gain and redundancy. Even though the pipelined architecture poses a higher design complex, it also enables a new paradigm to hybridize and/or optimize the conversion for various performance targets. Nowadays, the research focus of hardcore pipelined ADC is mainly on speed and digital-assisted solutions. For the high-speed target, except for optimizing the ADC core and residue amplifier design with calibration backup, time-interleaved (TI) technique is also applied. 12 b 3.2, 10 and 18 GS/s TI-pipelined ADCs linearized by calibrations are demonstrated in Refs. [163–165], respectively. They all maintain a competitive FoM_S with a feasible number of interleaving channels, as marked in Fig. 18.

In recent years, the basic operation of the pipelined ADC has been revisited. Conventionally, each stage (except the last one) has to accomplish three major operations in series, including sampling, quantization, and residue amplification. Ref. [166] with post-amplification residue generation (PARG) scheme alters this sequence and allows the quantization and amplification to happen simultaneously. Rather than generating the residue after the sub-quantizer conversion, this new scheme amplifies the input right away after the sampling; simultaneously, the sub-quantizer also makes its decision. The residue is eventually generated after the amplification in the following stage. The PARG can provide a 1.5-fold improvement in the conversion speed compared to the conventional pipelined ADCs with a low-to-moderate resolution target. Indeed, the actual speed improvement is more as the sampling period often prefers half-cycle of the clock. This new arrangement from PARG achieves a top speed of 3.3 GS/s single-channel pipelined ADC (marked as Ref. [166] in Fig. 18).

Another recently proposed technique that changes the nature of conventional pipelined ADCs is to move the architecture in fully continuous-time (CT)[167, 168]. By combining the residue amplification and the filtering, the CT pipelined

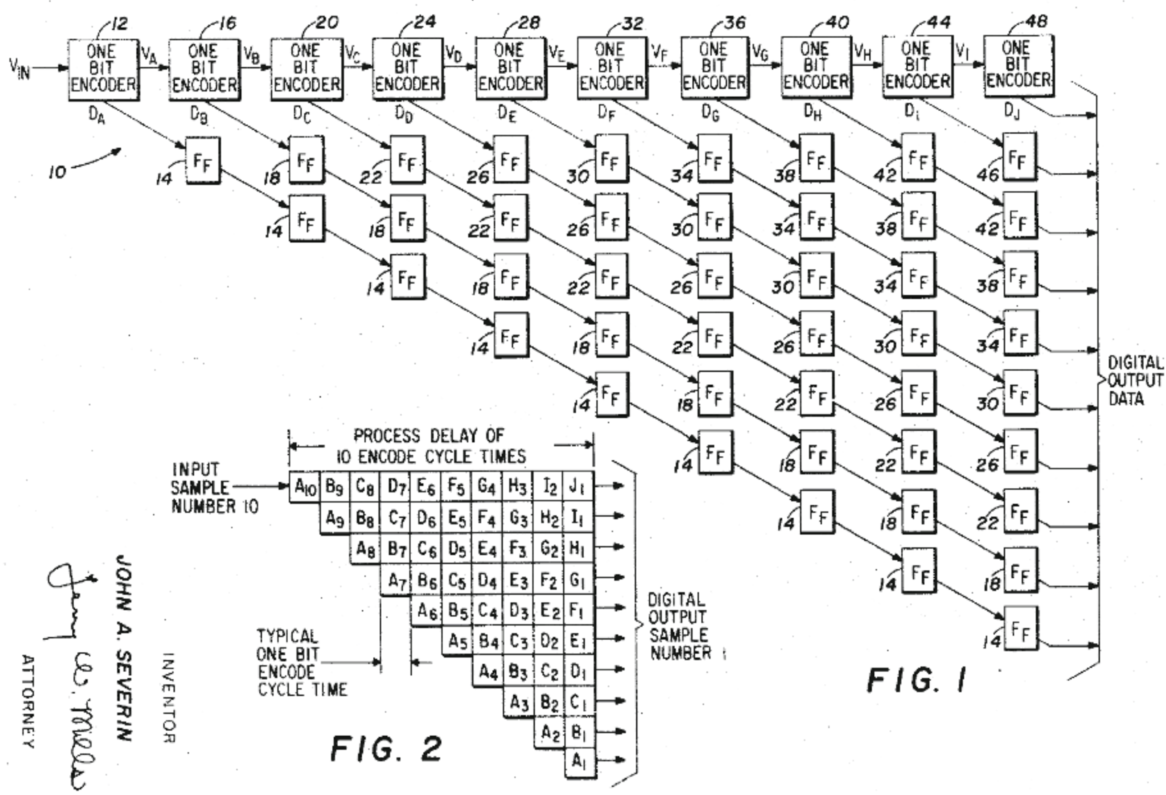


Fig. 17. Early pipelined ADC patent with 1 b/stage[162].

ADCs give a reasonable anti-aliasing performance at wideband. This architecture also relaxes the strict opamp requirement for stability in the conventional CT sigma-delta modulator. This and a later work combined with VCO-based ADC[168] demonstrate a promising performance toward very wideband (0.8–1 GHz bandwidth) CT-ADC designs (marked as Refs. [167, 168] in Fig. 18).

Going for the hybrid is the next popular option that further pushes the pipelined ADC performance. Benefiting from the outstanding energy efficiency of SAR architecture, the hybridization between the pipeline and SAR ADCs has also become attractive. From 2019 to 2022, various SAR-assisted pipelined (Pipe-SAR) ADCs achieve a top FoMs in their corresponding specification range. In Ref. [169], a 3-stage single-channel 12 b ADC reaches 1 GS/s with 168.2 FoMs. Ref. [170] further push the 16 b ADC to 15 MS/s with 176.8 FoMs. A 14 b 100 MS/s[171] and 130 MS/s ADC[172] shows a top FoM_S of 180.2 and 181.5 dB, respectively. A wide tuning sampling range (0–40MS/s) >75 dB ADC maintains an outstanding FoM_S of 179.6 dB in Ref. [173]. All their core architecture is Pipe-SAR and they are marked as Refs. [169–173], respectively, in Fig. 19.

Besides hardcore Pipe-SAR ADCs, other works[164–176] increase the hybridization domain where their performance also shines out in their specification range. While Refs. [174, 175] taking advantage of the outstanding energy efficiency of Pipe-SAR ADC at the large signal swing in the voltage domain, it switches the fine conversion in the time domain to maintain the efficiency at a low supply voltage (half of regular V_{DD}). The 13 b ADC[174] design running at 20 MS/s achieves 182.4 dB FoM_S and the 12 b ADC samples at 260 MS/s with 171.8 dB FoM_S, as marked in Fig. 19. Noise-shaping (NS)

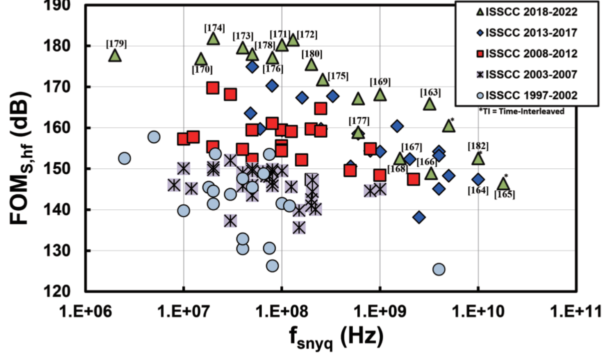


Fig. 18. (Color online) ADC survey with Schreier FoM vs. speed.

technique is also added in Pipe-SAR ADC[176], where a single residue amplifier involves all pipelining, loop filtering and summing operations to save power. This solution provides an additional error shaping on the noise of the 2nd stage quantization, thus potentially leading to a higher resolution or a better energy efficiency. It also extends the NS-SAR-type ADC to tens of Mega-Hertz bandwidth range while keeping outstanding energy efficiency. The ADC obtained a 75.2 dB SNDR and 40 MHz bandwidth with 177.1 dB FoM_S as marked in Fig. 19. Such additional domain of hybridization also can allow a more robust pipelined operation.

It is well known that the inter-stage gain error in the pipelined ADCs is circuital and often calls for power-hungry opamp or calibration. Ref. [177] introduces the incremental delta-sigma ADC in Pipe-SAR and puts the residue amplification stage (gain = 1 in their design) in the 2nd stage SAR feedback loop, removing the gain error by matching it with reference gain. Ref. [178] places the noise-shaping in the first stage of the NS Pipe-SAR ADC, the inter-stage gain error there-

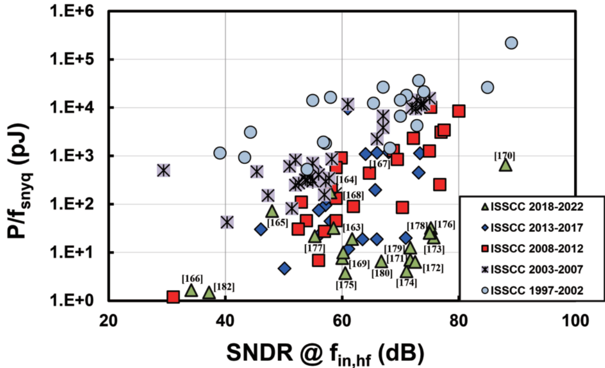


Fig. 19. (Color online) ADC survey with energy vs. SNDR.

fore a 2nd order shaped to the high frequency and eventually filtered by the decimation filter. Furthermore, as the pipeline operation inherently contains stage isolation and signal summation ability, they are also adopted to enable low input capacitance SAR-type ADCs (120 fF in Ref. [179] and 260 fF in Ref. [180] for 13–14 b resolution, respectively).

Last but not least, the pipelined concept itself is now moving from the classical voltage domain to the time domain. This new thought has been mentioned in Ref. [181] and well demonstrated in Ref. [182]. Such time-domain pipelining opens up a new research direction for very-speed single-channel ADC design with great potential, especially in advanced nodes.

5. Power converters

Many new architectures and emerging applications appeared in recent years in the power converters area. This section will summarize the recent hybrid DC–DC converter topologies, which provide higher power density and higher efficiency at large voltage conversion ratios. Then, we discuss the fast transient response issues of both conventional and hybrid DC–DC converters for point-of-load applications. In the second-half of this section, we discuss the challenges of the two emerging applications: isolated power for harsh environments, and supply modulator for 5G PA.

5.1. Hybrid DC–DC converter topologies

With the developments of portable, wearable, and IoT devices, the energy conversion technologies face many new challenges. These applications often require higher power density and efficient space utilization, wider input-output coverages, and the ability to maintain high efficiency over a wide voltage conversion ratio (VCR) range. Actually, there is a compromise among efficiency, power density, and conversion ratio.

Traditional inductive topologies, such as buck and boost converters, can achieve high efficiency with a wide voltage range and a continuous VCR, but require large-size high-quality inductor(s), which leads to low power density. Besides, when the input/output voltage is high, the conduction and switching loss deteriorate. On the other hand, switched-capacitor (SC) converter can achieve high efficiency at a specific VCR only, limited by the charge sharing loss. Even if the adjustable VCR is adopted, the increase of the number of switches will sacrifice power density.

The hybrid architecture converter combines the advantages of inductive and SC topologies. The large inductor can be replaced by a smaller one, while the soft charging of capacitors can alleviate the issue of charge sharing loss. The hybrid architecture provides an effective scheme to realize the favorable trade-off among the efficiency, power density and VCR.

As summarized in Fig. 20, the works on hybrid DC–DC converter architectures can be classified in 5 types, namely flying capacitor multi-level (FCML) topology[183–189], hybrid SC topology[190–193], inductor-first topology[194–198], dual-path topology[198–203], and double step-down (DSD) topology[204–207]. On the other hand, resonant SC converter that uses a resonant inductor to reduce the output impedance is essentially an SC converter, which still suffer from the charge sharing loss, is different from the above categories and will not be discussed here.

5.1.1. Flying capacitor multi-level topology

FCML topologies can reduce the voltage stress on the switches as well as the voltage ripple on the switching node by adding flying capacitor(s) in the buck topology, and can also realize a higher effective switching frequency (Fig. 20 bottom left). Therefore, the inductor current ripple is smaller, and the overall power density can be improved by using a smaller inductor. In recent years, progresses have been made in terms of higher efficiency with larger VCR and cascoded switches, and flying capacitors voltage balancing. For the 4-level FCML topology proposed in Ref. [183], an effective switching frequency of three times of the pulse-width modulation (PWM) frequency is realized, and thus the inductor can be reduced to 10 nH. However, the start-up and capacitor voltage balancing issues deteriorate. Similarly, in the modified fully-integrated 4-level hybrid converter proposed in Ref. [184], by designing the switching state of the flying capacitors, the voltage stress on the capacitor is reduced, and thus saving 75% of the capacitor area. Ref. [185] presents a symmetrical modified multilevel ladder converter, which divides the cascoded switches into 2 channels. The number of switches on the current path in each phase is halved, reducing the conduction loss, while the capacitors can be naturally balanced. In Ref. [186], two 3-level bucks are merged to achieve an efficiency of 85.5% at the VCR of 12.5. Of course, FCML topology can also be applied to boost[187], buck-boost[188] and isolated[189] converters to enjoy its advantage of reducing the device voltage stress.

5.1.2. Hybrid switched-capacitor topology

Hybrid switched-capacitor topology (Fig. 20 middle left) is the deformed structure based on SC topologies, such as Dickson, Fibonacci, series-parallel, ladder, doubler, etc. By adding a power inductor and PWM phase operation, it can realize capacitor soft charging, so as to achieve high efficiency and high power density.

A hybrid SC converter based on Dickson topology is proposed in Ref. [190]. Buffer phases are added to obtain a smooth capacitor current, which achieves high power density and efficiency. But the capacitor balance is still a challenge, and the increase of the number of switches also puts pressure on the gate driver and level shifter designs. The work in Ref. [191] eliminates the need of external bootstrap capacitors, which saves the area and cost. A Fibonacci hybrid topology in Ref. [192] reduces the volume of passive components and lowers the frequency to 78 kHz. A reconfigurable ca-

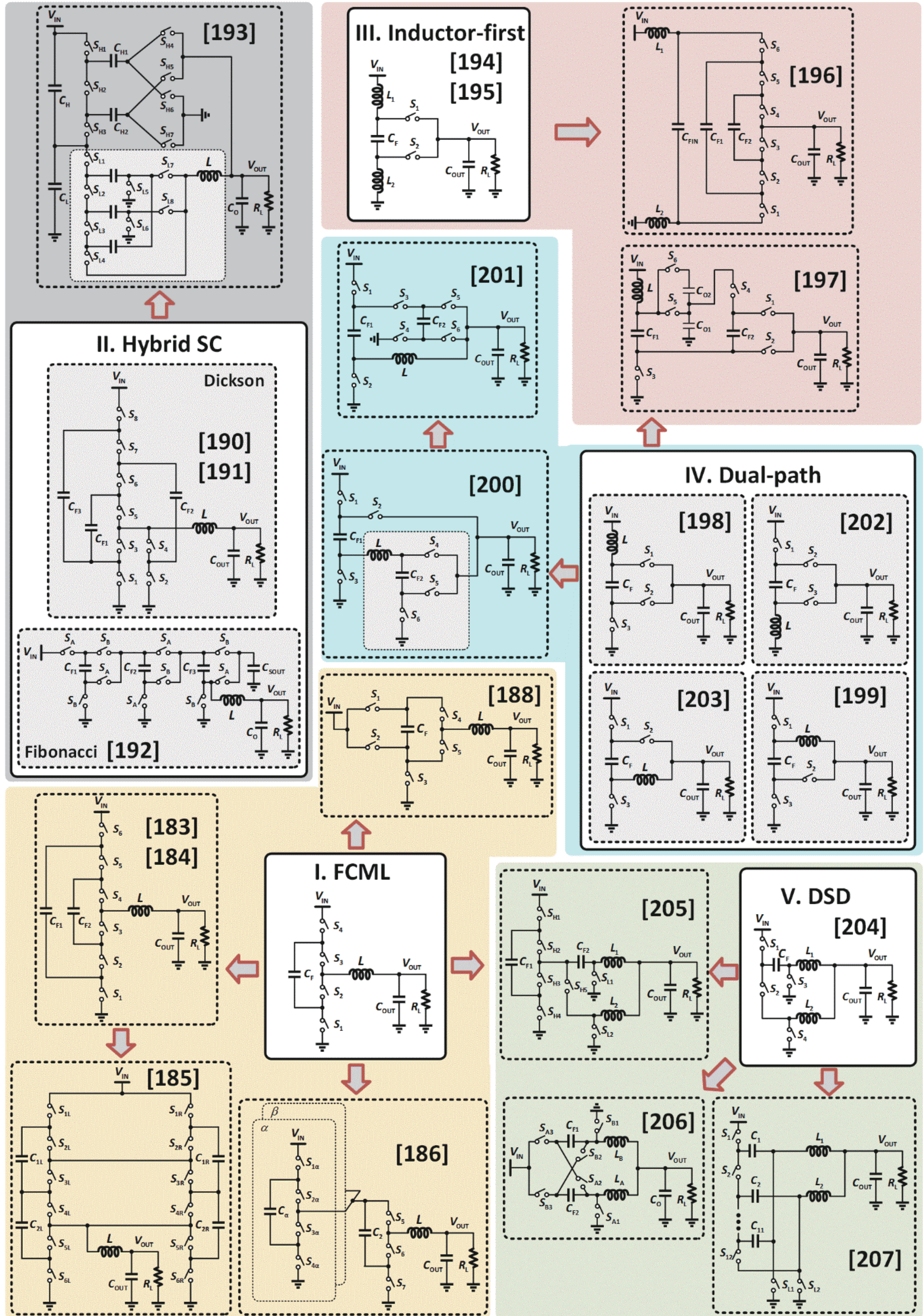


Fig. 20. Overview map of hybrid DC–DC topologies and their relevance.

pacitive-sigma converter is proposed in Ref. [193]. It consists of a 2 : 1 SC high-side and a 2-/4-level hybrid Dickson low-side, and achieves high efficiency over a broad VCR range.

5.1.3. Inductor-first topology

Repositioning the inductor from the output to the input (Fig. 20 top right) is an attractive solution to the conduction

Table 4. Pros and cons of different hybrid DC–DC topologies.

	FCML	Hybrid SC	Inductor-first	Dual-path	DSD
Typical topology					
Pros	Small I_L ripple Wide VCR range	Small I_L ripple Wide VCR range	Small I_L & ripple Continuous I_{IN}	Small I_L & ripple High power density	Small I_L ripple Shared I_L Less components
Cons	Needs C_F balancing Large I_L	Needs C_F balancing Large I_L Many components	Extra L Limited VCR range Negative voltage	Hard charging Limited VCR range	Extra inductor Needs 1 HV device

loss caused by the inductor DCR. With extra flying capacitors maintaining the step-down conversion, the inductor is relocated to the low current path (input path). Meanwhile, the input pulse current is changed into continuous current, which spares the area of the input capacitor.

A passive-stacked 3rd-order buck (PS3B) converter[194] replaces the large inductor in the buck converter with two front small flying inductors. The cancelling of input capacitor helps to realize a high power density of 0.7 W/mm^2. Based on PS3B, a small inductor and two switches are added to enable the recycling of gate charge[195]. This technology improves the light load efficiency and the peak efficiency is as high as 98.2%. Ref. [196] presents a topology combining PS3B with FCML, where a scheme for high input voltage is presented.

A flying inductor hybrid architecture for USB-C charging is proposed in Ref. [197]. The inductor at the input can be provided by the parasitic inductor of USB cable (about 500 nH), as a result, the power density is up to 1.48 W/mm^2. A switching inductor capacitor (SIC) buck topology is realized in Ref. [198] to improve the performance of the fully integrated buck. By arranging fewer resistive elements in series on the current path, the requirement for the inductor is effectively reduced.

5.1.4. Dual-path topology

An additional power path is formed by flying capacitors to share the current pressure on the inductor in the dual-path topologies (Fig. 20 middle right), which can effectively improve the efficiency of the converter under heavy load current. At the same time, similar to the advantages of inductor-first topology, this topology provides a chance to use smaller inductor.

A dual-path buck converter topology is presented in Ref. [199]. The average current and current ripple of the inductor are reduced at the same time, and the loss caused by DCR is reduced. However, the dual path of this topology only exists in specific phase. When VCR and the duty cycle changes, it may lose its advantage. An always-dual-path (ADP) buck converter[200] improves this defect, and keep the inductor current half of the load current. Ref. [201] presents a hybrid SC-parallel-inductor buck to reduce the inductor current without enlarging the current ripple. Four types of dual-path topologies are summarized in Ref. [202], while Ref. [203] complements the last type of dual-path topology other than Refs. [198, 199, 202].

5.1.5. Double step-down topology

Double-step down (DSD) topology (Fig. 20 bottom right) is commonly adopted in the scene from 12/24/48 V to 1 V in the automotive industry and datacenter, which helps to alleviate efficiency degradation at large VCR. The DSD topology mainly takes the advantage of low voltage stress on devices by the flying capacitors clamping voltage, and two inductors connected to the output share the current stress but cause additional cost.

The advantages of DSD topology are analyzed in detail in Ref. [204], and the direct conversion from 48 to 1 V is realized with GaN devices. A tri-state DSD topology merged FCML and DSD structures is realized in Ref. [205], achieving 88.3% efficiency under 24-to-1 conversion ratio. Ref. [206] presents a flying capacitor cross-connected (CCC) buck with an improved the transient performance using a dedicated operation phase. Also, all the switches in Ref. [206] only need to sustain $V_{IN}/2$ voltage stress, considerably reducing the chip area. A 12-level series capacitor DC–DC converter[207] is designed to disperse most of the input voltage stress on the series capacitors, in which only 5 V switches and a single GaN FET are used to realize the conversion from 48 to 1 V.

The comparison of the five different hybrid DC–DC categories is listed in Table 4. The hybrid DC–DC topology is expected to remain popular in the future, and plays a significant role in the field of large VCR power conversion. It helps to reduce the average current and current ripple in the inductor, disperse the voltage stress and achieve soft charging. Thus, it is proven to be a good solution to the system requiring high power density, large VCR, and high efficiency. Meanwhile, complex capacitor balancing, gate drivers, internal voltage domains, and operation phase control make the designs difficult. As the development of hybrid converter is still evolving, we believe that a better categorization can be made in the near future.

5.2. Fast transient DC–DC converters

Besides efficiency and power density, fast transient response is an important property of point-of-load voltage regulator for microprocessors for high-performance computing, which could have a fast load current transient approaching 1 A/ns and would require a dynamic voltage scaling (DVS) speed of 1 V/μs. Low-dropout regulators (LDOs) can provide both fast load transient response and DVS speed, but its efficiency degrades proportionally with the input-output voltage difference. Therefore, the buck DC–DC converter as the 1st-stage of the power delivery system should also have fast transient capability to support the LDOs for higher system effi-

Table 5. Recent fast-transient DC–DC converters.

	[208]	[209]	[210]	[211]	[212]	[213]	[214]	[215]	[206]
Process (nm)	130	180	180	28	350	28	4	180 BCD	180 BCD
Topology	Buck	Buck	Buck	Buck	Buck	Buck	Buck	DSD	CCC
V_{in} (V)	3.3	3.3	3–5	1.2	3.3	1.2	1.8	12/24	12
V_{out} (V)	1.8	1–2.5	0.5–2.5	0.6–1	0.3–2.6	0.45–0.9	1	1	0.9–1.8
f_{sw} (MHz)	30	10	30	75	25	400	50	1	2
Phase number	1	1	4	4	4	6	4	2	2
Inductor/phase (nH)	90	200	100	15	200	1 (bond-wire)	5 (in package)	1800	740
C_{out} (μF)	0.94	2	0.84	0.2	2.47	0.0002	0.8	10	10.6
Control law & transient technique	VM & LDO assist	SH & DAB	VM & OCB	DAOT	SH & AW, APC	VM	VM	VM & delay-insensitive, DP charging	SH & Intrinsic DP charging
Auto phase shedding	n.a.	n.a.	No	Yes	Yes	Yes	Yes	n.a.	n.a.
Compensator optimization	n.a.	n.a.	No	Not necessary	Not necessary	Yes	Yes	n.a.	n.a.
Peak efficiency	90.70%	91%	91%	89%@1 V	88.10%	83.70%	91.50%	88.3%@1 V	86.8%@1.2 V
ΔI_{load} (A)	1.25	1	2	1	4	1	10	3	4
Δt (ns)	2	3	5	10	5	1	10	20	20
ΔV_{out} (V)	0.036	0.031	0.034	0.08	0.1	0.2	0.09	0.056	0.11
Normalized ΔV_{out}	0.742	1.082	1.008	12.800	1.096	n.a.*	2.560	3.833	4.981

*Load current step edge time Δt is too slow that is comparable to its switching cycle.

ciency.

As a large inductance is favorable for reducing the inductor current ripple, the maximum transient response speed of a conventional buck converter is limited by the current slew rate of the power inductor (SR_L). Also, the transient response can be limited by the controller's delay. For the hybrid DC–DC converters discussed in the sub-section above, a smaller inductor can be used for higher efficiency and also higher power density, which should be good for fast transient. However, as the voltage across the power inductor in a hybrid topology is also reduced, the SR_L would be considerably limited by the lower voltage across the inductor. Recent literatures[206, 208–214] tried to address these issues from the power stage and/or the controller's perspectives. Refs. [208, 209] presented fast transient techniques for single-phase conventional buck converter. Meanwhile, Refs. [210–214] proposed the techniques for multiple-phase buck converter, where the SR_L is increased by N times benefiting from the multi-phase characteristics. The transient improvement techniques in Refs. [206, 215] are for hybrid DC–DC topologies, which are used in large conversion ratio applications.

Table 5 lists the key performances of these literatures. We use the performance normalized V_{OUT} undershoot ($\Delta V_{OUT,Norm}$) to fairly compare how fast can these works achieve, under different V_{IN}, V_{OUT}, L, N, output capacitance C_{OUT}, load current step ΔI_{LOAD}, load current step edge time Δt, and even topologies. Here, we define $\Delta V_{OUT,Norm}$ as the ratio of the measured ΔV_{OUT} and its theoretical minimum value $\Delta V_{OUT,MIN}$[210], where $\Delta V_{OUT,MIN}$ is:

$$\Delta V_{OUT,MIN} = \frac{\frac{\Delta I_{LOAD}^2}{SR_L} - \Delta I_{LOAD} \cdot \Delta t}{2C_{OUT}} = \frac{\frac{\Delta I_{LOAD}^2 \cdot L}{(V_{IN} - V_{OUT})N} - \Delta I_{LOAD} \cdot \Delta t}{2C_{OUT}}. \quad (2)$$

The $\Delta V_{OUT,Norm}$ should be larger than one if all the I_{LOAD} during the transient response is provided by inductor current I_L. The smaller $\Delta V_{OUT,Norm}$ indicates a faster controller speed.

Ref. [208] uses the voltage mode (VM) PWM control, with a 30-MHz switching frequency (f_{SW}), 90-nH inductance. The transient response is accelerated by a digital linear regulator, sourcing/draining additional current under a transient event, and hence allowing $\Delta V_{OUT,Norm} < 1$. The error amplifier (EA) output voltage V_{EA} is designed to swing out of the RAMP signal range during transient, turning on the regulator rapidly. In order to not to interrupt the PWM loop, the regulator is turned off slowly. Meanwhile, the large V_{EA} swing during transient enforces a 100% duty cycle (D), in other words a maximum SR_L. An improved type-III compensator extends the bandwidth and reduces the settling time. The $\Delta V_{OUT,Norm}$ is 0.742 as tabulated.

Ref. [209] uses a synchronized hysteretic (SH) control with a double adaptive bound (DAB), working under a 10-MHz f_{SW}, 200-nH inductance. The DAB facilitates a fast transient response under both I_{LOAD} step up and down. A ripple injection scheme is implemented, with an inductor DC resistance offset cancellation for an improved load regulation. Moreover, the controller power consumption is designed to be scalable with the I_{LOAD}, benefiting a high efficiency over a wide power range (80% efficiency over 99.9% of full load range). The measured $\Delta V_{OUT,Norm}$ is 1.082.

Ref. [210] is a 4-phase buck converter with a 30-MHz f_{SW}, 90-nH inductance/phase. VM control is employed at the steady-state, implemented with a conventional type-II compensator that provides the proportional-integral (PI) control. A one-cycle charge balance (OCB) scheme is activated to regulate V_{OUT} within a single switching cycle from the C_{OUT} current detected by a capacitor–current sensor (CCS). This optimizes ΔV_{OUT} close to its theoretical minima. An improved CCS calibration scheme is proposed to provide an accurate C_{OUT} current information under process, bias voltage and temperature (PVT) variations and taking PCB parasitics into ac-

count. The calibration is executed in the background, adding a flexibility for the controller's transient scheduling. As predicted, the measured $\Delta V_{OUT,Norm}$ is 1.008, very close to the ideal value.

Ref. [211] proposes an integrated 4-phase buck converter, with a digital adaptive on-time (DAOT) control for high-speed digital systems. A 75-MHz f_{SW} and 75-nH inductance/phase are employed. To fix the f_{SW} in AOT control, the proposed controller adapts the turn-on time accurately from the V_{IN} and V_{OUT}, using a digital-controlled delay line (DCDL). The turn-on time accuracy should thereby be higher than that in an analog control. Meanwhile, a digital ripple-injection scheme is optimized to mitigate V_{OUT} droop. All the sub-converters share the off-time comparator and DCDL to reduce the I_L imbalance among phases. Additionally, the digital control allows a multi-phase synchronization with a higher accuracy. An automatic phase shedding scheme is used to extend the good efficiency to light load conditions. With a synthesizable digital controller, the achieved $\Delta V_{OUT,Norm}$ is 12.8.

Ref. [212] shows a 4-phase buck converter with 25-MHz f_{SW} and 200-nH inductance/phase. By adding a V_{OUT} transient sensing circuitry, an adaptive hysteretic window (AW) scheme fulfills a fast transient response. The hysteretic control is synchronized for a fixed f_{SW}. The V_{OUT} transient sensing is reused to activate all phases within one cycle, a.k.a. active phase counting (APC), benefitting the transient response significantly. The APC also ensures a high efficiency over a wide power range. The measured $\Delta V_{OUT,Norm}$ is 1.096.

Ref. [213] presents a 6-phase buck converter with 400-MHz f_{SW} and 1-nH inductance/phase. The small inductors are implemented with bonding wires. Then the output stage complex pole pair is located at a high frequency, allowing a VM control with a type-I compensator. A flying capacitor (C_F)-based I_L balancing scheme is proposed, removing the high-speed I_L sensors in conventional designs. In addition, fine-grained phase shedding, allowing any phase count from 1 to 6, is achieved with the proposed delay locked loop (DLL). This further extends the high-efficiency I_{LOAD} range. Finally, the C_{OUT} is re-allocated as C_F, and the compensation capacitance is adjusted, both in proportional to the shedded phase count. This allows a faster response under the phase shedding operation. As the load current step edge time Δt is too slow that is comparable to its clock cycle, the $\Delta V_{OUT,MIN}$ indicator is not applicable to this work.

Ref. [214] presents a 4-phase buck converter for a fully-integrated voltage regulator in compute platform power delivering. It operates at 50-MHz f_{SW}, with 5-nH inductance/phase. The converter is implemented with a 4-nm class CMOS process, together with in-package magnetic inductors. It achieves a highest current density of 47 A/mm^2. By monitoring the current and asynchronous events, the phase count is decided as an automatic phase shedding. The converter uses a type-III compensator, where the RC components are automatically tuned to ensure the stability under different phase count. The automatic phase shedding almost tracks the optimal efficiency. Hard switching is used at 4 phases for a better efficiency at heavy load, while the controller transits to soft switching at other phase counts. The measured $\Delta V_{OUT,Norm}$ is 2.56.

Refs. [215, 206] are hybrid converters based on double step down (DSD) topology, which has a two-phase operation. The C_F is used to halve the voltage swing on the switching nodes (V_X), and hence allows low-voltage rating low-side power switches for a better efficiency. The C_F is soft charged/discharged by the two inductor currents, enforcing I_L balancing automatically. However, this topology under a conventional control does not favor for a fast transient response for two reasons. First, the halved V_X swing also reduces the single-phase SR_L to $(V_{IN}/2-V_{OUT})/L$, compared to a conventional buck converter. Secondly, with a conventional control, only single-phase charging is allowed at transient, otherwise the low-side switches will be overstressed.

Therefore, Ref. [215] adds auxiliary power switches to facilitate a dual-phase charging, doubling the SR_L compared to the conventional control. Furthermore, Ref. [215] uses VM control with a delay-insensitive technique. This allows the controller to response the transient event without waiting for the next system clock. The achieved $\Delta V_{OUT,Norm}$ is 3.83. Here, $\Delta V_{OUT,Norm}$ is defined as the ratio of measured ΔV_{OUT} and $\Delta V_{OUT,MIN}$ defined in Eq. (2), facilitating the comparison among different topologies.

Ref. [206] achieves dual-phase charging based on the symmetric DSD, or C_F-cross-connected (CCC) topology[216]. CCC divides the C_F and one power switches in the DSD converter[217] into two, resulting in more control states than the DSD without degrading the power density and efficiency. An intrinsic dual-phase charging can be achieved through combining some of the states, without adding any auxiliary switch. A synchronized hysteretic control is used to activate dual-phase charging quickly when load transient occurs. In addition, a shared bootstrap capacitor scheme is proposed to reduce the silicon area and switching loss. The $\Delta V_{OUT,Norm}$ is 4.981.

As a brief summary, recent fast-transient buck converters used small inductors (down to several nH), to increase the SR_L. Therefore, they used several tens of MHz f_{SW} to reduce the inductor current ripple and prevents the inductors from saturation. Multiple-phase buck converters require auto phase shedding to extend high efficiency to a wider power range. Subsequently, the VM-based multiple-phase converters need to optimize compensator according to the phase count activated. For the hybrid converters, they may have inherently inferior SR_L. The study for their fast transient performance should be a future hotspot.

5.3. Isolated DC–DC converter

Galvanic isolation separates the input and output supplies of a system to allow power and data delivering through an isolation barrier instead of electrical connections. Unlike a non-isolated DC–DC converter that has only one ground, isolated DC–DC converter can avoid the surge and ground shifting problems by adding this isolation between two voltage sides. So isolated DC–DC converter plays a key role in guaranteeing system safety and reliability in harsh industrial environments (e.g. electrical vehicle, communication systems, medical devices, etc.). Some examples include preventing electrical shock to human operators, protecting expensive devices from risk of damage in a high voltage side, and breaking ground loop. In Fig. 21, the isolated DC–DC converters commonly consist of three parts: a transmitter (TX), an isolation barrier, and a receiver (RX). To transfer power across the isolation barrier, an inverter for DC–AC conversion, a rectifier for AC–DC conversion, and an isolated feedback control for load regulation are implemented in the TX and the RX, respect-

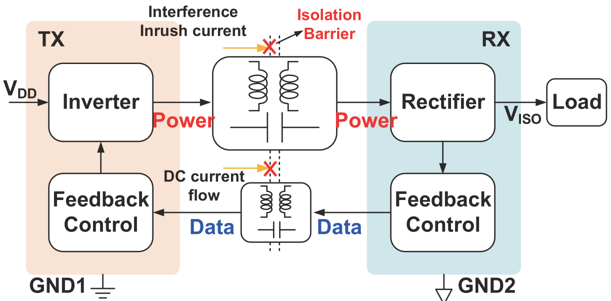


Fig. 21. (Color online) Block diagram of an isolated DC–DC converter.

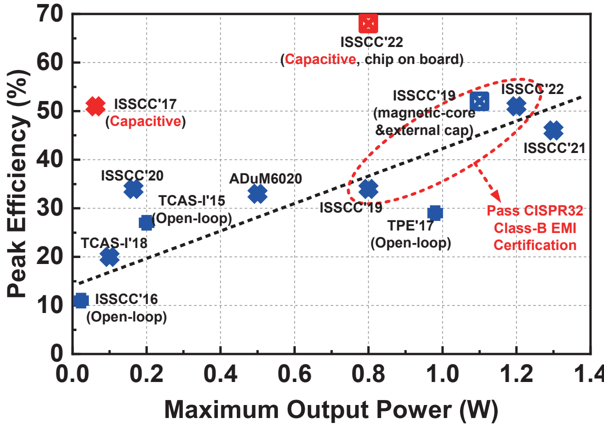


Fig. 22. (Color online) Peak efficiency, maximum output power and EMI performance comparison for the reported isolated DC–DC converters.

ively. However, delivering hundreds of mW power under low-EMI emissions across an isolation barrier presents several challenges regarding the cost, efficiency, power density, and EMI performance. Fig. 22 compares the efficiency, power capacity, and EMI performances of the prior-art isolated DC–DC converters[218–229].

5.3.1. Efficiency and power density of isolated DC–DC

To keep improving the efficiency and power density of isolated DC–DC converters, some state-of-the-art efforts have been devoted to meet these challenges recently. Power delivering with isolation barrier can be implemented through capacitive coupling or a transformer. Due to the output power is proportional to isolation capacitance, and its inversely proportional to thickness of dielectric, and thus high-isolation-rate capacitors limit the power capacity[218, 219]. For example, an isolated DC–DC converter using on-chip capacitors and an off-chip inductor is presented in Ref. [218], but it only transfers a maximum output power of 62 mW with <1 kV isolation rating that is limited by the on-chip capacitors. A capacitive isolated DC–DC converter proposed in Ref. [219] achieves a significant efficiency improvement to 68.3% and reconfigurability of single- and dual-phase operations with 1TX-1RX and 1TX-2RX for a power capacity extending from 0.4 to 0.8 W. However, ceramic SMD capacitors with PCB coils takes up a large size of the converter that is difficult to achieve a miniaturized package, and the dielectric insulation strength is 1 kV only.

In order to increase both the output power and the isolation rating, isolated DC–DC converters using micro-transformers have been reported[220–228]. Some open-loop converters with an on-chip transformer and an LC tank oscillator operate over 160 MHz while the measured efficiency is less than 30%[220, 222]. Soon after, 6-μm-thick gold winding for both the primary and the second coils, with 20-μm polyimide between them to provide >5 kV isolation rating, are implemented in Ref. [223] and an AC-coupled LC tank oscillator with the transformer resonates at 180 MHz, transferring a maximum output power of 0.8 W. But the peak efficiency of the converter is lower than 34% because Q of the micro-transformer is only 6.8 at 200 MHz. A high-performance integrated transformer with a magnetic-core achieving a Q of 15.8 and an inductance of 130 nH is demonstrated in Ref. [224] to achieve a peak efficiency of 52% and a maximum power capacity of 1.1 W. However, the fabrication process of the magnetic-core transformer is complex and the cost is high. In Ref. [225], a coreless micro-transformer is formed by using 100-μm-thick winding with silicon-embedded, and large inductances with a high-Q of 15.7 for primary coil are achieved to allow the converter switching at 11 MHz. However, the efficiency of transformer is still limited by secondary coil and the fly-back power converter produces large resonant currents that flow into the coils, and thus degrading the efficiency to 34% with only 165 mW output power.

In addition, these isolated converters are assembled in a small-outline integrated-circuit (SOIC) package with size of 6 × 10 mm^2[220] and 10 × 18 mm^2[221] that measure a maximum power density of 13.33 and 6.11 mW/mm^2 only, respectively. A transformer-in-package solution for galvanic isolated DC–DC converter by using fan-out wafer-level packaging (FOWLP) is presented in Ref. [226] to achieve a maximum output power of 1.25 W in a 5 × 5 mm^2 package (maximum power density of 50 mW/mm^2) and a peak efficiency of 46.5%. Although the power density is significant enhanced, this small form factor of the converter will limit the distance between pin and pin in different voltage side that causes a low isolation voltage by air-creepage and bring heat dissipation issue. An isolated DC–DC converter with a high-Q substrate-based transformer in a land grid array (LGA) package is presented in Ref. [227] recently, the converter reaches a peak efficiency of 51% at 0.4 W output power and maximum power capacity of 1.2 W in a 10 × 12 mm^2 package (maximum power density of 10 mW/mm^2), while due to the thickness of insulation material in the substrate process is limited to 100 μm, the coupling coefficient of the substrate-based transformer will be restricted.

5.3.2. EMI emission of isolated DC–DC

Along with isolated DC–DC converters scaling, those converters above switch currents of several hundred mA at frequencies more than tens of MHz, and thus operation at these high frequency raises concerns about EMI radiated emissions. Some converters use the LC tank oscillator adopted in Ref. [223, 226] or the leakage-inductance-resonant fly-back topology proposed in Ref. [225], the common-mode voltage of primary coil V_{CM_PRI} suffers from large and quick fluctuations so as to a high radiation is caused by large common-mode current I_{CM} across the isolation barrier. To pass the EN55032/CISPR32 Class-B EMI radiation standard, a multi-layer (4-layer or 6-layer) PCB with a stitching capacitor implemented by the internal layers is taken to provide a low impedance path between two ground or power plane to reduce dipole radi-

ation[228], which will greatly increase the system cost and the effort of PCB layout.

Recently, low-cost circuit techniques to reduce EMI at the source are demonstrated in Refs. [223, 224, 227]. For example, frequency hopping technique can be employed to suppress I_{CM}[223], the converter meets the CISPR22 Class-B standard with a 6.4 dB margin at 500 mW output power on a two-layers PCB without any stitching capacitor, but it will greatly increase the circuit complexity. Besides, the frequency hopping circuit cannot operate in full PWM duty cycle, and thus difficult to meet the standard under heavy load. In Ref. [224], an LLCC topology with a multistage pre-driver is proposed to form a more symmetrical structure to reduce I_{CM}, passing CISPR22 Class-B limits with 5.8 dB margin at output power of 0.75 W. Unfortunately, a costly magnetic-core transformer and two extra external capacitors are needed. In Ref. [227], a symmetric Class-D oscillator with shoot-through-free technique is used for DC–AC inverter in TX chip to suppress I_{CM} efficiently and to avoid shoot-through currents, it can pass the CISPR32 Class-B certification on a two-layer PCB without using any stitching capacitors when output power of 0.5 W with 1.93 dB margin in the vertical field and 2.27 dB margin in the horizontal field, respectively. But the power stage topology is difficult to achieve fully symmetry during packaged by bonding wires, resulting in difficult to pass the Class-B limits under heavy load (output power >0.5 W).

In summary, the capacitive isolated DC–DC converters offer remarkable conversion efficiency, while extra devices needed and low-breakdown-voltage capacitive isolation limit the overall package from being further minimized and working in high isolation rating scenarios. The peak efficiency and power density of transformer-based isolated DC–DC converters are constantly refreshed. However, the efficiency in light load condition and EMI performance in heavy load condition are still the main challenges.

5.4. Supply modulators for PA

The 5G mobile communication enables up to 100/200 MHz signal bandwidth, which is much faster than 4G long-term-evolution (LTE) communication, however, features a higher peak-to-average power ratio (PAPR) around 10 dB, which significantly reduces the radio-frequency (RF) power amplifiers (PA) efficiency to below 10%. To solve this critical problem, envelope tracking (ET) supply modulator (SM) is the key. The requirements on the ETSM for 5G are extremely challenging, including above several hundred MHz bandwidth, 0.5 to 6 V dynamic output voltage range, a couple of Watts instantaneous output power, and higher than 80% efficiency.

Most supply modulators adopt a hybrid topology composed of a wide-bandwidth low-efficiency linear amplifier in charge of high frequency power and a high-efficiency switching converter taking over low frequency power as shown in Fig. 23. For 5G communication, the linear amplifier is required to provide up to 5 V output with above several hundred MHz unity gain frequency (UGF). To fulfill the bandwidth requirement, the critical signal paths are implemented with core devices with small parasitic capacitances. At the same time, I/O devices are stacked to handle the high voltage and protect the core devices[229]. All the poles except the output pole are pushed to frequencies higher than the UGF without compensation. A voltage buffer, which has low input capacitance and low output resistance, is inserted at the gate of the power transistors to push pole at the gate to frequency higher than UGF[230]. Then a miller compensation can be adopted to stabilize the loop. With this method, the achieved bandwidth is above 100 MHz but the voltage buffer consumes extra currents. However, in terms of efficiency, one of the targets of supply modulator designs is always to reduce the power consumption.

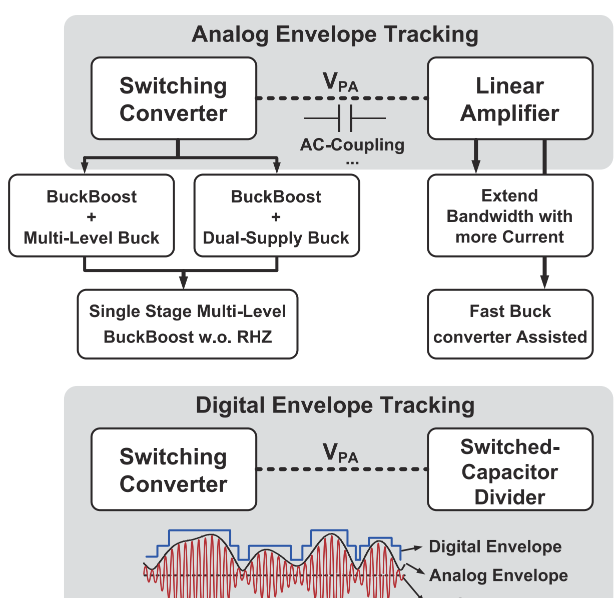


Fig. 23. Design directions of supply modulators.

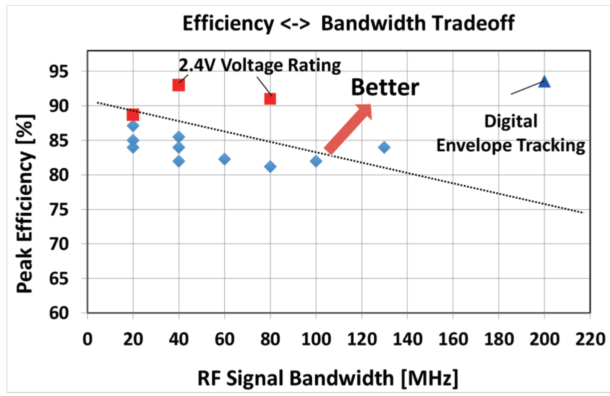


Fig. 24. (Color online) Comparison of state-of-the-art supply modulators showing efficiency versus bandwidth.

On the topology level, to improve the linear amplifier efficiency, an AC capacitor at its output is added to isolate its DC current and reduce its supply voltage[229–235]. The comparison of state-of-the-art supply modulator works showing efficiency versus bandwidth are illustrated in Fig. 24. There is a clear trend that the efficiency drops at higher bandwidth since more power will come from the linear amplifier, which has much worse efficiency than switching converters. As for 5G, the signal bandwidth is larger and the power of V_{PA} is distributed over 100 MHz. To alleviate the problem, Samsung[230] proposed a hybrid topology of a fast buck, a slow buck and a linear amplifier. In terms of the mid-to-high frequency power, it is provided by the fast buck converter rather than the linear amplifier to improve the overall efficiency. Both the feed-forward envelope signal and the linear amplifier current are used in the controller of the fast buck con-

verter to make sure that the power between the fast buck and the linear amplifier is appropriately divided. As a result, this topology achieved a better tradeoff between efficiency and bandwidth. This supply modulator achieves 84% maximum efficiency over 1.2 W output power for LTE-40M and 82% efficiency over 1.3 W output power for NR-100M as annotated in Fig. 24[230]. Those points are on or above the boundary, showing the effectiveness of the proposed topology. The supply modulator enables a NR-100M ET-PA save 400 mW compared with an APT-PA[230].

As for switching converters, they are required to have high-efficiency, fast transient response and high voltage rating. Most of the supply modulators are designed to be directly connected to a lithium-ion battery, of which the voltage can range from 2.5 to 4.2 V with a typical value at 3.7 V. However, the output of the supply modulator can range from 0.5 to 6 V for 5G applications. So both step-up and step-down functions are required for the supply modulator. A buck-boost (BB) converter is usually designed in the SM to generate a stable and high voltage V_{BB}[229, 231]. A traditional buck-boost converter has slow response due to the right-half-plane (RHP) zero, so a buck converter is cascaded after that. To implement the buck converter, we could see two trends from latest arts, which are multi-level and dual supply implementations.

To support high voltage with good efficiency, low-voltage devices in advanced technologies such as 65 nm can be stacked to replace thick-oxide devices e.g. LDMOS or I/O devices with smaller switching loss[232–235]. With a 3-level power stage, the switching node swinging is $\frac{1}{2}V_{DD}$ instead of V_{DD} of a 2-level buck converter at equivalently doubled frequency, thus reducing the inductor current ripple to 1/8, which can reduce the conduction loss with smaller root-mean-square current. Or, on other hand, smaller power inductor can be used to improve large-signal response or power density. Thanks to those advantages, the supply modulator in Refs. [232, 233] achieves 93% efficiency for LTE-40M and 91% efficiency for LTE-80M both at 1 W Pout. The supply modulator in Refs. [234, 235] achieves 88.7% efficiency at 0.7 W P_{out} for LTE-20M. Those efficiencies are high and above the boundary line, but also note that they have low voltage rating with output lower than 2.5 V. Multi-level converters also have their own concerns. For example, the voltage of C_{FLY} could deviate from $\frac{1}{2}V_{DD}$ and a calibration loop is required. The system complexity is also increased, as multiple floating domains for each stacked power transistor must be carefully designed to ensure reliability, especially during startup or transients.

The second trend is to design a dual-power-line (DPL) buck converter proposed in Refs. [229, 231]. When V_{PA} is lower than V_{BAT}, the DPL buck switches between V_{BAT} and ground like a typical buck converter. When V_{PA} is higher than V_{BAT}, it switches between V_{BB} and V_{BAT} (return to battery, R2B) instead of ground (return to ground, R2G). R2B has better efficiency and less noise compared to R2G. The work in Ref. [229] is measured to have 87.1% peak efficiency at 3 W output power for LTE-20M and 81.2% at 3.25 W P_{out} for LTE-80 M. The supply modulator in Ref. [231] reaches 84% peak efficiency for LTE-20M at 1.8 W output power and 82% for LTE-40M at 0.8 W P_{out} with low output noises. One thing to be careful is that the PMOS in the V_{BAT} branch needs a body switch, which should be fast and in synchronous with the gate driving signal to handle the dead time current.

Both of multi-level and DPL buck have improved the performance. However, when cascaded with a buck-boost converter, the overall structure has lower efficiency and higher cost and volume, compared with a single-stage converter. To solve those problems while still being able to provide both step-up and step-down voltages, a novel buck-boost converter, which is single stage and does not have RHZ, is proposed in Ref. [236]. With the help of a flying capacitor, the available voltage levels at the switching node are GND, V_{BAT} and $2V_{BAT}$. Thus it is able to generate a higher-than-V_{BAT} voltage and at the same time has similar transient response of a traditional buck converter. Moreover, the 3-level topology can reduce the voltage stress of the power transistor to V_{BAT} rather than $2V_{BAT}$ or V_{BB}. In later art[237], the novel BB is directly used as the switching converter and a micro-BB only supplies the linear amplifier with much smaller current ratings.

As the bandwidth of 5G increases to 200, 300 and even 320 MHz, traditional analog envelope tracking (AET) encounters an almost impossible challenge to achieve such a wide bandwidth with around 5 V voltage rating and a few hundred pF output capacitor. Moreover, the efficiency predicted by the boundary is lower than 75% for 200 MHz. In ISSCC 2022, a new concept — digital envelope tracking (DET) is proposed by Samsung[238], in which multiple voltage levels instead of the actual envelope are generated by the supply modulator as illustrated in Fig. 23. This DET supply modulator is composed of the fast-transient buck-boost converter mentioned in last paragraph and a switched-capacitor voltage divider (SCVD). The dynamic output voltage is produced by connecting one of the multiple voltages from the SCVD. The SCVD has higher efficiency than the linear amplifier while does not have the bandwidth requirement thanks to DET scheme. Moreover, this DET supply modulator is not sensitive to distance to the PA and the RF-envelope delay, which are critical for AET scheme. The peak efficiency is 93.6% with NR 200 MHz, higher than other state-of-the-art works which target for lower bandwidth. However, the PA will have lower efficiency with DET compared with AET while this paper does not show the overall efficiency including the PA. Moreover, the digital levels are generated from Modem, which causes some overheads. It is also an open question on how to generate the optimal digital levels.

In summary, the design of supply modulators for future communications is difficult and challenging but on the other hand it also opens new opportunities and provides new possibilities.

6. CMOS image sensors and range sensors

The development of CMOS image sensors is in the trends of better performance and diverse functions, including high speed, high dynamic range, 3D imaging and many other aspects. The high speed dynamic vision sensor mimics the biological visual perception mechanism, which converts light intensity information into visual pulse data to quantify high-speed scenes with a low amount of data. High dynamic range image sensor, which improves the detection ability under high light intensity and low light intensity simultaneously. Also, we will discuss the state-of-the-art time-of-flight (ToF) range sensors for distance detection, including direct ToF sensors

Fig. 25. (a) DVS Pixel circuit diagram[239]. (b) Pixel-triggered event process.

and indirect ToF sensors, which have the features of low cost, small size and low power consumption.

6.1. High speed dynamic vision sensors

Active pixel sensor (APS) quantifies dynamic scenes as a series of images. It enables high frame rate recording with high power consumption. Compared to APS, biological vision system has superior image information perception and processing capabilities. Inspired by its imaging characteristics, researchers proposed the architecture of dynamic vision sensor (DVS), which abandons the concept of frame, to greatly improve the temporal resolution of quantified light intensity. The schematic diagram of DVS pixel is shown in Fig. 25(a)[239].

The photoreceptor logarithmically converts the input photocurrent to the output voltage. Then, the amplifier amplifies the variation of voltage. Finally, the comparator detects the voltage change and triggers an event pulse when it exceeds the threshold voltage. In other words, the intensity change detector circuit encodes the light intensity changes over time into pulse events of different polarities, as shown in Fig. 25(b).

Delbruck's group proposed the classic DVS architecture[239], which outputs only changing pixel information and quantizes dynamic scenes into event streams with microsecond precision. DVS can realize low time delay and large dynamic range, which means that the DVS can operate under high-speed scenes and challenging lighting conditions. The development trend of DVS is to reduce the pixel size, increase the event rate, and improve the imaging quality with a small pixel size.

Ref. [240] proposed a threshold subtraction method to replace the reset method and used a programmable capacitive-coupled amplifier as a pre-amplification stage. The proposed method improves the signal integrity while improving the temporal contrast sensitivity to 1%. In Ref. [241], the row sampling circuit is adopted to group adjacent pixels and processed event data in parallel, greatly improving the event readout speed. The event output data rate is up to 300 Meps. The pixel size is reduced to 9 μm using the backside illumination (BSI) and gain boosting technology. In Ref. [242], the pixel circuit is implemented in a two-layer wafer using Cu–Cu connection, which achieved a pixel size of 4.95 μm. The minimum chip power consumption 32 mW and the maximum event rate is 1.3 Geps. A gate induced drain leakage (GIDL) scheme is used to suppress periodic noise events. A global event preservation function is employed to minimize motion artifacts. In Ref. [243], the new stacked event vision sensor uses Cu–Cu connection process to achieve the pixel size of 4.86 μm. The sensor implements event data compression technology, increasing the event rate to 1.066 Geps.

Researchers have also made improvements to the quality of sensor output event data. As DVS pixel size shrinks, it becomes more susceptible to noise triggering noise events. In Ref. [244], the proposed dynamic vision image sensor suppresses pixel noise. Since the background noise is random and has no correlation in the temporal and spatial neighborhoods, the proposed method utilizes the spatiotemporal correlation of valid events to filter out random background noise. In Ref. [245], the DVS architecture implements spatiotemporal redundant compression of event data. It is implemented by redundant compression circuits embedded in the centers of several neighboring DVS pixels.

However, DVS discards absolute light intensity information which is useful for many computer vision algorithms. Recently, three pioneering works address the need for high-speed object detection and tracking using dynamic event information and object recognition classification using intensity information[246–248]. This will make event sensors more widely used in the field of high-speed sensing. In Ref. [246], the dynamic and active pixel vision sensor (DAVIS) integrates APS and DVS at the pixel level, which shares a photodiode. It can output synchronous static background grayscale information and asynchronous dynamic event information. In Ref. [247], the CeleX architecture directly uses the logarithmic photodetector output voltage as its light intensity information. When a pixel is selected, this voltage can be read out by the source follower, thereby quantifying the light intensity. In Ref. [248], the asynchronous time-based image sensor (ATIS) fuses temporal contrast detection and luminance measurement. The DVS pixel structure only responds to changing pixels and triggering events. The PWM pixel structure quantifies the varying light intensity information.

Bionic visual perception combines optoelectronic perception with neuromorphic computing. It achieves high-speed sensing while the pixel structure is complex. The evolution of the event sensor process is shown in Fig. 26. Compared to front-side illumination (FSI), backside illumination (BSI) has become another standard image sensor technology due to its superior quantum efficiency and fill factor[249]. In event sensors, the BSI process can greatly increase the fill factor of complex pixels. With the development of the three-dimensional stacking process, Researchers adopt the stacking process of Cu-Cu connection to achieve small pixel size[242, 243].

With the advancement of process technology and in-depth research, the pixel size of the event sensor is continuously reduced and the event rate is continuously increased, en-

Fig. 26. (Color online) The evolution of the event sensor process.

abling faster event transmission at higher spatial resolution, as shown in Fig. 27. The performance of state-of-the-art event sensors is summarized in Table 6. Event sensors are developing in the direction of further realizing large-array high-speed sensing and deepening the integration of sensing and computing.

6.2. High dynamic range image sensors

In the IoT era, new vision applications in scientific, security, automotive, and computer vision areas, need to work in real-time under indoor/outdoor, daytime/nighttime, all kinds of scenarios. To achieve this, high dynamic range (HDR) sensors, which has excellent imaging performance under both high and low illumination environments, is required. Dynamic range (DR) is defined as the ratio of the maximum non-saturated incident light intensity to the minimum detectable optical power, and typically, it can be calculated by the full well capacity (FWC) of pixels divided by the noise signal under dark conditions:

$$\mathrm{DR} = 20\lg\left(\frac{\mathrm{FWC}(e^-)}{\mathrm{noise}(e^-)}\right). \quad (3)$$

Therefore, to implement a HDR sensor, various methods to increase full well capacity and to reduce readout noise have been proposed, as shown in Fig. 28.

6.2.1. Multi-gain response HDR sensor

The dynamic range of image sensor can be improved by implementing multiple conversion gain (CG) of the pixel, as high gain can provide low noise and high sensitivity, while low gain benefits to larger full well capacity. However, the simplest multiple gain design for the image sensor cannot realize HDR imaging in a single exposure time, and thus they need a complicated post-processing. Therefore, the researchers with new technologies still intend to achieve HDR within a single exposure time, or by finishing the HDR data processing on chip.

Ref. [250] proposed a 64 Megapixels CMOS image sensor with 12 ke$^-$ FWC and low readout noise by dual conversion gain (DCG). A stacked voltage mode (VM) GS CIS with lateral overflow integration capacitor (LOFIC) technology was reported in Ref. [251]. Benefiting from the development of 3D stack technology, the control signals of the pixel array can be implemented more flexibly, which will allow the exposure time of different pixels being different. In Ref. [252], a back-illuminated stacked CMOS image sensor with adaptive dynamic range based on the coded-exposure pixel array was proposed. The pixel array, arranged on the top chip of the 3D stacked structure, were divided into several exposure blocks.

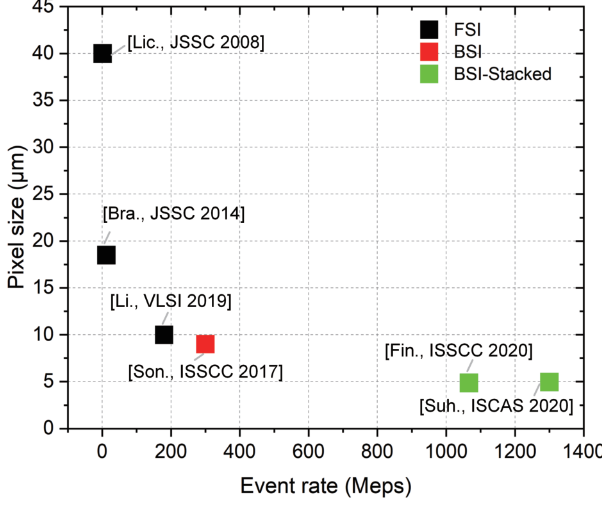


Fig. 27. (Color online) Pixel size and event rate of the event sensors.

And the pixel driver signals were provided from the bottom chip of the 3D stacked structure. An HDR of 134 dB can be achieved because the exposure time of every exposure block can be adjusted independently according to the illumination. In Ref. [253], a 132 dB image sensor was proposed, using two different size photodiodes in each pixel for different sensitivities.

In addition to combining limited linear responses, many scholars are also engaged in the research of nonlinear photoresponse image sensors, which can be considered as a combination of numerous linear responses. Ref. [254] proposed a HDR CMOS image sensor providing an instantaneous dynamic range of >120 dB and a maximum signal-to-noise ratio of ~56 dB. The image sensor offers the high performance required for real-time surgical application. 3T architecture used in digital pixel also works with nonlinear response principle, such as the event image sensors[255]. Wide DR (>124 dB) is achieved due to good low-light performance and the absence of leakage activity from parasitic photocurrents at high light.

6.2.2. Low-noise HDR sensor

Low-noise design of image sensors is critical for HDR because the noise level decided the minimum detectable light intensity. The correlated multiple sampling technique (CMS) and high CG are useful to suppress the sensor's noise. The CMS, of which the sample of the pixel readout signal is operated more than one time, is an effective method to suppress the random noise caused by the transistors in pixel, especially the source follower. However, the repeated sample process will occupy a large amount of readout time. High conver-

Table 6. Performance summary of state-of-the-art event sensors.

Supplier	InIVation				Prophesee		Samsung		CelePixel
Journal, Year, Ref	JSSC, 2008, [239]	JSSC, 2014, [246]	JSSC, 2015, [240]	VLSI, 2019, [244]	JSSC, 2011, [247]	ISSCC, 2020, [242]	ISSCC, 2017, [241]	ISCAS, 2020, [243]	CVPR, 2019, [248]
Resolution (pixel)	128 × 128	240 × 180	60 × 30	132 × 104	304 × 240	1280 × 720	640 × 480	1280 × 960	1280 × 800
Latency (μs)	12	12	N/A	N/A	3	20–150	65–410	150	N/A
DR (dB)	120	120	130	N/A	143	>124	90	100	N/A
Sensitivity (%)	17	11	1	N/A	13	11	9	20	N/A
Power (mW)	23	5–14	0.72	4.9	50–175	32–84	27–50	130	400
Chip size (mm^2)	6.3 × 6	5 × 5	3.2 × 1.6	2 × 2	9.9 × 8.2	6.22 × 3.5	8 × 5.8	8.4 × 7.6	2 × 2
Pixel size (μm^2)	40 × 40	18.5 × 18.5	31.2 × 31.2	10 × 10	30 × 30	4.86 × 4.86	9 × 9	4.95 × 4.95	9.8 × 9.8
Fill factor (%)	8.1	22	10.3	20	20	>77	11	22	N/A
Max event rate (Meps)	1	12	N/A	180	N/A	1066	300	1300	N/A
Stationary noise (ev/pix/s)	0.05	0.1	N/A	N/A	–	0.1	0.03	N/A	N/A
Technology (nm)	350 FSI	180 FSI	180 FSI	65 FSI	180 FSI	90 BSI-stacked	90 BSI	65 BSI-stacked	65 FSI
Grayscale output	no	yes	no	no	yes	no	no	no	yes
Grayscale DR (dB)	N/A	55	N/A	N/A	130	N/A	N/A	N/A	N/A
Max. frame rate (fps)	N/A	35	N/A	N/A	N/A	N/A	N/A	N/A	N/A

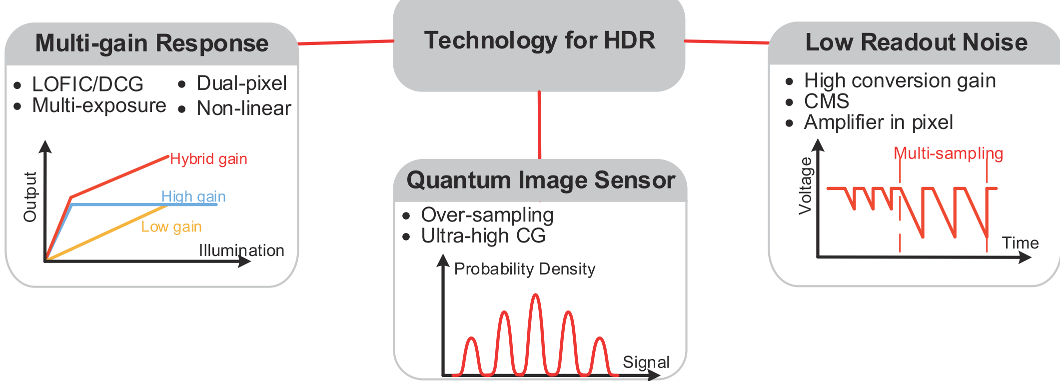


Fig. 28. (Color online) Summary of high dynamic range techniques.

sion gain, or amplifying the floating diffusion (FD) voltage in pixel is a direct way to suppress the noise in the readout circuits. But they need additional transistors and thus difficult to apply in a small-pitch pixel.

For reducing the readout noise, Ref. [256] introduces a 5-transistors (5T) pixels enabling the combination of deep sub-electron noise performance by reducing the sense node capacitance. Ref. [257] released a 1.45 μm pitch pixel image sensor. An amplifier structure is used in the sensor pixel to achieve a conversion gain of 560 μV/e$^-$, reducing the noise to 0.5 e^-_{rms}. To reduce the time of CMS, Ref. [258] proposed a conditional CMS method that achieved 0.66 e^-_{rms} random noise with 5-time sampling at a frame rate of 7.2 frames/s, which corresponds to a sampling-rate frequency of 36.1 kHz for the column parallel ADC.

6.2.3. Quanta image sensor

In recent years, there are many new structures and operation processes of image sensor proposed to achieve HDR, such as quanta image sensor (QIS). A typical QIS integrates up to a few photoelectrons per pixel in one frame. Spatial and temporal oversampling are implemented to achieve a high dynamic range and a high frame rate that are comparable to the ideal CIS operating mode. Ref. [259] proposed a 4 M pixel, 3D-stacked backside illuminated QIS, which realized a readout noise of 0.3 e^-_{rms} and a single-exposure dynamic range of 100 dB.

The performance of state-of-the-art HDR sensors is summarized in Table 7. The DR can be over 100 dB by applying new structures of image sensor, or combining the multiple HDR technique. In the future, for typical image sensor, the LOFIC which is known to have a potential of achieving higher DR than the dual CG pixel, would be the dominant technique in the next generation. And, we expect that novel image sensors may improve the DR more drastically.

6.3. Range sensors

Range sensors have shown growing demand in many applications, such as autonomous driving, augmented reality, robotics, and smart homes. Time-of-flight (ToF) sensor, which can be realized in CMOS process, is one of the range sensors with the features of low cost, small size, and low power consumption. There are two types of ToF sensors according to the depth measurement principles: direct ToF (D-ToF) sensor and indirect ToF (I-ToF) sensor. Fig. 29 shows the principles of the ToF sensor system. The modulated or pulsed light is emitted from the light source and the fight time is measured from the reflected light of the target to extract the depth in-

Table 7. Performance summary of the state-of-the-art HDR sensors.

	IEDM, 2019, [250]	IISW, 2020, [251]	ISCAS, 2020, [254]	ISSCC, 2020, [255]	EDL, 2020, [256]	JSSC, 2018, [258]	VLSI, 2021, [259]
Sensor type	Multi-gain response	Multi-gain response	Non-linear response	Non-linear response	Low-noise	Low-noise	QIS
Process	N/A	45 nm CIS/65 nm logic	350 nm CIS	90 nm CIS/45 nm logic	180 nm CIS	45 nm CIS/65 nm Logic	45 nm CIS/65 nm Logic
Pixel array	64 M	0.8 M	0.07 M	9.2 M	0.02 M	8.3 M	4 M
Pixel pitch (μm)	N/A	4	15	4.86	NA	1.1	2.2
FWC (e-)	1.2×10^4	1.3×10^5	N/A	N/A	6.5×10^3	N/A	3×10^4
Noise (e-)	1.2	4	N/A	N/A	0.32	0.66	0.27
DR (dB)	80	90	124	>124 dB	84.8	N/A	100

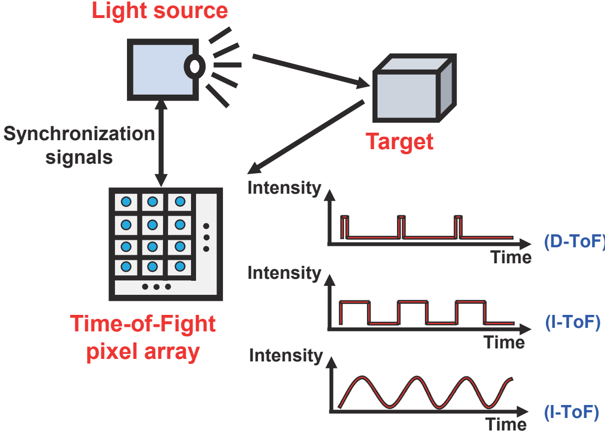


Fig. 29. (Color online) Principles of ToF sensor system.

formation based on timing or time-gated integration pixels.

6.3.1. Direct ToF (D-ToF) sensor

D-ToF sensor directly measures the flight-time of the pulsed light to calculate the depth between the target and the sensor by recording the pulsed light emission time and photon-incidence time using high resolution time-to-digital converter (TDC) and high-gain photodetector. The photodetector is usually implemented with avalanche photodiode (APD) or single-photon avalanche diode (SPAD). As SPAD has characteristics of high sensitivity, fast response speed and low time jitter, it is more commonly used in D-ToF sensors compared with APD. According to the measurement principle of D-ToF sensor, the depth (d) can be calculated by

$$d = \frac{ct}{2}, \tag{4}$$

where t is the flight time of the light and c is the speed of the light. This equation shows that to reach a millimetric depth resolution, the flight time of the light should be measured with picosecond level precision.

Although D-ToF sensor can achieve long detection distance, its lateral resolution is limited. This is because, a large number of on-chip memories and processing units, which include transimpedance amplifier (TIA) or TDC and histogram generating/processing circuits, are usually required by the pixel array to avoid the influence of photon detection probability and dark count rate of SPAD. Furthermore, the power consumption, dynamic range (DR), frame rate and the adaptability with ambient light of the D-ToF sensor still limit its application areas.

To improve the lateral resolution and frame rate, the pixel-wise exposure control and adaptive clocked recharging have been proposed to suppress the maximum power consumption and improve the DR, so that the lateral resolution of D-ToF sensor has been improved to 960 × 960 with 143 dB DR, 90 fps frame rate and 0.37 W power consumption[260]. Furthermore, in this sensor, 3D-stacked BSI CMOS process has been adopted to reduce pixel pitch down to 9.585 μm. To suppress the ambient light, small clusters of pixels and shared TDC with coincidence detection method are used to perform photon detection, which makes sensor achieve maximum detection distance above 100 m at 10 klux background light with TDC resolution of 60 ps[261]. In Ref. [262], macro pixels including 3 × 3 or 6 × 6 SPADs and the background signal subtraction in the histogram processing are proposed to make the D-ToF sensor achieve a maximum detection distance of 200 m at 117 klux background light.

The technology trend of the D-ToF sensors are similar to the CMOS image sensors. The early D-ToF sensors realized with front-side illuminated (FSI) CMOS process, have the disadvantages of large pixel size and low lateral resolution[263, 264]. Recently, the 3D-stacked BSI CMOS process has been adopted in D-ToF sensors to achieve small pixel size and high lateral resolution[260]. In these sensors, the pixel array and logic circuits can firstly be optimized individually in different chips, and then be connected with face-to-face bonding technology.

6.3.2. Indirect ToF (I-ToF) sensor

I-ToF sensor measures the phase shift of the modulated light to indirectly calculate the depth. The phase shift is measured by the demodulation process, in which the reflected light signal is sampled by four clocks with different phases. If the phase shifts between the sampling clock and the emitted signal are set to be 0°, 90°,180° and 270° at four sampling points, respectively. The phase shift ϕ can be calculated by

$$\phi = \arctan \frac{S_3 - S_1}{S_2 - S_0}, \tag{5}$$

where S_0–S_3 represents the sampled signals in four sampling phases. Since the demodulated phase delay has an unambiguous range of 2π, the maximum measurement depth range d_R is limited by

$$d_R = \frac{c}{4\pi f_m} \cdot 2\pi = \frac{c}{2f_m}. \tag{6}$$

I-ToF sensor can achieve higher lateral resolution than D-ToF sensor. This is because the I-ToF sensor can detect the

phase shift by performing simple calculations without large volume memories and complex processing units. However, the maximum detection distance of the I-ToF sensor is short because of the limited emitting power of the light source and limited sensitivity of the photodetector. Furthermore, there are two critical problems in I-ToF sensor: motion artifact for moving objects and depth error from background light or multi-user interference.

To suppress the motion artifact, a dynamic pseudo 4-Tap pixel has been proposed to generate a depth image in a single frame, and over-pixel MIM capacitor has been used to achieve background light cancelling over 120 klux[265]. To cancel out the multi-user interference and suppress the motion artifact, another I-ToF sensor with 4-tap pixel and lateral resolution of 1280 × 960 has also been proposed[266], which adopts multiple-interleaving and pseudorandom modulation methods reduce the peak current and cancel out the multi-user interference respectively. To further improve the depth measurement precision, the charge injection pseudo photocurrent reference has been used to reduce the gating driver jitter, and the depth measurement precision has been improved to 38 μm[267].

The technology trend of the I-ToF sensors is similar to the D-ToF sensors. The early I-ToF sensors, implemented with FSI CMOS process, have the shortcomings of large pixel size and low lateral resolution[268]. Then, the BSI CMOS process, has been used to improve sensitivity of the pixel to reduce the pixel size and improve the lateral resolution[269]. Recently, 3D-stacked BSI CMOS process has also been adopted to further reduce the pixel size and improve the lateral resolution[270].

To further improve the lateral and depth resolution of D-ToF sensor, the ToF sensors combining both D-ToF and I-ToF methods have been reported recently. By detecting phases for short ranges while creating a sparse depth map with counting photons for long ranges, the lateral resolution has been improved to 1200 × 900 with configurable depth resolution down to 10 cm[271]. In this sensor, a 6 μm pixel circuit including a vertical APD and a charge accumulator has been proposed, and the single-slope column analog-to-digital converters (ADC) are also included in the sensor. Another ToF sensor using in-pixel histogramming TDC based on quaternary search and time-gated Δ-intensity phase detection achieves lateral resolution of 80 × 60 and depth resolution of 1.5 cm[272].

Several ToF sensors combing D-ToF and I-ToF methods proposed in recent years are implemented with FSI CMOS process[271–273]. The prototype sensor in Ref. [271], implemented with vertical APD in FSI CMOS process, not only achieves high depth resolution similar to the I-ToF sensors, but also achieves much further maximum detection distance than I-ToF sensors. Although the sensors implemented with SPAD still suffer from low spatial resolution[272, 273], the depth resolution has been improved compared with that of D-ToF sensor.

In summary, Fig. 30 illustrates the number of pixels versus the maximum detection distance of ToF sensors[261, 262, 265, 266, 271, 273, 274–276], showing that the maximum detection distance of D-ToF sensors and the number of pixels of I-ToF sensors are kept increasing in recent years. Although, the ToF sensors combing D-ToF and I-ToF methods show a moderate maximum detection distance, the depth resolution is higher than that of D-ToF sensors. Moreover, for the ToF sensors

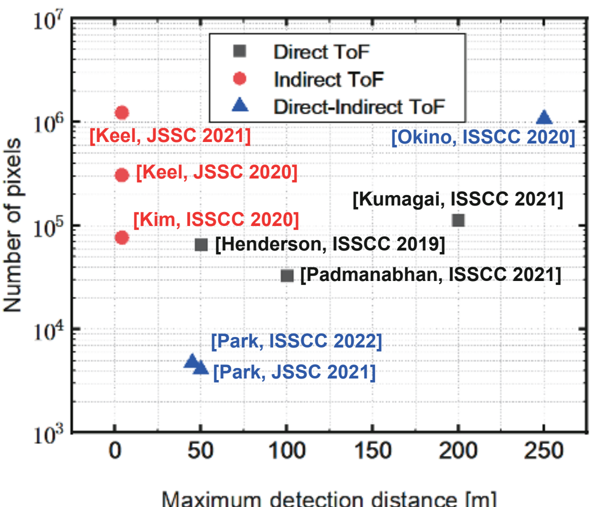


Fig. 30. (Color online) Number of pixels versus the maximum detection distance of ToF sensors.

combing D-ToF and I-ToF methods, if vertical APD is adopted in the pixel, the maximum detection distance and the lateral resolution can be greatly improved. Table 8 shows the performances of the state-of-the-art ToF sensors. For D-ToF sensors, the resolution has been improved up to 1 M pixels, and the power consumption from the SPAD array grows significantly under high light conditions. In the future, smarter pixel architecture and signal processing unit can be expected to realize an energy efficient D-ToF sensor with high frame rates. For I-ToF sensors, high lateral resolution and depth resolution have been achieved. However, the motion artifact and depth error from background light or multi-user interference still need be reduced in the future for improving reliability in applications. For ToF sensors combing D-ToF and I-ToF methods, 3D-stacked BSI CMOS process could be adopted to further reduce the pixel size and improve the lateral resolution.

7. Emerging directions

This section will be focusing on the emerging technologies and applications. In the recent years, there are two major emerging hot topics: 1) the quantum computing, and 2) the application-specific integrated circuit (ASIC) design for biomedical and/or healthcare applications.

7.1. Cryogenic CMOS for qubit

Compare with the classical computing, quantum computing features higher computing speed and parallel computing capability[277, 278]. The quantum computing systems usually work in the cryogenic temperature environment, while the qubit control devices usually work at room temperature[279]. Typically, a computing system with only 50 qubits requires about 2000 interconnecting cables and hundreds of microwave instruments, which result in a huge system volume size. With the rapid development of quantum computing, although a 127-qubit computing system (IBM, Eagle)[280] has be realized, an available quantum computing system with error correction capability needs at least hundreds of qubits[281]. The key challenges in the design of a very-large-scale quantum computing system are placed in the number of interconnect cables, noise crosstalk, limited cooling power, and

Table 8. Performance summary of the state-of-the-art ToF sensors.

	ISSCC '22, Canon, [260]	ISSCC '21, Neuchâtel, [261]	ISSCC '21, Sony, [262]	ISSCC '20, Sungkyunkwan U., [265]	JSSC '21, Samsung, [266]	ISSCC '2, Panasonic, [271]	ISSCC '22, UNIST, [272]
ToF type	Direct	Direct	Direct	Indirect	Indirect	Direct+Indirect	Direct+Indirect
Process	90 nm/40 nm 3D-BSI CMOS	45 nm CIS3D-BSI	90 nm/40 nm 3D BSI CMOS	90 nmBSI CMOS	65 nm/65 nm 3D BSI CMOS	65 nm CMOS	110 nm
Pixel array	960 × 960	256 × 128	189 × 600	320 × 240	1280 × 960	1200 × 900	80 × 60
Pixel pitch (μm)	9.585	7	10	8	3.5	6	75
Wavelength (nm)	510	780	905	N/A	850/940	N/A	905
Fill factor (%)	~100	N/A	N/A	43	N/A	N/A	10.4
Frame rate (fps)	90	N/A	20	10–60	60	450	30
Maximum range (m)	N/A	100	150–200	0.75–4.0	0.4–4.0	250	45
Depth resolution/ Depth noise	N/A	7 cm	15–30 cm	<0.54%	<0.92% (full) <0.3% (2 × 2 bin)	1.5 m@max.range 10 cm@min.range	2.5 cm
DR (dB)	143	N/A	N/A	N/A	N/A	N/A	N/A
Background light (klux)	N/A	8–10	117	>120	0.7/20	N/A	30
Power (mW)	330–370	51.9	N/A	N/A	290 (full), 220 (2 × 2 bin)	2500	1500

computing system volume. The cryogenic CMOS IC technology provide a promising solution for the miniaturization of quantum computing systems.

Charbon *et al.*[282, 283] first proposed a cryogenic qubit controller scheme based on the standard CMOS technology. The key circuit blocks were verified at the cryogenic temperature of 4 K. Bardin *et al.*[284] realized a monolithically integrated qubit control chip for the first time, which can directly work at a 3K cryogenic temperature and can only control the *XY* axis of a single qubit. Patra *et al.*[285] realized a qubit controller with a complete pulse shaping circuits integrated. This controller integrated 4 independent channels. Each channel controls 32 qubits with a time-division multiplexing mode. Park *et al.*[286] further improved the qubit controller integrated both the qubit state readout circuits and the auxiliary circuits, such as the microcontrollers, the temperature sensors, etc. This is the first fully functional qubit control SoC IC. In addition, Frank *et al.*[287] proposed a qubit controller with a semi-automatic digital processing unit integrated on the chip to generate the specific pulses for qubit controlling. The power dissipation of such controller has been reduced significantly. Kang *et al.*[288] further reduced the power consumption by adopting a pulse shaping scheme combining a linear digital-to-analog converter and a nonlinear digital-to-analog converter. A local oscillator circuit was also integrated on the chip.

The qubit state readout circuit is a key module in the qubit controller. Prabowo *et al.*[289] realized the quadrature readout circuit of the gate-biased spin qubit for the first time, which can work directly at a cryogenic temperature of 4.2 K. Ruffino *et al.*[290] proposed the first low-IF readout circuit with a local oscillator circuit integrated together. A noise figure of 0.55 dB and a bandwidth of 1.4 GHz bandwidth can be achieved. In addition, Gong *et al.*[291] realized an oscillator with an on-chip auto-calibration technique to optimize the phase noise performance and ensure that the oscillator can obtain optimal phase noise performance at each frequency. Peng *et al.*[292] proposed a cryogenic oscillator with wide adjustment range and low flicker noise corner frequency for the first time in SiGe process by adopted the hybrid mode switching technology. Kiene *et al.*[293] realized a cryogenic 1 GS/s 8-bit analog-to-digital converter circuit for the first time, which provided the possibility of on-chip digital post-processing for qubit state readout.

The research on cryogenic temperature qubit controlling IC is one of the emerging technology direction in the last decade. The reported solution still suffers from its high-power consumption, single control function, and limited capability of multi-qubits controlling. Recent researches are pushing the frontier of cryogenic qubit controller with lower power consumption and higher integration of more complex quantum system controlling functionalities.

7.2. Biomedical frontiers

Recent development in advanced electrochemistry materials and low-power circuit technology makes it possible to create super compact sensor system for various applications, i.e., healthcare and scientific researches. Typically a sensor interface with the impedance detection capability is required. Qu *et al.*[294] presents an electrochemical impedance spectroscopy (EIS) SoC for electrochemical gas detection with 0.28 mΩ sensitivity, 105 dB dynamic range and less than 1 μA average power, by maintaining a good trade-off between the low-power module and the high speed. Sonmezoglu and Maharbiz[295] present a fully implantable, wireless, battery-free, real-time deep-tissue oxygen sensor system combines a luminescence sensor with ultrasound technology, achieving better resolution, lower power consumption and smaller volume. Yeknami *et al.*[296] describes a 0.3 V biofuel-cell-powered glucose/lactate, representative of physiologic indicators in human perspiration, biosensing system with a delta-sigma ADC and a wireless transmitter. Circuit designs such as dynamic threshold MOS (DTMOS) techniques, 3× clock boosting circuit, and passive integrator are used to guarantee efficiency at low supply voltages. Ansary *et al.*[297] presents a CMOS-based miniature impedance analyzer for low-power high-spatial-resolution monitoring of Potassium (K+) achieving near the 1pA sensitivity with the advanced electrode sur-

face in vivo in an anesthetized immobilized mouse.

Advanced imaging technologies have also been applied to realize compact device for biomedical applications. Jang *et al.*[298] demonstrates a 4-camera VGA resolution capsule endoscope system with integrated high-throughput communications and sub-cm range capsule tracking with 360°-visual angle. Park *et al.*[299] shows a 1225-channel neuromorphic retinal prosthesis (NRP) SoC with 56.3 nW/Ch neuromorphic image processor and the localized (49-point) temperature regulation circuit. The NRP SoC adopts spike-based photo-diode sensor (Spike PD) and neuromorphic image processor (NMIP) to minimize the static power dissipation and regulates the supply voltage of LDOs and bridge rectifier to reduce temperature increase.

In addition, ultrasound, light and other energy supply methods and information transmission technology have been introduced into neural interface applications experiments. Yu *et al.*[300] shows an implantable neuro-stimulator utilizing magnetoelectric power and data transfer. The Magnetoelectric neural implant integrates a 1.5 mm^2 180-nm CMOS SoC, an in-house built 4×2 mm^2 magnetoelectric film, a single energy storage capacitor, and on-board electrodes onto a flexible polyimide substrate. Lee *et al.*[301] presents the electronics for a wireless electrode unit, powered by, and communicating through a microscale optical interface, achieving lower power consumption and higher integration level. Xu *et al.*[302] introduces a low-power active ASIC for multimodal wearable functional brain imaging including near-infrared spectroscopy (NIRS) (supporting both SiPMs and PDs), electroencephalogram (EEG), electrical impedance tomography (EIT) for the first time. Li *et al.*[303] shows an ambient energy harvesting and a body-coupled power delivery system, achieving full-body coverage “body-coupled power delivery” and the placement-independent “body-coupled ambient energy harvesting”. Tang *et al.*[304] showcases a wireless concurrent EEG recording and body-coupled communication with a concentric electrode based on blind courtesy copy data transmitting.

8. Conclusions

Thanks to the great joint efforts of a large number of Authors, who presented their understanding and insights with their expertise, this paper summarizes the IC design trends in the year of 2022. Although the integrated circuits have been developed for decades, new system architectures and novel circuit topologies/techniques still keep coming out. And people's demands for higher data rate, higher energy efficiency, higher level of integration, smarter and safer electronic devices have not stopped.

Application-specific or domain-specific IC designs are trending in the AI machine learning and biomedical areas. Hybrid conversion topologies are very popular not only for data converters, but also for power converters as well as for sensors. The operation frequencies of the communication ICs range from kHz to mm-wave bands. To arrive at energy-efficient, compact, and robust solutions, the circuit systems heavily depend on semiconductor technologies, electronic devices, packaging, as well as high-quality passive components. Due to limited capacity and capability, we cannot discuss all the interesting and trending IC design topics in this paper. We believe that more promising solutions to the current challenges and more killer applications will appear to keep the IC design area thriving and flourishing. Last but not least, we hope you enjoyed reading this paper and could find this paper useful for your future research and works.

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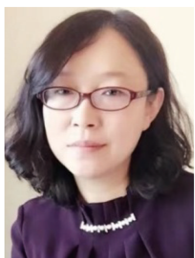
Chi-Hang Chan was born in Macau S.A.R., China, in 1985. He received the B.S. degree in electrical engineering from University of Washington (U.W. Seattle), USA, in 2008, the M.S. and Ph.D. degree from the University of Macau, Macao, China, in 2012 and 2015, respectively, where he currently serves as an Assistant Professor. He is the recipient of the 2015 IEEE Solid-State-Circuit-Society (SSCS) Pre-doctoral Achievement Award. He also is the co-recipient of the 2014 ESSCIRC best paper award. His research interests include Nyquist and oversampling ADCs, PLL, hardware security and mixed-signal circuits.

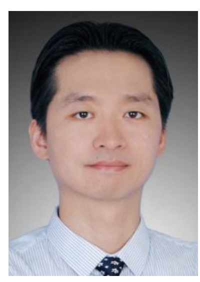
Lin Cheng received the B.Eng degree from Hefei University of Technology, Hefei, in 2008, the M.Sc. degree from Fudan University, Shanghai, in 2011, and the Ph.D. degree from The Hong Kong University of Science and Technology (HKUST), Hong Kong, China, in 2016. In 2018, he joined the School of Microelectronics, USTC, where he is currently a Professor. Before that, he was a Post-doc Researcher with HKUST and an Analog Design Intern with Broadcom, San Jose, USA. His current research interests include power management and mixed-signal integrated ICs, wireless power transfer circuits and systems, and automotive ICs. Dr. Cheng was a recipient of the IEEE SSCS Pre-doctoral Achievement Award 2014–2015, Hong Kong Institution of Science 2018 Young Scientist Awards (Honorable Mention).

Wei Deng received the B.S. and M.S. degrees from the University of Electronic Science and Technology of China (UESTC), China, and the Ph.D. degree from the Tokyo Institute of Technology, Japan. He was with Apple Inc., Cupertino, CA, USA and currently he is an Associate Professor at Tsinghua University. He is a TPC Member of ISSCC, VLSI, and ESSCIRC. He is an AE of the IEEE SSC-L.

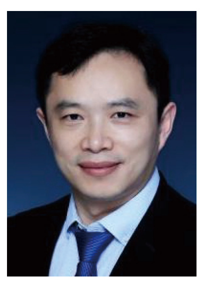
Peng Feng got his BS degree in 2006 at Sichuan University and the PhD degree in 2011 at the Institute of Semiconductors, Chinese Academy of Sciences (CAS). He is now an associate researcher at the Institute of Semiconductors, CAS. His research interests include ultra-low power mixed signal/RF integrated circuits and CMOS image sensors.



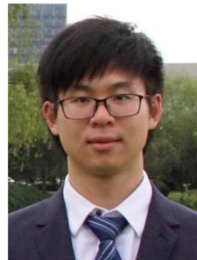
Li Geng is currently a Professor with the School of Microelectronics, Xi'an Jiaotong University, Xi'an. Her research interests include power management integrated circuits, low-voltage low-power analog and mixed-signal integrated circuits, RF integrated circuit, and bio-implant systems. Dr. Geng was a Technical Program Committee Member of ASSCC from 2010 to 2018. She is currently a Technical Program Committee Member of ISSCC. She was a recipient of the Science and Technology Improvement Award by the Ministry of National Mechanical Industry, China, in 1999, and also the Science and Technology Improvement Award by Shaanxi Municipal Government in 2000, 2001, 2010, 2015 and 2021.



Mo Huang received the B.Sc., M.Sc., and Ph.D. degrees in microelectronics and solid-state electronics from Sun Yat-sen University, Guangzhou, China, in 2005, 2008, and 2014, respectively. From 2008 to 2014, he was an IC Design Engineer and a Project Manager with Rising Microelectronic Ltd., Guangzhou, China. From 2015 to 2016, he was a Post-Doctoral Fellow with the State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macau, China. From 2017 to 2019, he was with the School of Electronic and Information Engineering, South China University of Technology, Guangzhou, China, as an Associate Professor. He is now an Assistant Professor with Institute of Microelectronics, University of Macau, Macau, China. His current research interests include power management IC design.



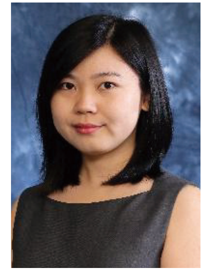
Haikun Jia received the Ph.D. and B.S. degree in electronics engineering from Tsinghua University, Beijing, China, in 2015 and 2009, respectively. Since 2020, He works as an Assistant Professor in Tsinghua University. His research interests include millimeter-wave integrated circuits, systems, and high-speed wireline transceivers.



Lu Jie received the B.Eng. degree in Electrical and Electronic Engineering from the Zhejiang University, Hangzhou, Zhejiang, China, in 2017, M.S. and Ph.D. degree in Electrical and Computer Engineering from the University of Michigan, Ann Arbor, US, in 2021. Since 2021, he is currently with Tsinghua University, Beijing, China, as an Assistant Professor. His research interest includes hybrid-architecture ADCs, high-speed circuits, and mixed-signal computation.

Ka-Meng Lei received the B.Sc. degree in EEE from the University of Macau in 2012. He received the Ph.D. degree in ECE in the State-Key Laboratory of AMS-VLSI and FST, University of Macau, in 2016. He serves as an Assistant Professor at the University of Macau since 2019. He was a Postdoctoral Fellow at Harvard University from 2017 to 2019. His current research interests include ultralow voltage analog circuit techniques, sensors and analog front-end interfaces, and high-resolution portable NMR platform. Dr. Lei (co-)received Distinguished Design Award in IEEE A-SSCC 2015; the Silkroad Award in ISSCC 2016; and IEEE SSCS Pre-doctoral Achievement Award 2017. He serves as the TPC member of ICTA. He is the Associate Editor of IEEE Open Journal of Circuits and Systems.

Xihao Liu received the B.Sc. degree in microelectronics from Xi'an Jiaotong University, Xi'an, China, in 2020, where he is currently working toward the Ph.D. degree in the School of Microelectronics. His research interests include power management circuit and system design.



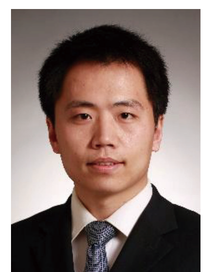
Xun Liu is an Assistant Professor with the School of Science and Engineering (SSE), Chinese University of Hong Kong, Shenzhen. She received the B.Eng. degree in Electronic and Information Engineering from Zhejiang University, China in 2011, and the Ph.D. degree in electronic and computer engineering from The Hong Kong University of Science and Technology (HKUST), Hong Kong, in 2017. She was a senior design engineer with Qualcomm, Santa Clara, USA, working on cutting-edge integrated circuits and systems designs for 5G application, and holding 2 US patents. She is a TPC Member of ISSCC.

Yongpan Liu received the B.S. (99), M.S. (02), and Ph.D. (07) degrees all from Tsinghua University. He is currently a Full Professor (Cheung Kong Scholar) with the Department of Electronic Engineering, Tsinghua University, China. Prof. Liu is a Program Committee Member for ISSCC, A-SSCC and DAC. He served as General Secretary for ASPDAC 2021 and Technical Program Chair for NVMSA 2019. He was Associate Editor of the IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, the IEEE Transaction on Circuits and Systems II, and the IET Cyber-Physical Systems. He is an IEEE Senior Member. He served as A-SSCC 2020 and AICAS 2022 tutorial speaker and IEEE CASS Distinguished Lecturer 2021.

Yan Lu received his BEng and MSc degrees from South China University of Technology, Guangzhou, in 2006 and 2009, respectively, and the PhD degree in 2013 from the Hong Kong University of Science and Technology (HKUST), Hong Kong, China. In 2014, he joined the State Key Laboratory of AMS-VLSI, University of Macau, Macao, China, where he is currently an Associate Professor. He has authored/coauthored two books and more than 120 peer-reviewed technical papers. His research interests include wireless power transfer circuits and systems, high density power converters, integrated voltage regulators. He served as a Guest Editor for IEEE JSSC, TCAS-I and TCAS-II, is serving on the TPC of ISSCC and CICC, and is an IEEE SSCS Distinguished Lecturer 2022-23.

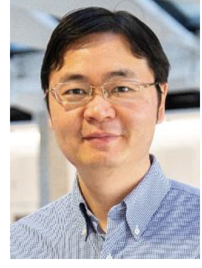
Kaiming Nie received the B.E., M.S., and Ph.D. degrees from the School of Electronic Information and Engineering, Tianjin University, Tianjin, China, in 2009, 2011, and 2014, respectively. From July 2014 to September 2017, he had been a post-doctoral researcher at the same institution. Since September 2017, he has been an Associate Professor at the School of Microelectronics, Tianjin University. His research interests are in mixed analog/digital circuit design and CMOS image sensor design.

Dongfang Pan received the Ph.D. degree in electronics science and technology from the Department of Electronics Science and Technology, University of Science and Technology of China (USTC), China, in 2019. From 2018 to 2019, He was a Visiting Scholar with the Department of Electrical Engineering, Southern Methodist University (SMU), Dallas, USA. From 2019 to 2021, he was a Post-Doctoral Fellow with the School of Microelectronics, USTC. He is currently an Associate Researcher with the School of Microelectronics at USTC. His research interests include Isolated DC-DC converters, high-frequency power ICs, CMOS RF transceivers, and system designs including PA, LNA, VCO, and analog IC.



Nan Qi received the B.S. degree from Beijing Institute of Technology, Beijing, China, in 2005, the M.S. and Ph.D. degrees in microelectronics from Tsinghua University, Beijing, in 2008 and 2013, respectively. From 2013 to 2015, he was a Research Scholar with the Department of Electrical Engineering and Computer Science, Oregon State University, Corvallis, OR, USA. From 2015 to 2017, he was a Visiting Scholar and Circuit-Design Engineer at Hewlett-Packard Labs, Palo Alto, CA, USA. In 2017, he joined the Institute of Semiconductors, Chinese Academy of Sciences, Beijing, China, where he is now a Professor of Electrical Circuits and Systems. His research interests include the design of integrated circuits for high-speed wireline and optical transceivers.

Sai-Weng Sin is currently an Associate Professor with the Dept. of ECE, Faculty of Science and Technology, and the Deputy Director of State-Key Laboratory of AMS-VLSI, University of Macau. He holds 7 US and 3 Taiwan patents and 150 technical journals and conference papers in the field of high-performance data converters and analog mixed-signal integrated circuits. Dr. Sin is a TPC member of IEEE A-SSCC. He served as an Associate Editor for the IEEE Transaction on Circuits and Systems II – Express Briefs. He was the co-recipient of the 2011 ISSCC Silk Road Award, Student Design Contest Award in A-SSCC 2011 and the 2011 State Science and Technology Progress Award (second-class), China.

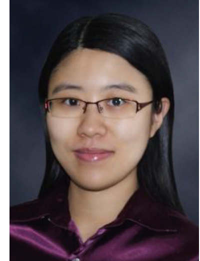


Nan Sun is a Professor with Tsinghua University since 2020. He was Assistant and then tenured Associate Professor with University of Texas at Austin. He received B.S. degree from Tsinghua University in 2006, and Ph.D. degree from Harvard University in 2010. Dr. Sun received the NSF Career Award in 2013, and the IEEE SSCS New Frontier Award in 2020. He has published 30+ JSSC papers and 50+ ISSCC/VLSI/CICC/ESSCIRC papers. He has graduated 26 PhD students, 10 of whom are professors at top universities in the US and China. He serves on the TPC of ISSCC, CICC, and ASSCC. He was Associate Editor of IEEE TCAS-I, and a Guest Editor of JSSC. He also serves as Distinguished Lecturer for both IEEE Circuits-and-Systems Society and IEEE Solid-State Circuits Society.

Wenyu Sun received B.S. degree and Ph.D. degree in electrical engineering from Tsinghua University, Beijing, China, in 2016 and 2021, respectively. He is currently a post-doctoral researcher at Tsinghua Shenzhen International Graduate School. His research interests include deep learning and energy-efficient circuit design for AI accelerators, and he has authored or co-authored more than 15 papers in related conferences and transactions. He won the second place in EDAthon 2017 (Programming Competition on Electronic Design Automation) hosted by IEEE CEDA, and the second prize of final contest in International Invitational Tournament for Brain-inspired Computing and Application 2017.

Jiangtao Xu received the B.E., M.S., and Ph.D. degrees from the School of Electronic Information and Engineering, Tianjin University, Tianjin, China, in 2001, 2004, and 2007, respectively. From 2007 to 2010, he was a Lecturer, and from 2010 to 2018 he was an Associate Professor at Tianjin University. Since 2018, he has been a professor at the School of Microelectronics, Tianjin University. His research interests are in CMOS image sensors and mixed signal integrated circuits.

Jinshan Yue received the B.S. and Ph.D. degree from the Electronic Engineering Department, Tsinghua University, Beijing, China, in 2016 and 2021, respectively. He is currently a post doctor and research assistant in the Institute of Microelectronics, Chinese Academy of Sciences. His current research interests include energy-efficient neural network processor, non-volatile memory, and computing-in-memory system design. He has authored and co-authored over 30 technical papers. He has received the excellent doctoral dissertation of Tsinghua University, ASP-DAC2021 Student Research Forum Best Poster Award, and 2021 Beijing Nova Program.



Milin Zhang is an Associate Professor in the Department of Electronic Engineering, Tsinghua University. She received the B.S. and M.S. degrees in electronic engineering from Tsinghua University, Beijing, China, in 2004 and 2006, respectively, and the Ph.D. degree in the ECE Department, Hong Kong University of Science and Technology (HKUST), Hong Kong. Then, she worked as a postdoctoral researcher at the University of Pennsylvania, USA. She joined Tsinghua University in 2016. Her research interests include designing of various non-traditional imaging sensors and biomedical sensing applications. She serves and has served as the TPC member of ISSCC, CICC, A-SSCC and ISCAS. She is the Chapter Chair of the SSCS Beijing chapter.

Zhao Zhang received the Ph.D. degree from the Institute of Semiconductors, Chinese Academy of Sciences, Beijing, in 2016. From 2016 to 2018, he was a Post-Doctoral Fellow with The Hong Kong University of Science and Technology, Hong Kong. From 2019 to 2020, he was an Assistant Professor with Hiroshima University, Higashi-Hiroshima, Japan. In 2020, he joined the Institute of Semiconductors, Chinese Academy of Sciences, where he is currently a Full Professor. His research interests include the design of low-jitter PLLs, ultra-high-speed wireline transceivers, and ultra-low-voltage ICs. He (co)authored more than 40 conference and journal papers, including ISSCC, VLSI and JSSC. He is the guest editor of Electronics Letters, and a reviewer of JSSC, TCAS-I, TCAS-II, TMTT.