

# Effect of charge trapping on electrical characteristics of silicon junctionless nanowire transistor

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**Abstract:** We investigated the effect of charge trapping on electrical characteristics of silicon junctionless nanowire transistors which are fabricated on heavily n-type doped silicon-on-insulator substrate. The obvious random telegraph noise and current hysteresis observed at the temperature of 10 K indicate the existence of acceptor-like traps. The position depth of the traps in the oxide from Si/SiO<sub>2</sub> interface is 0.35 nm, calculated by utilizing the dependence of the capture and emission time on the gate voltage. Moreover, by constructing a three-dimensional model of tri-gate device structure in COMSOL Multiphysics simulation software, we achieved the trap density of  $1.9 \times 10^{12} \text{ cm}^{-2}$  and the energy level position of traps at 0.18 eV below the intrinsic Fermi level.

**Key words:** junctionless transistor; charge trapping; random telegraph signals

**Citation:** Y F Fu, L H Ma, Z Y Duan, and W H Han, Effect of charge trapping on electrical characteristics of silicon junctionless nanowire transistor[J]. *J. Semicond.*, 2022, 43(5), 054101. <https://doi.org/10.1088/1674-4926/43/5/054101>

## 1. Introduction

Rapid downscaling of metal-oxide-semiconductor field-effect transistors (MOSFETs) causes many adverse issues, such as short channel effects (SCEs) and carrier mobility degradation, which will seriously affect the performance of related devices. More seriously, as the size of MOSFETs continues to shrink to the nanometer scale, the fabrication process for the source/drain of the traditional inversion mode transistor is facing more challenges. In recent years, several novel materials have been proposed to keep up with the pace of Moore's law, such as two-dimensional (2D) semiconductor materials<sup>[1, 2]</sup>. For traditional silicon materials, researchers try to improve device performance from the aspect of device structure. A silicon-based junctionless nanowire transistor (JNT) which can be considered as a gated resistor, has been proposed as a promising alternative to a new generation of transistors. The manufacturing process of JNT is relatively simple, with a constant doping concentration from source to drain and without any PN junctions. In addition, JNT is completely compatible with the CMOS manufacturing process<sup>[3–5]</sup>. Compared with existing field-effect transistors (FETs), JNTs have more potential advantages due to junctionless characteristics. For example, the manufacturing complexity is reduced due to the low thermal budget and the requirement to eliminate junctions as well as reduce the SCEs<sup>[6, 7]</sup>. Consequently, JNT has the potential to become the sub-10 nm technology node and subsequent technical solution<sup>[8]</sup>.

The key to the fabrication of JNTs is that the channel must be thin enough to ensure that the device is turned off at zero gate voltage. In addition, due to the excellent electrostatic controllability, the tri-gate structure is undoubtedly the best choice for JNT manufacture. Interface traps will be inevitably formed in the process of transistor fabrication, which will directly affect the electrical characteristics and reliability of devices<sup>[9–12]</sup>. Owing to the large surface-to-bulk aspect ratio, the trapping and detrapping of the interface traps become crucial in JNT. Random telegraph signals (RTS) are fluctuations of the current between discrete levels. In nanoscale transistors, two-level fluctuations are generally attributed to the capture and emission of single carrier by traps in the gate oxide layer. Since the carriers in the JNTs are transported in bulk model, the noise signal caused by the surface roughness of the nanowire can be ignored. Hence, JNT is suitable to observe RTS introduced by the interface traps. Previous publications which describe the electrical characteristics for JNT mostly focus on ideal conditions<sup>[13–15]</sup>. In fact, whether for long-channel or short-channel devices, the interface traps in the gate dielectric stack can affect the electrical properties of the devices, such as changing the threshold voltage, causing irregular current jump, and reducing the drive current.

In this paper, we fabricated tri-gate JNTs through experiments, and investigated the electrical properties of the fabricated devices at different temperatures. At low temperatures, we observed irregular current protrusions. This is a phenomenon caused by interface traps. We analyzed the influence of interface traps on the electrical characteristics of JNT by adding interface traps with different densities and different energy levels to a three-dimension (3D) model built by COMSOL Multiphysics simulation software<sup>[16]</sup>. Besides, according to the

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Received 24 DECEMBER 2021; Revised 21 JANUARY 2022.

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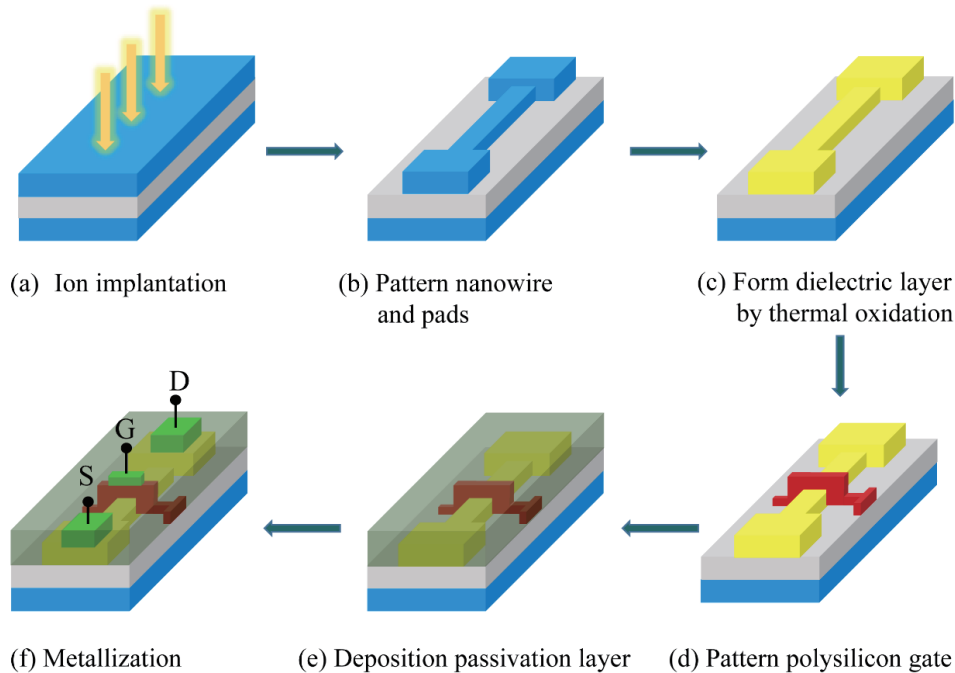


Fig. 1. (Color online) Schematic diagrams of the fabrication process for JNTs.

trap density obtained by the experiment, combined with the simulation results, we get the energy level position of interface traps. This paper can provide guidance for the extraction of the spatial position and energy level position of interface defects in transistors.

## 2. Experimental methods

Fig. 1 shows the schematic diagrams of the fabrication process of JNTs. The devices were fabricated on a silicon-on-insulator (SOI) substrate with the top silicon layer of 55 nm. The SOI wafer was uniformly and heavily doped by phosphorus ion implantation with a dose of  $5 \times 10^{13} \text{ cm}^{-2}$  (Fig. 1(a)). And then electron beam lithography (EBL) and inductively coupled plasma (ICP) etching were performed to define the active region and the channel fin (Fig. 1(b)). It was followed by a sacrificial oxidation to eliminate the etching induced surface damage and then 22-nm-thick gate oxide was grown at 900 °C in dry oxygen for 1 h (Fig. 1(c)). Then, a 150-nm-thick boron doped polysilicon gate was defined, wrapped around three sides of the silicon channel (Fig. 1(d)). The poly-silicon was then doped by arsenic ion implantation at a dose of  $1 \times 10^{20} \text{ cm}^{-3}$  after annealing at 1000 °C for 10 s. After depositing 200-nm-thick silicon dioxide as the protective layer, ohmic contact windows were opened (Fig. 1(e)). Following 400-nm-thick aluminum was evaporated and lifted off as final metallization via conventional optical lithography (Fig. 1(f)). The cross-section schematics and the scanning electron microscope (SEM) image of the tri-gate JNT are shown in Fig. 2. The final cross section of the silicon core was estimated to be 30 nm in height ( $H$ ) and 30 nm in width ( $W$ ), respectively. The length of polysilicon gate ( $L_g$ ) was 280 nm. For the low temperature electrical characterization, the devices were measured in a vacuum chamber, which can be cooled down to 10 K. The conventional operation of JNTs is to apply a positive gate voltage to create an electroneutral region in the channel region and allow electrons to flow.

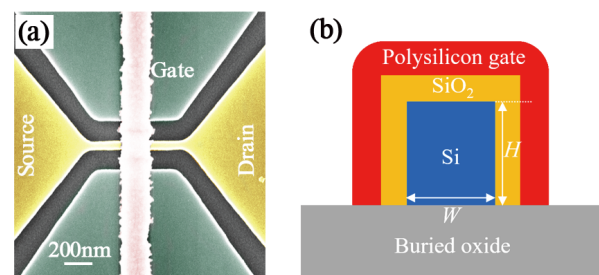


Fig. 2. (Color online) (a) The color SEM image of devices with the gate length of 280 nm. (b) The cross-section schematics of the devices.

## 3. Results and discussion

Firstly, we tested the relevant electrical characteristics of the devices at room temperature. Fig. 3(a) shows the transfer characteristic curves. The drain voltage  $V_{DS}$  is set to be 0.1 to 4.1 V with the step of 1 V. As the gate voltage  $V_{GS}$  continues to increase, the drain current  $I_{DS}$  also increases, gradually reaching a saturated state. The subthreshold swing (SS) and the threshold voltage ( $V_{TH}$ ) are 132 mV/dec and 0.26 V, respectively. The curves of drain current  $I_{DS}$  versus  $V_{GS}$  show that the fabricated JNT operates as a normally-off device with a low gate leakage current of several pA and the on/off current ratio larger than  $1 \times 10^4$ . Besides, the output curves in Fig. 3(b) demonstrate excellent gate control ability in our devices.

The temperature-dependent electrical properties of JNT were carried out by Lakershore-340 temperature controller under vacuum environment. Fig. 4(a) shows the output characteristics of JNT measured at the temperature of 10 K. Obvious current jumps are observed at some special values of  $V_{GS}$  such as 2.20 V. Besides, the current jumps increase with the increase of the absolute value of the bias, indicating the existence of active traps<sup>[17]</sup>. For the analysis of current hysteresis, a single staircase voltage ramp was used. The gate voltage  $V_{GS}$  was varied by 0.02 V steps and the duration of each step was 0.1 s, and  $V_{DS}$  was set to be 0.2 V. In the forward sweep,

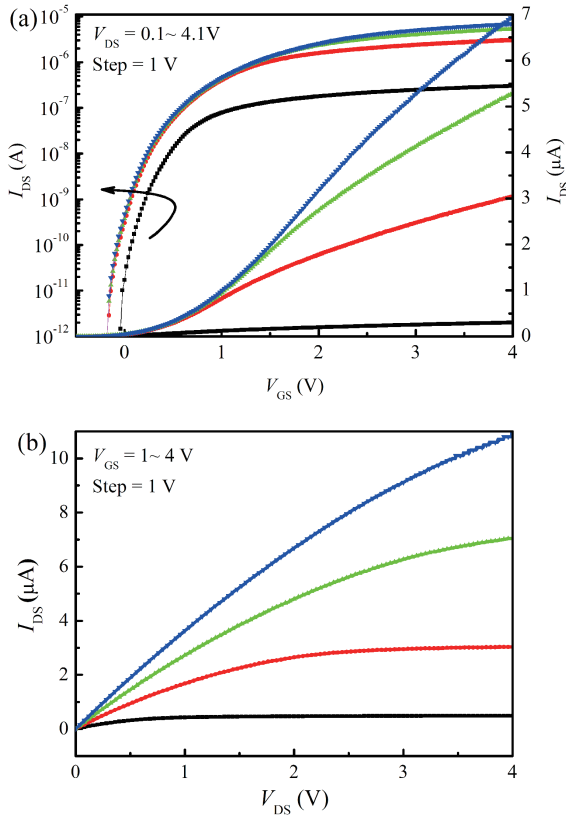


Fig. 3. (Color online) Measured drain current characteristics at room temperature, showing (a) drain current versus gate voltage for drain voltages of 0.1 to 4.1 V with step of 1 V, and (b) drain current versus drain voltage for gate voltages from 1 to 4 V with step of 1 V.

the forward bias was increased from 0 to 3.5 V. In the backward sweep, the sweep started at 3.5 V, and was gradually decreased to 0 V. The measured results are shown in Fig. 4(b). The curves clearly show hysteretic nature. The current hysteresis behavior is larger than that measured during the reverse sweep. This is because the charging and discharging process are slower than the sweep rate, leading to identical currents in both sweep directions due to the fact that the traps cannot remain in the same initial state<sup>[18]</sup>.

Fig. 5(a) shows the transfer characteristic curve of this device at a low temperature of 10 K. The drain voltage is set to be 2–10 mV with the step of 2 mV. Obvious current jumps are observed around the gate bias of roughly 2.2 V, at which voltage, the trap level and the silicon channel Fermi level move close to each other so that hopping and tunneling happen. The trap is found to be an acceptor type center<sup>[19]</sup>. Typical time domain current levels are shown in Fig. 5(b). The average time at the highest current level, so-called the capture time  $\tau_c$ , decreases as  $V_{GS}$  increases. It is ascribed to the fact that the electron concentration in channel increases with increasing  $V_{GS}$ . The average time at the lowest current level, can be considered as the emission time  $\tau_e$ . The accurate vertical trap depth  $x_T$  can be extracted by the following expression<sup>[20]</sup>

$$x_T = -\frac{kT}{q} \frac{d \ln(\tau_c/\tau_e)}{dV_{GS}} t_{ox}, \quad (1)$$

where  $t_{ox}$  is the oxide thickness,  $k$  is Boltzmann constant and  $q$  is the elementary charge. Through linear fitting of  $V_{GS}$  dependence of  $\ln(\tau_c/\tau_e)$  as shown in Fig. 6, the accurate vertical

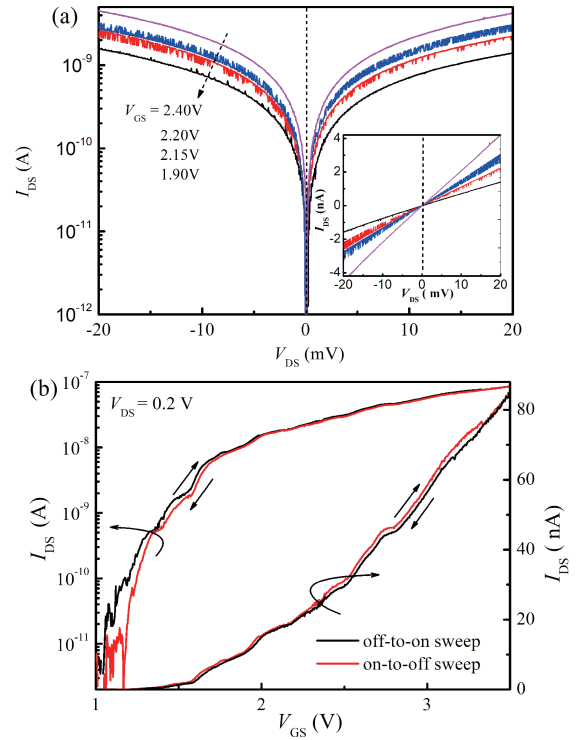


Fig. 4. (Color online) (a)  $I_{DS}$ - $V_{DS}$  output characteristics of JNT device at  $T = 10$  K. (b) The transfer characteristics of the JNT with  $V_{GS}$  sweep from 0 to 3.5 V and back.

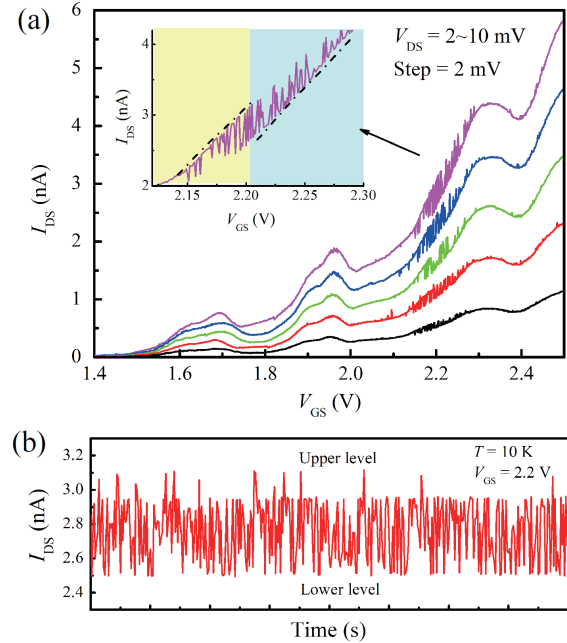


Fig. 5. (Color online) (a)  $I_{DS}$ - $V_{GS}$  curves for  $V_{DS}$  values ranging from 2 to 10 mV in steps of 2 mV. The detail image in the upper left corner is an enlarged detail. (b) Time domain current levels versus time trace at  $V_{GS} = 2.2$  V and  $V_{DS} = 10$  mV.

trap depth obtained by Eq. (1) is 0.35 nm. Compared to the oxide thickness of 22 nm, these traps can be considered as interface traps.

In Fig. 7(a), the measured  $I_{DS}$  as a function of the  $V_{GS}$  with the device biased at a drain voltage of  $V_{DS} = 0.1$  V is presented for different temperatures. It can be noted that the drain current decreases with temperature. The threshold voltage  $V_{TH}$  and subthreshold swing  $SS$  are presented as a function of

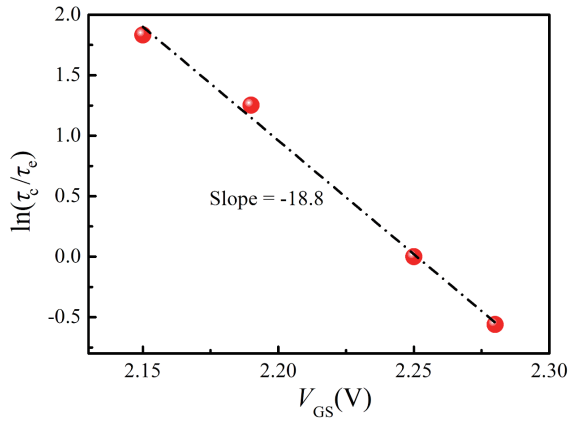


Fig. 6. (Color online)  $\ln(\tau_c/\tau_e)$  and its linear fitting. The slope is proportional to  $x_T$ , the position of the traps in the oxide.

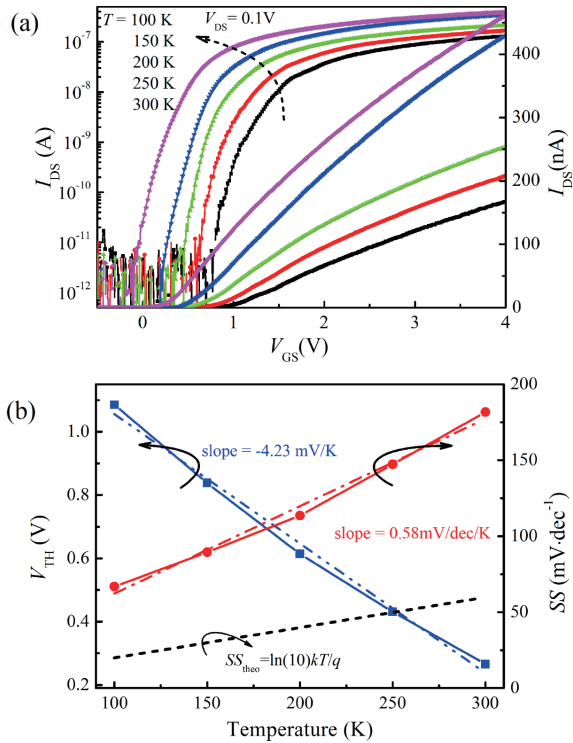


Fig. 7. (Color online) (a) Transfer characteristics at the temperatures of 100 to 300 K with the step of 50 K. (b) Measured  $V_{TH}$  and SS at  $V_{DS} = 0.1$  V versus temperature. The black dashed line represents the theoretical value of subthreshold swing  $SS_{theo}$ .

the temperatures in Fig. 7(b). The slope of  $V_{TH}$  varied with the temperatures is an approach to  $-4.23$  mV/K and the slope of SS is  $0.58$  mV/dec/K. It should be noted that the SS variation with temperatures of our JNT device is larger than that of the theoretical value. We attribute this phenomenon to the influence of interface traps. The subthreshold swing SS depending on the trap density  $N_{trap}$  is described by<sup>[21]</sup>

$$SS = \frac{kT \ln 10}{q} \left( 1 + \frac{q^2 N_{trap}}{C_{ox}} \right), \quad (2)$$

where  $C_{ox}$  is the gate oxide capacitance per unit area (estimated to be  $1.56 \times 10^{-7}$  F/cm<sup>2</sup>). The presence of interface traps will deteriorate the subthreshold characteristics. The interface trap density obtained from Eq. (2) is approximately to be

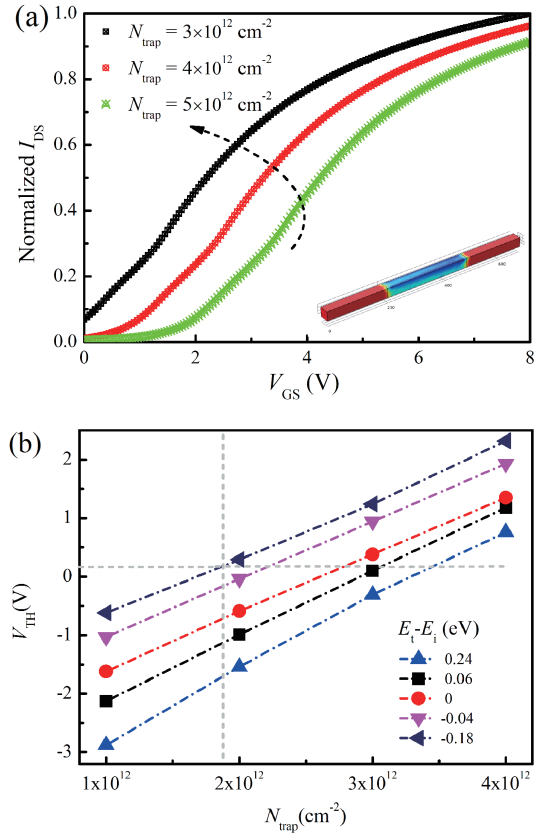


Fig. 8. (Color online) (a) Simulated  $I_{DS}-V_{GS}$  curves for different trap densities with the trap level equals to the intrinsic Fermi level. (b) Threshold voltage as a function of trap densities with different trap levels.

$1.9 \times 10^{12}$  cm<sup>-2</sup>.

To further investigate the influence of interface traps on JNT electrical characteristics, we construct a 3D tri-gate JNT structure in COMSOL Multiphysics simulation software with the Semiconductor Module. The parameters of the simulation device are consistent with the experimental device. The gate with a 22-nm-thick oxide layer and surface traps is modeled using the thin insulator gate boundary condition around the perimeter of the channel. The drain and source boundaries are ideal ohmic contacts, and the voltages are set to ground and 0.1 V, respectively. The gate voltage is swept from 0 to 8 V for different surface trap densities. The simulated device structure is shown in the insert of Fig. 8(a). Here,  $L_s$  and  $L_d$  are the distances of the source and the drain from the channel region, respectively. Those two parameters are set to 200 nm. At first, the influence of trap density on the transfer characteristic is investigated. The simulated curves are shown in Fig. 8(a). The transfer curves are positively shifted with increasing interface trap density. Besides, the influence of the trap levels is also investigated in Fig. 8(b). Here the energy difference between the trap energy level  $E_t$  and the intrinsic Fermi level  $E_i$  is set as  $-0.18$ ,  $-0.04$ ,  $0$ ,  $0.06$  and  $0.24$  eV, respectively. For the same trap density, the threshold voltage will shift positively as the trap level moves away from the conduction band. Therefore, combining the experimental data with the simulation results, we obtain that the position of trap level is 0.18 eV below the intrinsic Fermi level, and the trap density is  $1.9 \times 10^{12}$  cm<sup>-2</sup>.



## 4. Conclusion

In summary, we fabricated junctionless tri-gate nanowire transistors on the SOI substrate. We analyzed the electrical properties of the manufactured devices at different temperatures (10–300 K). Obvious RTS were observed at low temperature of 10 K. This phenomenon indicates that there are acceptor-like trap states in the devices. Through linear fitting of gate voltage dependence of  $\ln(\tau_c/\tau_e)$ , the accurate vertical trap depth of 0.35 nm is obtained. Thus, the acceptor-like traps can be considered as interface traps. Besides, from the slope of the subthreshold swing versus temperature, we estimate the interface trap density to be  $1.9 \times 10^{12} \text{ cm}^{-2}$ . In addition, we use COMSOL Multiphysics simulation software to build a 3D model for the device. In the model, traps with different densities and different energy levels are added to the interface between the conductive channel and the gate dielectric layer. According to the simulation results of threshold voltage, we estimate that the energy level of the interface traps is located at 0.18 eV below the intrinsic Fermi level. The results provide a theoretical guidance for analyzing the effects of interface traps on the junctionless transistors.

## Acknowledgements

This work is supported by the National Natural Science Foundation of China (Grant Nos. 613760966, 1327813, 61404126 and 11947115), the Natural Science Foundation of Henan Province under (Grant No. 202300410444), and Foreign Experts Program of Ministry of Science and Technology in China (Grant No. G2021026027L).

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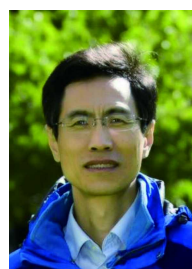
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