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Double-balanced mixer based on monolayer graphene field-effect transistors

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Abstract: Graphene field-effect transistors (GFET) have attracted much attention in the radio frequency (RF) and microwave fields because of its extremely high carrier mobility. In this paper, a GFET with a gate length of 5 μm is fabricated through the van der Walls (vdW) transfer process, and then the existing large-signal GFET model is described, and the model is implemented in Verilog-A for analysis in RF and microwave circuits. Next a double-balanced mixer based on four GFETs is designed and analyzed in advanced design system (ADS) tools. Finally, the simulation results show that with the input of 300 and 280 MHz, the IIP3 of the mixed signal is 24.5 dBm.

Key words: GFET; mixer; RF; simulation; IIP3

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1. Introduction

Since the discovery of monolayer graphene[1], graphene has become an attractive candidate to replace or supplement traditional semiconductors due to its excellent electrical and mechanical properties, as well as high compatibility with standard processes. Compared with semiconductors, only one atomic layer thickness, ultra-high carrier mobility[2–4] and higher saturation velocity[5] make it possible to produce graphene field-effect transistors (GFETs) with higher cut-off frequencies[6]. Bipolar transmission is a main feature of GFETs, that is, the conductivity of GFETs can be controlled by holes or electrons. It results in a 'V'-shaped transfer characteristic (I_{ds}–V_{gs})[1]. Due to its unique ambipolar transport properties and extremely high mobility, graphene provides a wide range of applications for radio frequency and microwave fields.

Because of these excellent characteristics, graphene was used in practice, such as frequency multipliers[7, 8], voltage amplifiers[9], ring oscillators[10], and mixers[11]. Graphene is even being studied in fields related to RF switches[12] and memory[13]. The study of graphene mixers is particularly concerned. Mixers are essential for almost all telecommunications and radar equipment, and limit the intermodulation performance of the receiver front end. Schottky barrier diodes and active FETs are the most commonly used mixer elements in microwave systems, but the linearity of these mixers is very low due to the strong nonlinearity of these devices. In contrast, the linear output characteristics of graphene makes it particularly suitable for such circuit applications. Although unsaturation is detrimental to traditional amplifier circuits, it is an advantage of resistive mixers now. Palacios *et al.* prepared a graphene resistive mixer for the first time using the characteristics of graphene bipolar transport. Conversion loss was 30–40 dB and IIP3 was 13.8 dBm at 10 MHz[14]. In Ref. [15], the first graphene integrated circuit work was to realize a resistive mixer. Moon *et al.* also used the structure to prepare a graphene mixer, and showed the IIP3 of 22 dBm at a LO power of –3.5 dBm[16].

This paper explores the potential of graphene mixers. In order to further improve the linearity of the mixers, a graphene double-balanced mixer with four GFETs with cross-coupling structure is designed. The circuit structure is based on a proposed GFET large-signal model in ADS for circuit simulation[17]. And it achieves IIP3 of 24.5 dBm with a LO signal of –2 dBm at 280 MHz. The main performance characteristics of the double-balanced GFET mixer are compared with CMOS technologies and the reported GFET mixer.

2. Monolayer graphene field-effect transistor

2.1. GFET fabrication

In this work, the transistor was fabricated on a high-resistance silicon (>10 kΩ·cm) substrate with 1 μm thick silicon oxide. Monolayer graphene is grown on Ge substrate by chemical vapor deposition (CVD) method[18], and germanium-based graphene is used as a smooth substrate. Then 50 nm Au was evaporated by UV lithography and electron beam as source and drain, next 3 nm Al was evaporated by electron beam, after that 30 nm Al_2O_3 was grown by ALD as the gate dielectric layer, and then 50 nm Au was evaporated by electron beam as the top gate electrode. Finally, the PVA solution was dripped, and after the PVA was dried, the metal (source and drain)/oxide layer (gate dielectric layer)/metal (gate) sandwich layer was transferred to the SiO_2/Si (>10 kΩ·cm) with graphene channel. A GFET is formed on the substrate, and the graphene channel forms a vdW contact with the contact electrode. This transfer process reduces the damage of photolithography to the graphene channel and the contact resistance, which can have better device performance[19–21].

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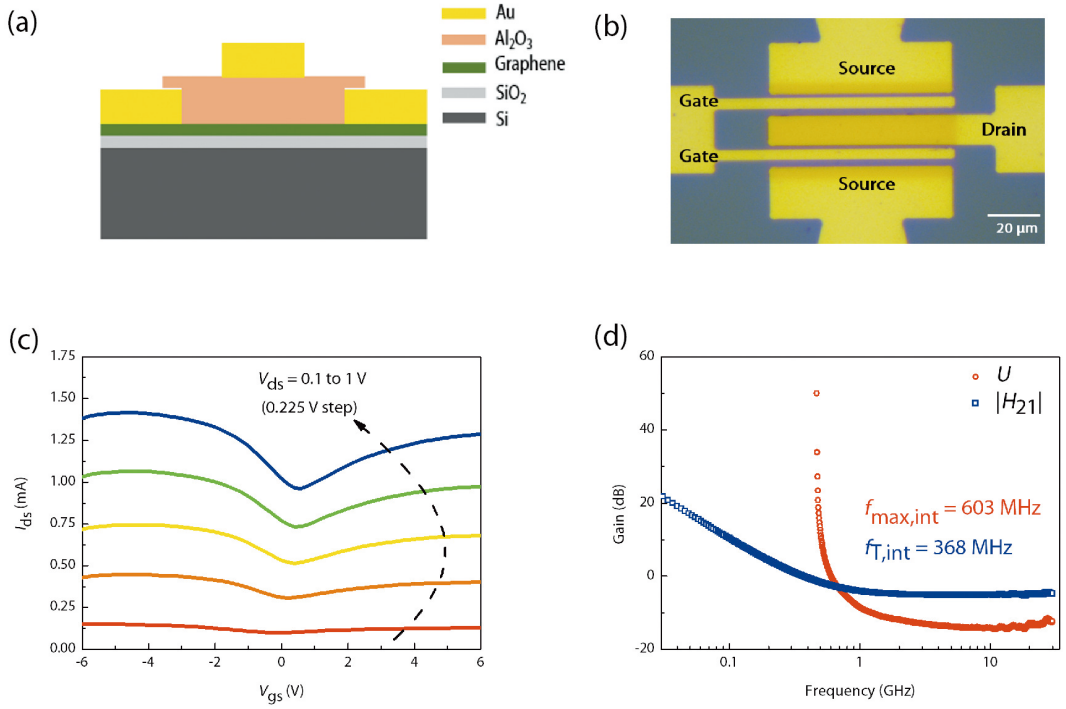

Fig. 1. (Color online) (a) Schematic of top-gated Al_2O_3/monolayer graphene FET. (b) Photograph of a dual-finger gate 5-μm-length and 70-μm-wide graphene FET. (c) Measured data for the I_{ds}–V_{gs} characteristic curves at V_{ds} = 0.1 to 1 V. (d) Current gain, $|H_{21}|$, and unilateral gain, U, with de-embedding at V_{ds} = 0.8 V.

Fig. 1(a) shows a 3D schematic diagram of GFETs on SiO_2/Si. Fig. 1(b) is an optical microscope image of GFETs with a dual-finger gate and ground–signal–ground (GSG) structure for the RF test. The gate length L_g is 5 μm and gate width W is 70 μm. Fig. 1(c) presents the transfer characteristic curve (I_{ds}–V_{gs}) of the GFET at V_{ds} = 0.1 to 1 V and the Dirac point was observed to be located at around V_{dirac} = –0.2 V. We adopt standard de-embedding method for avoiding the influence of parasitic capacitance and inductance of the GSG pad[22]. And we prepared the open circuit and short circuit structure of the same device size to ensure reliable de-embedding results. In Fig. 1(d), we show the current gain $|H_{21}|$ and the unilateral gain $|U|$ of the GFET with L_g = 5 μm and W = 70 μm at V_{ds}= 0.8 V. The highest (intrinsic) maximum oscillation frequency f_{MAX} of ~603 MHz and the highest (intrinsic) cutoff frequency f_T of ~368 MHz are found.

2.2. A large-signal model of monolayer GFET

During circuit design, accurate GFET models are required to predict device and circuit performance. The small signal model cannot describe the nonlinear effects of the device to meet the simulation requirements of nonlinear circuits such as mixers and oscillators. However, the large signal model can give the complete characteristics of the device. Several models of GFET were developed recently[23–27]. This article uses a monolayer GFET large-signal behavior model developed by Jan Stake *et al.* and based on the drift-diffusion equation[17].

In this model, the graphene quantum capacitance will be ignored when the thickness of the gate dielectric layer is greater than 10 nm. And we also ignore the quantum capacitance of graphene. The model can be implemented by Verilog-A language in ADS environment.

The schematic of a monolayer GFET large-signal model is presented in Fig. 2. The current in the channel can be expressed as:

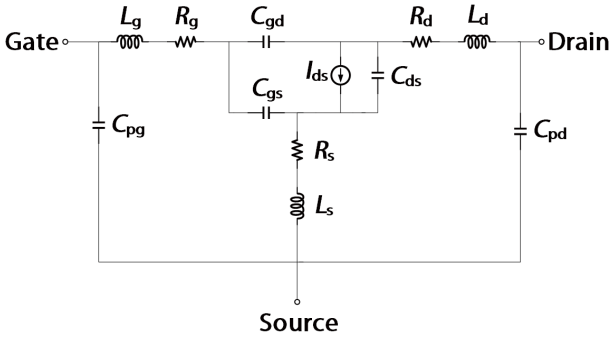

Fig. 2. Large-signal model of a GFET. C_{pd}, C_{pg}, L_g, L_d and L_s are pad parasitic capacitance values and inductances, R_g is the gate resistance, and R_s and R_d are the source and drain resistances including contact and access resistances.

$$I_{ds1} = \frac{\mu_e V_{dirac} Q_0}{\sqrt{1+\frac{\mu_e |V_{gs} V_{ds}|}{L v_{sat}}}} \frac{W}{L} f\left(\overline{V_{gs}}, \overline{V_{gd}}\right) \quad (1)$$

with $V_{gs} > 0$, $V_{gd} > 0$.

$$I_{ds2} = \frac{\mu_e V_{dirac} Q_0}{\sqrt{1+\frac{\mu_e |V_{gs} V_{ds}|}{L v_{sat}}}} \frac{W}{L} f\left(\overline{V_{gs}}, 0\right) + \frac{\mu_h V_{dirac} Q_0}{\sqrt{1+\frac{\mu_h |V_{gs} V_{ds}|}{L v_{sat}}}} \frac{W}{L} f\left(0, \overline{V_{gd}}\right) \quad (2)$$

with $V_{gs} > 0$, $V_{gd} < 0$.

Table 1. GFET large-signal model parameters.

Parameter	Value	Parameter	Value
C_{gs}	327 fF	L_g	83 pH
C_{gd}	8 fF	R_g	30 Ω
C_{ds}	15 fF	R_0	326 Ω
C_{pd}	32 fF	R_{ext0}	26 Ω
C_{pg}	35 fF	μ_e	1108 cm^2/(V·s)
L_s	25 pH	μ_h	2080 cm^2/(V·s)
L_d	39 pH	V_{dirac}	–0.2 V

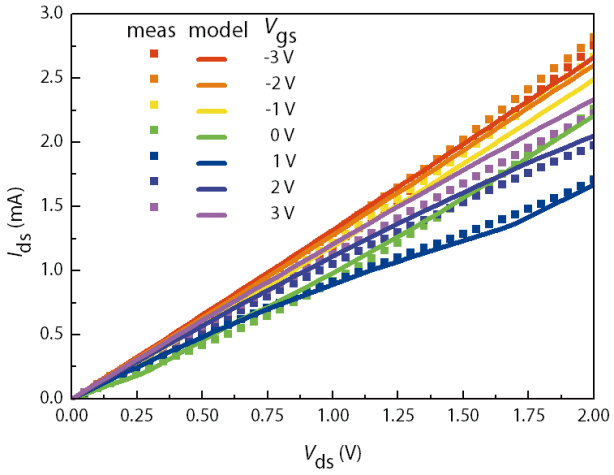

Fig. 3. (Color online) Model versus measured data for the I_{ds}–V_{ds} characteristic curves at V_{gs} = –3 to 3 V.

$$I_{ds3} = \frac{\mu_h V_{dirac} Q_0}{\sqrt{1+\frac{\mu_h |V_{gs} V_{ds}|}{L\overline{v_{sat}}}}} \frac{W}{L} f\left(\overline{V_{gs}}, 0\right) + \frac{\mu_e V_{dirac} Q_0}{\sqrt{1+\frac{\mu_e |V_{gs} V_{ds}|}{L\overline{v_{sat}}}}} \frac{W}{L} f\left(0, \overline{V_{gd}}\right) \quad (3)$$

with $V_{gs} < 0$, $V_{gd} > 0$.

$$I_{ds4} = \frac{\mu_h V_{dirac} Q_0}{\sqrt{1+\frac{\mu_h |V_{gs} V_{ds}|}{L\overline{v_{sat}}}}} \frac{W}{L} f\left(\overline{V_{gs}}, \overline{V_{gd}}\right) \quad (4)$$

with $V_{gs} < 0$, $V_{gd} < 0$.

Among them, the following function is defined as:

$$f(x,y) = x\sqrt{1+x^2} - y\sqrt{1+y^2} + \frac{\ln\sqrt{1+x^2}+x}{\sqrt{1+y^2}+y}, \quad (5)$$

where $\overline{v_{sat}} = v_F \beta \sqrt[4]{n_0^2 + \frac{C(V_{gs}+V_{gd})^2}{2q}}$ is the saturation velocity of the carrier at the average gate voltage, $C = (C_{gs} + C_{gd})/(LW)$ is the gate capacitance per area, $v_F = 10^8$ cm/s and β relates to the optical phonon wavelength of the dominant scattering phonon, Q_0 ($q \times n_0$) is the residual charge density, μ is the carrier mobility, V_{dirac} is the Dirac voltage, and defining: $\overline{V_{gs}} = V_{gs}/V_{dirac}$ and $\overline{V_{gd}} = V_{gd}/V_{dirac}$.

Resistance between the source and drain can be expressed as:

$$R_d = R_s = R_0 + R_{ext}(V_{gs}, V_{gd}), \quad (6)$$

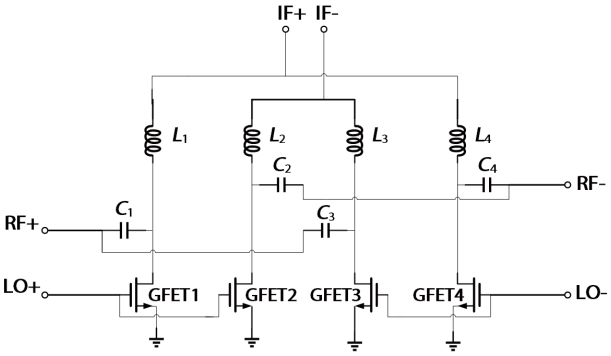

Fig. 4. Schematic of the GFET double-balanced mixer.

$$R_{ext}(V_{gs}, V_{gd}) = \frac{1+\tanh V_{gs}}{2} \frac{1+\tanh V_{gd}}{2} R_{ext0}, \quad (7)$$

where R_0 is the contact resistance and R_{ext0} is an extra resistance when the majority carriers are electron.

Intrinsic capacitors were extracted by *S*-parameters biased at Dirac voltage ($V_{gs} = V_{dirac}$, $g_m = 0$). By de-embedding the *S*-parameters, we can get: $C_{gd} = -Y_{12}/j\omega$, $C_{gs} = (Y_{11} + Y_{12})/j\omega$, $C_{ds} = \mathrm{Im}(Y_{22} + Y_{12})/\omega$. The model parameter extraction method in Fig. 2 is the same as the method described in Ref. [17], and the parameters were extracted as shown in Table 1. The behavior model is implemented by Verilog-A and is compatible with ADS. As shown in Fig. 3, the solid lines are the measured output characteristic curve (I_{ds}–V_{ds}) of the GFET, showing excellent linearity. The dotted lines are the output characteristic curves of the GFET DC simulation. It can be seen that the model is consistent with the measurement results. The large-signal model will be applied to subsequent mixer circuit design in section 3.

3. GFET double-balanced mixer

3.1. GFET mixer circuit design

Compared with a single GFET mixer, a graphene double-balanced mixer can have better linearity and can suppress the feedthrough of RF and LO signals[28]. The circuit diagram of the GFET double-balanced mixer in this article is shown in Fig. 4. It consists of four GFETs with cross-coupling structure and four LC components, in which the inductance is 25 nH and the capacitance is 25 pF. The LC component has a filtering function, and LO, RF and IF are all differential signals. The four GFETs (with L_g = 5 μm, W = 70 μm) operate at V_{gs} = –0.6 V and V_{ds} = 0.8 V. And the mixer is simulated in ADS. Due to the linear characteristics of the GFET, the mixer is expected to have a high linear output.

3.2. Simulation of the GFET double-balanced mixer

Fig. 5 shows the RF performance of the GFET double-balanced mixer. Fig. 5(a) presents the simulated conversion loss (CL) versus LO power with a minimum CL of 23 dB at 300 MHz. Fig. 5(b) is IF power versus RF power with f_{LO} = 280 MHz (4 dBm) and f_{RF} = 300 MHz. The dots in the figure are simulated data, and the line is the linear fitting, indicating that the 1 dB compression point is 6.5 dBm. Fig. 5(c) reveals the simulated two-tone spectra of the mixer. The third-order intermodulation product (IM3) is 85 dBm lower than IF with RF power of –20 dBm. According to IIP3 = RF_{in} + (IF – IM3)/2, IIP3 is calculated as 22.5 dBm. The fundamental and the third-order term in the output signal versus RF power are

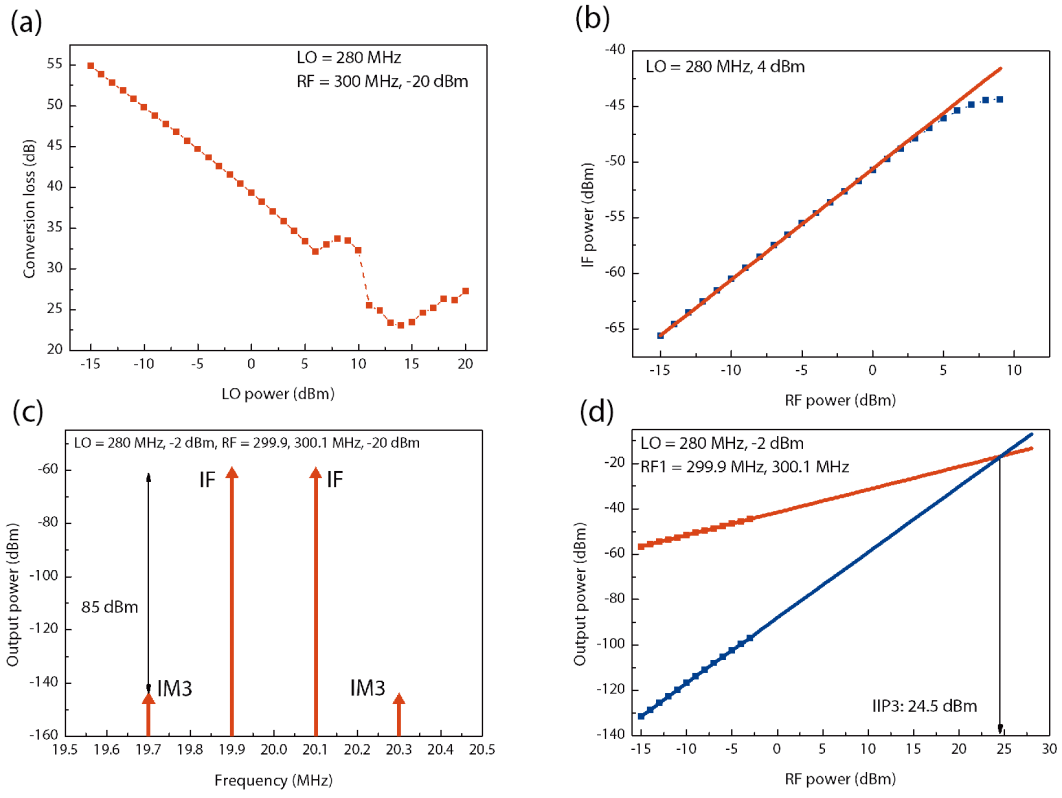

Fig. 5. (Color online) RF performance of the double-balanced mixer. (a) Simulation result of conversion gain. (b) Simulation result of –1 dB compress point. (c) Simulated two-tone spectrum of the mixer. (d) Simulation result of IIP3.

Table 2. Comparison between performance parameters of GFET and CMOS mixer.

Ref.	This work	[29]	[30]	[31]	[32]	[33]	[12]	[28]	[11]
Type	Sim.	Meas.	Meas.	Meas.	Sim.	Sim.	Meas.	Meas.	Meas.
Tech. (μm)	GFET, 5	CMOS, 0.18	CMOS, 0.065	CMOS, 0.032	CMOS, 0.18	CMOS, 0.18	GFET, 2	GFET, 1.5	GFET, 1
Freq. (GHz)	0.3	2–12	10	10	2.4	3.35	0.01	1.59	2
Gain (dB)	–23	11–13.3	–1.6	1	15.8	1.7	–40	–53	–22
IIP3 (dBm)	24.5	–8 to –6.8	15	12.6	1.4	–1.5	13.8	12.7	4.9

shown in Fig. 5(d). After linear fitting and expansion, the IIP3 is displayed as 24.5 dBm. In Table 2, the main performance of the mixer reported in this article is compared with the recently reported GFET mixer and CMOS mixer. It can be seen from the table that the designed mixer in this paper has more excellent linearity.

4. Conclusion

In this work, we prepared a monolayer GFET by transfer process and assessed the DC and RF characterization. And we performed large-signal modeling on the GFET, which is written in Verilog-A and connected in ADS. A double-balanced mixer is designed based on the GFET and it provides a IIP3 of 24.5 dBm at 300 MHz. Compared with traditional CMOS mixers and GFET mixers that have been reported, it has better linearity. In addition, the operating frequency of the mixer is only limited by the f_T of the GFET, and the gate length of the GFET can be reduced to broaden the operating frequency[34].

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