ARTICLES

Journal of Semiconductors
(2022) 43, 032801
doi: 10.1088/1674-4926/43/3/032801

Instability of parasitic capacitance in T-shape-gate enhancement-mode AlGaN/GaN MIS-HEMTs

Lan Bi[1, 2], Yixu Yao[1, 2], Qimeng Jiang[1, 2, †], Sen Huang[1, 2, †], Xinhua Wang[1, 2], Hao Jin[1, 2], Xinyue Dai[1, 2], Zhengyuan Xu[1], Jie Fan[1, 2], Haibo Yin[1, 2], Ke Wei[1, 2], and Xinyu Liu[1, 2]

[1]High-Frequency High-Voltage Device and Integrated Circuits R&D Center, Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China

[2]Institute of Microelectronics, University of Chinese Academy of Sciences, Beijing 100049, China

Abstract: Parasitic capacitances associated with overhangs of the T-shape-gate enhancement-mode (E-mode) GaN-based power device, were investigated by frequency/voltage-dependent capacitance–voltage and inductive-load switching measurements. The overhang capacitances induce a pinch-off voltage distinguished from that of the E-mode channel capacitance in the gate capacitance and the gate–drain capacitance characteristic curves. Frequency- and voltage-dependent tests confirm the instability caused by the trapping of interface/bulk states in the LPCVD-SiN_x passivation dielectric. Circuit-level double pulse measurement also reveals its impact on switching transition for power switching applications.

Key words: AlGaN/GaN MIS-HEMTs; enhancement-mode; T-shape gate; parasitic capacitance; trapping/de-trapping; capacitance-voltage hysteresis

Citation: L Bi, Y X Yao, Q M Jiang, S Huang, X H Wang, H Jin, X Y Dai, Z Y Xu, J Fan, H B Yin, K Wei, and X Y Liu, Instability of parasitic capacitance in T-shape-gate enhancement-mode AlGaN/GaN MIS-HEMTs[J]. *J. Semicond.*, 2022, 43(3), 032801. https://doi.org/10.1088/1674-4926/43/3/032801

1. Introduction

AlGaN/GaN high-electron mobility transistors (HEMTs) or metal–insulator–semiconductor HEMTs (MIS-HEMTs), by virtue of the superior polarization-induced high mobility 2-D electron gas (2DEG), are well-proposed for their high switching speed, low parasitic parameters and low on-resistance, and have achieved recognized success in both high frequency RF and power switching applications[1–4]. Gate- and/or source-field plates above thick passivation dielectrics like SiN_x, are commonly implemented to alleviate the high electric field in the gate-drain region and obtain higher breakdown voltage[5–7]. They are also contributed to the suppression of surface-state-introduced current collapse[5, 8]. However, the field plates structure will introduce extra parasitic capacitances, leading to higher $V_{DS} \times I_{DS}$ power loss and longer switching duration. In addition, the passivation layer will also bring in the passivation dielectric/(Al)GaN interface states and even bulk states in the dielectric itself. Their trapping/de-trapping processes cause the dynamic shifts of parasitic capacitances, leading to disordered ON-OFF transition and failure of dV/dt control in practical applications[9–11].

In this work, gate-related parasitic capacitances of the T-shape-gate E-mode AlGaN/GaN HEMT were investigated by high-frequency C–V measurements as well as the inductive switching measurement, where C_{GD} was individually observed during the Miller plateau. The instability of C_{GD}, caused by the trapping/de-trapping of deep interface/bulk states in LPCVD-SiN_x dielectric in the gate overhang region[12], was characterized by voltage-dependent C–V measurements.

2. Device fabrication and characteristics of E-mode MIS-HEMT

The E-mode MIS-HEMT was fabricated on an ultra-thin-barrier (UTB) AlGaN/GaN heterostructure grown on the Si substrate[13, 14]. The UTB AlGaN consists of a 1-nm AlN interlayer, a 3-nm $Al_{0.25}Ga_{0.75}N$ barrier layer and a 1.5-nm GaN cap layer. Fig. 1(a) shows the schematic structure of the E-mode MIS-HEMT. A 10-nm LPCVD-grown SiN_x passivation layer was able to recover the 2DEG at the UTB-AlGaN/GaN interface in the access region[15], featuring a sheet resistance of 545 Ω/□. The LPCVD-SiN_x in the gate region was etched by fluorine-based plasma. Then in-situ NH_3/N_2 remote plasma pretreatment was utilized to improve the etched (Al)GaN surface[16], followed by the gate dielectric deposition. The gate dielectric stack consists of a 3-nm atomic layer deposited (ALD) SiN_x layer and a 15-nm ALD-Al_2O_3 layer with an ozone precursor, followed by the evaporation of a Ni/Au bilayer gate metal. The fabricated E-mode MIS-HEMT features a total gate width of 1 mm, a gate length of 1 μm, a source-to-gate spacing of 1.75 μm, and a gate-to-drain spacing of 10 μm. The T-shape gate has a 0.5 μm overhang on the source side and a 0.75 μm overhang on the drain side, as shown in Fig. 1(b).

Fig. 2(a) shows the transfer characteristics at drain bias V_{DS} = 1 V and V_{DS} = 10 V. The E-mode MIS-HEMT exhibits a threshold voltage V_{TH} of 1.26 V defined at I_D = 1 μA with a hysteresis of 0.3 V at V_{DS} = 1 V, indicating a decent ALD-SiN_x/AlGaN (F-etched) interface quantity. Fig. 2(b) shows the output characteristics. A saturation current of 339 mA is obtained at

Correspondence to: Q M Jiang, jiangqimeng@ime.ac.cn; S Huang, huangsen@ime.ac.cn

Received 27 SEPTEMBER 2021; Revised 15 OCTOBER 2021.

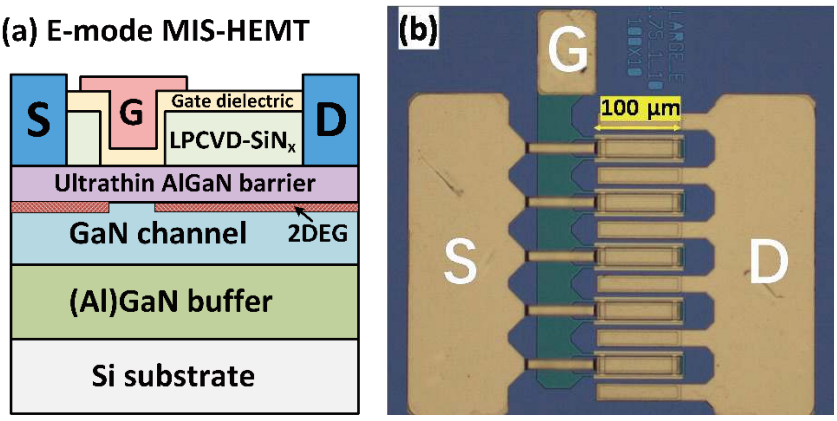

Fig. 1. (Color online) (a) Cross sectional schematic of the E-mode AlGaN/GaN MIS-HEMT. (b) Microscope photograph of a 1-mm device.

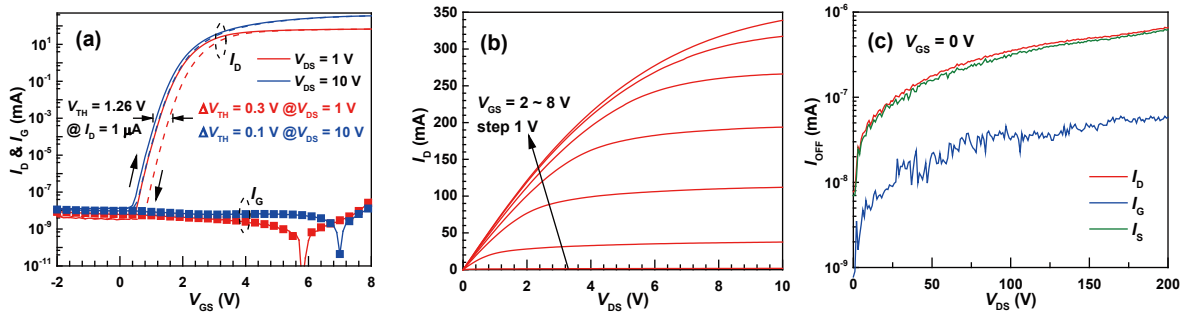

Fig. 2. (Color online) (a) Transfer, (b) output, and (c) three-terminal off-state leakage of the 1-mm E-mode MIS-HEMT.

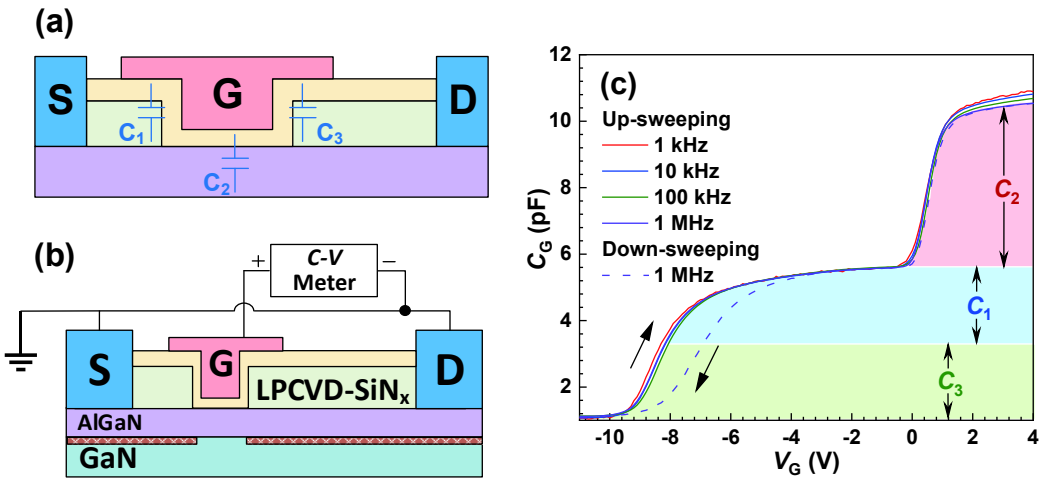

Fig. 3. (Color online) (a) Schematic of the gate-related capacitances in T-shape gate E-mode AlGaN/GaN MIS-HEMT. (b) Bias set of the C_G–V_G measurement, and (c) the multi-frequency curves of the 1-mm MIS-HEMT.

V_{GS} = 8 V. Fig. 2(c) shows the three-terminal off-state currents at V_{GS} = 0 V. A small drain leakage lower than 10^{-6} mA is obtained and the gate leakage is always around 10 times lower.

3. Gate-related capacitances and dynamic characteristics of E-mode MIS-HEMT

Fig. 3(a) shows the schematic of the gate-related capacitances in the T-shape gate E-mode AlGaN/GaN MIS-HEMT. C_2 is the channel capacitance performing in the E mode and C_1/C_3 is the gate-source/drain overlay capacitance performing in the depletion mode (D mode). Multi-frequency C–V measurements were conducted on the T-shape gate E-mode MIS-HEMT with source and drain both grounded (shown in Fig. 3(b)), and the C_G–V_G curves are shown in Fig. 3(c). Two pinch-off points are observed in the whole V_G range, corresponding to different capacitance components. The first one at V_G ~ –10 V is related to the overhang capacitances (i.e., C_1 and C_3), and the second one is related to the E-mode channel (i.e., C_2). Very small frequency dispersion is observed on both E-mode gate and D-mode gate overhang, informing a high quality ALD-SiN$_x$/(Al)GaN and LPCVD-SiN$_x$/(Al)GaN interface. Unlike the E-mode portion, the D-mode portion exhibits a noticeable hysteresis between up- and down-sweeping curve, probably caused by deep interface/bulk states in the LPCVD-SiN$_x$ passivation dielectric.

Since the Miller capacitance C_{GD} plays an important role

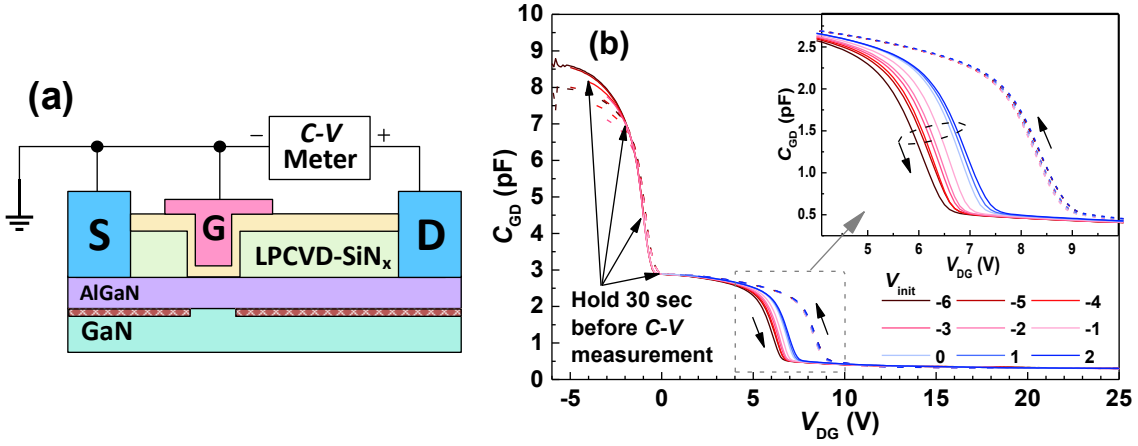

Fig. 4. (Color online) (a) Bias set of the C_{GD} measurement. (b) C_{GD}–V_{DG} curves with varied hold and forward stressing voltage.

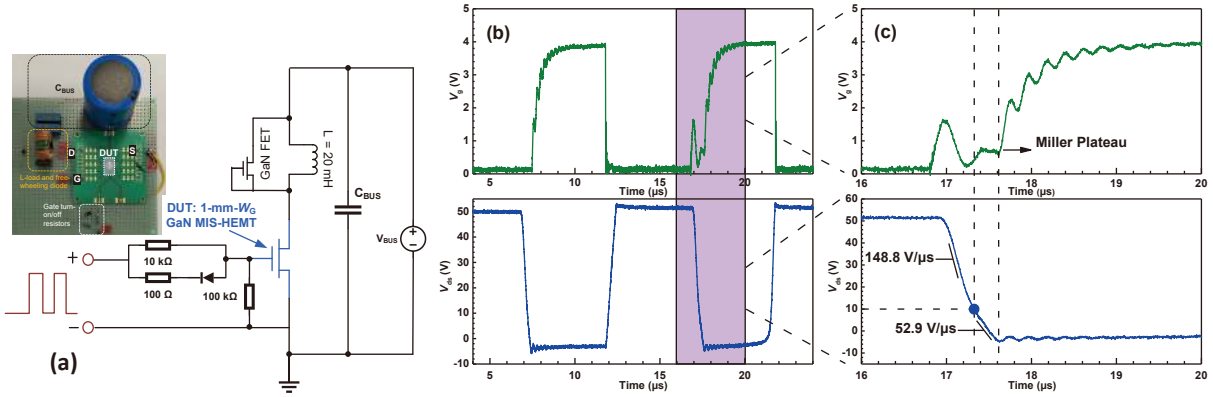

Fig. 5. (Color online) (a) Schematic and photo of the inductive switching circuit. (b) Waveform of the inductive switching under 50-V V_{BUS} and (c) the turn-on transients of the DUT.

on the device switching performance, in this paper, C_{GD} was individually investigated by *C*–*V* measurement with a shorted source/gate terminal and a sweeping drain terminal, as shown in Fig. 4(a). In this measurement, drain terminal voltage (V_{DG}) is swept from an initial voltage V_{init} (holding for 30 seconds before *C*–*V* sweep) to 25 V and double-mode sweep was used to estimate the instability of the C_{GD}. It is noted that a negative V_{DG}, corresponding to a positive bias applied on the overhang capacitor, is able to assist the spill-over of the electrons to the SiN_x/(Al)GaN interface as well as the trapping of the interface or dielectric bulk states. Fig. 4(b) plots the measurement results and an obvious hysteresis (> 1.5 V) on the up- and down-sweep D-mode pinch-off voltage is obtained, which is directly dependent on the magnitude of the negative stress voltage V_{init}. The hysteresis increases owing to the enhanced trapping in the passivation dielectric. In the down-sweep curves under different initial stress, the D-mode pinch-off voltage merges together, indicating that an efficient electrons' de-trapping is achieved with a 25 V V_{DG}.

In this work, to further identify the effect of the overhang capacitance on the device switching performance, a double-pulse measurement was executed with measurement setup plotted in Fig. 5(a). A device bare die was mounted on a testing PCB by conductive silver epoxy, and its pads were bonded out by golden wires. A simple gate driver circuit is used with a separate turn-on and turn-off path. In order to enlarge the Miller plateau, a 10 kΩ charging resistor was used to slow down the turning-on process. The waveform of inductive switching under 50 V V_{BUS} and the turn-on transients are shown in Figs. 5(b) and 5(c). During the turn-on period of the second pulse, the presence of the D-mode portion of C_{GD} reduces the slew rate of output voltage, leading to a longer Miller plateau and extra switching power loss. The turning point of two sections of dV_{DS}/dt is around 10 V in the beginning of Miller plateau, which coincides with the pinch-off voltage of C_{GD}.

4. Conclusion

In this work, gate-related capacitances of the T-shape-gate E-mode AlGaN/GaN HEMT have been investigated by *C*–*V* measurements and the inductive switching measurement. The overhang-related C_{GD} exhibits a noticeable hysteresis in double sweeps, informing its sensitivity to forward stressing voltage due to the trapping of deep interface/bulk states of LPCVD-SiN_x passivation dielectrics. During the turn-on period of inductive switching measurement, two sections of dV_{DS}/dt with a turning point around 10 V are observed for the presence of D-mode portion in C_{GD}, leading to a longer switching transfer and higher switching power loss.

Acknowledgements

This work was supported in part by the National Natural Science Foundation of China under Grant 61822407, Grant 61527816, Grant 11634002, Grant 61631021, Grant 62074161, Grant 62004213, and Grant U20A20208; in part by the Key Re-

search Program of Frontier Sciences, Chinese Academy of Sciences (CAS) under Grant QYZDB-SSW-JSC012; in part by the Youth Innovation Promotion Association of CAS; in part by the University of CAS; and in part by the Opening Project of Key Laboratory of Microelectronic Devices & Integrated Technology, Institute of Microelectronics, CAS.

References

[1] Boutros K S, Chu R M, Hughes B. GaN power electronics for automotive application. 2012 IEEE Energytech, 2012, 1
[2] Piedra D, Lu B, Sun M, et al. Advanced power electronic devices based on gallium nitride (GaN). 2015 IEEE International Electron Devices Meeting, 2015, 16.6.1
[3] Kizilyalli I C, Xu Y A, Carlson E, et al. Current and future directions in power electronic devices and circuits based on wide band-gap semiconductors. 2017 IEEE 5th Work Wide Bandgap Power Devices Appl, 2017, 417
[4] Chen K J, Häberlen O, Lidow A, et al. GaN-on-Si power technology: Devices and applications. IEEE Trans Electron Devices, 2017, 64, 779
[5] Saito W, Nitta T, Kakiuchi Y, et al. Suppression of dynamic on-resistance increase and gate charge measurements in high-voltage GaN-HEMTs with optimized field-plate structure. IEEE Trans Electron Devices, 2007, 54, 1825
[6] Chu R M, Corrion A, Chen M, et al. 1200-V normally off GaN-on-Si field-effect transistors with low dynamic on -resistance. IEEE Electron Device Lett, 2011, 32, 632
[7] Ma X B, Zhang J C, Guo L L, et al. Effects of passivation and FP structure on current collapse in an AlGaN/GaN HEMT. Chin J Semicond, 2007, 28, 73
[8] Lei Y, Lu H. Influence of field plate on surface-state-related lag characteristics of AlGaN/GaN HEMT. J Semicond, 2015, 36, 074007
[9] Meneghesso G, Bisi D, Rossetto I, et al. Reliability of power devices: Bias-induced threshold voltage instability and dielectric breakdown in GaN MIS-HEMTs. 2016 IEEE Int Integr Reliab Work, 2016, 35
[10] Zhao R, Huang S, Wang X H, et al. Interface charge engineering in down-scaled AlGaN (<6 nm)/GaN heterostructure for fabrication of GaN-based power HEMTs and MIS-HEMTs. Appl Phys Lett, 2020, 116, 103502
[11] Yang S, Tang Z K, Hua M Y, et al. Investigation of SiN_x and AlN passivation for AlGaN/GaN high-electron-mobility transistors: Role of interface traps and polarization charges. IEEE J Electron Devices Soc, 2020, 8, 358
[12] Viey A G, Vandendaele W, Jaud M A, et al. Investigation of nBTI degradation on GaN-on-Si E-mode MOSc-HEMT. 2019 IEEE International Electron Devices Meeting, 2019, 4.3.1
[13] Huang S, Liu X, Wang X, et al. Ultrathin-barrier AlGaN/GaN heterostructure: a recess-free technology for manufacturing high-performance GaN-on-Si power devices. IEEE Trans on Electron Devices, 2018, 65, 207
[14] Huang S, Wang X H, Liu X Y, et al. Monolithic integration of E/D-mode GaN MIS-HEMTs on ultrathin-barrier AlGaN/GaN heterostructure on Si substrates. Appl Phys Express, 2019, 12, 024001
[15] Huang S, Liu X Y, Wang X H, et al. High uniformity normally-OFF GaN MIS-HEMTs fabricated on ultra-thin-barrier AlGaN/GaN heterostructure. IEEE Electron Device Lett, 2016, 37, 1617
[16] Guo F Q, Huang S, Wang X H, et al. Suppression of interface states between nitride-based gate dielectrics and ultrathin-barrier AlGaN/GaN heterostructure with *in situ* remote plasma pretreatments. Appl Phys Lett, 2021, 118, 093503

Lan Bi got his MS degree from the Institute of Electrons, Chinese Academy of Sciences, Beijing. Now he is a PhD student at the Institute of Microelectronics, Chinese Academy of Science. His research focuses on fabrication and monolithic integration of GaN devices.

Qimeng Jiang received his PhD degree from The Hong Kong University of Science and Technology, Hong Kong, China, in 2015. He is currently a professor with the Institute of Microelectronics, Chinese Academy of Sciences, Beijing. His current research interests include advanced design and fabrication technologies for power semiconductor devices and ICs.

Sen Huang received his PhD degree from Peking University, Beijing, China, in 2009. He is currently a professor with the Institute of Microelectronics, Chinese Academy of Sciences, Beijing. His current research interests include advanced design, fabrication, and characterization technologies for III–V power semiconductor devices.