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An integrated front-end vertical hall magnetic sensor fabricated in 0.18 μm low-voltage CMOS technology

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Abstract: An integrated front-end vertical CMOS Hall magnetic sensor is proposed for the in-plane magnetic field measurement. To improve the magnetic sensitivity and to obtain low offset, a fully symmetric vertical Hall device (FSVHD) has been optimized with a minimum size design. A new four-phase spinning current modulation associated with a correlated double sampling (CDS) demodulation technique has been further applied to compensate for the offset and also to provide a linear Hall output voltage. The vertical Hall sensor chip has been manufactured in a 0.18 μm low-voltage CMOS technology and it occupies an area of 1.54 mm^2. The experimental results show in the magnetic field range from –200 to 200 mT, the entire vertical Hall sensor performs with the linearity of 99.9% and the system magnetic sensitivity of 1.22 V/T and the residual offset of 60 μT. Meanwhile, it consumes 4.5 mW at a 3.3 V supply voltage. The proposed vertical Hall sensor is very suitable for the low-cost system-on-chip (SOC) implementation of 2D or 3D magnetic microsystems.

Key words: vertical Hall sensor; dynamic offset cancellation; 1/*f* noise; residual offset

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1. Introduction

Due to their full compatibility with CMOS technologies, Hall sensors have been widely applied in many different fields such as industrial control systems, computers, automobiles, and consumer electronics, where magnetic field detection or contactless measurement are required[1–4]. For instance, in the automobile, there is a heavy user of Hall magnetic sensors in the applications of anti-lock braking systems (ABS), pedal position sensor, non-contacting potentiometer, etc. Generally, CMOS Hall sensors adopt integrated horizontal Hall plates as sensing devices, which are capable of detecting the magnetic field component orthogonal to the device surface[5–6]. However, in many applications such as tracking systems in MRI surgery tools[7] or position measurement in automobiles, there is a growing demand for the detection of three-dimensional (3D) magnetic field components[8, 9]. Therefore, the vertical Hall devices (VHDs), which are sensitive to the magnetic field components parallel to the device surface are needed and technical solutions have been proposed to achieve this request[10]. Nowadays, VHDs provide a cost-optimized system-on-chip (SoC) solution for 2D or 3D Hall sensors. Meanwhile, the area, power consumption, and circuit complexity are much reduced.

In the past few decades, many attempts of fabricating vertical Hall sensors have been undertaken[11–18]. However, it is difficult to realize highly sensitive VHDs in low-cost, low-voltage CMOS technologies. Due to their inherent topology built-in planar CMOS technologies, VHDs are subjected to short circuit effect, which seriously degrades their sensitivity[11, 12]. Especially in advanced CMOS technologies, the shallow diffusion layers and high doping levels of the N-wells cause the input bias current to flow easily through the surface contact regions, leading to extremely low sensitivity. To mitigate this short circuit effect, high-voltage (HV) CMOS technologies with a special low-doped deep n-diffusion layer (NTUB) are developed to manufacture VHDs[13]. However, it will inevitably increase the additional fabrication cost. Moreover, offset is quite difficult to get rid of it on VHDs due to the lack of electrical symmetry structure such as traditional five-contact devices[14]. The offset voltage is often much larger than the Hall voltage, making it difficult for VHDs to detect low magnetic fields. The offset is also sensitive to temperature variations, thermally drifting in a low-frequency range. At present, the fully symmetric vertical Hall device (FSVHD) is suggested to reduce the offset of the VHDs. The four-folded and three-contact VHD structure is a good solution[16–18], nevertheless, its sensitivity still needs to be improved. Besides, the low-frequency 1/*f* noise is also an issue for CMOS VHDs. The noise power spectral density of VHDs shown in Fig. 1 reveals that the 1/*f* noise is significantly higher than the thermal noise in the low-frequency band, which is within the bandwidth of the target signals. Indeed, the high 1/*f* noise figures combined with the low magnetic sensitivity and large offset limit the resolution and accuracy in the actual magnetic field measurements.

To effectively remove the offset and 1/*f* noise of Hall devices, the dynamic offset cancellation technique has been broadly adopted[19]. The two-phase spinning current (SC) technique has proven very efficient for the offset cancellation on the horizontal Hall devices (HHDs)[19–22], but, it is not effective to VHDs because of the intrinsic asymmetric device structure. The four-phase SC technique has also been applied to CMOS VHDs, showing the better ability to eliminate

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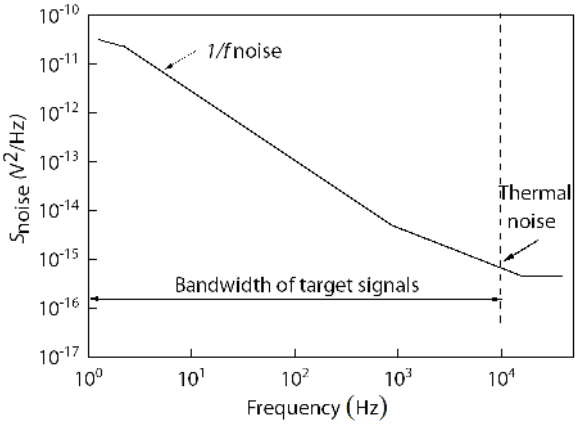

Fig. 1. Schematic diagram of the noise power spectral density of VHDs.

offset[23–24]. For example, an offset compensation-oriented four-phase SC technique was implemented in the Hall sensors for broadband current sensing by using a novel front-end circuit architecture[23]. A four-phase bi-current SC technique was proposed to remove offset and lower 1/*f* noise, allowing to obtain the maximum sensitivity and to enhance the resolution of the VHD designed in low-voltage CMOS technologies[24]. For a Hall sensor microsystem, it is highly expected for a very small residual offset and a high magnetic field resolution. Therefore, a robust four-phase SC modulation circuit and the corresponding demodulation circuit should be considerably implemented to effectively remove the large offset and noise and meanwhile maintain the optimal sensitivity for VHDs.

In our work, a magnetic sensor microsystem integrated with a VHD has been implemented in a 0.18 μm low-voltage CMOS technology. The structure of an FSVHD is optimized for sensitivity improvement and noise reduction. A new four-phase SC circuit and its corresponding modulated circuit are proposed to effectively cancel Hall offset and linearly amplify the Hall signal. The experimental results show that the vertical Hall microsystem can achieve high system sensitivity, low residual offset, and high linearity, indicating that it is very suitable for a low-cost 2D or 3D Hall sensor microsystem.

2. Hall microsystem design

The block diagram of the proposed vertical Hall sensor is depicted in Fig. 2, which consists of a vertical Hall device, a spinning current (SC) switch box, an instrumentation amplifier (INA), a correlated double sampling (CDS) circuit, a sample/hold (S/H) adder, a low-pass filter (LPF), and a clock generator. The operating principle of the front-end Hall microsystem is described as follows. Firstly, the output Hall signals of the VHD are modulated to high frequency under the control of the four-phase SC switches. Then, the differential Hall signals proportional to the changing magnetic field are amplified by the instrumentation amplifier. After that, the CDS and S/H adder cancel the offset and 1/*f* noise of the VHD and demodulate the Hall signal back to the low frequency at the same time. Finally, the low pass filter removes high-frequency harmonic components and outputs Hall signals with the low residual offset.

2.1. Vertical Hall device

The optimization of the VHDs is based on a fully symmetric topology[17, 18]. Fig. 3(a) schematically shows the cross-section of the fully symmetric vertical Hall device (FSVHD) that is realized in low-voltage CMOS technology. The FSVHD consists of four identical three-contact vertical Hall elements (3CVHE) built on the p-type substrate in a closed-loop connection[17, 18]. Each 3CVHE element comprises a low-voltage n-well (NW), two P+, and three N+ diffusion regions. These diffusion stripes are arranged on the surface of the n-wells. The N+ stripes on both sides of each 3CVHE realize the interconnection of the individual 3CVHE, while the four central N+ stripes are used as the drive and sense terminals (a, b, c, d) respectively. As shown in Fig. 3(b), the path of internal current flowing is the same in the four operating modes. This electrical symmetry is fully similar to that of the planar Hall plate, hence it is very fit for the application of the four-phase SC offset cancellation technique. It is interesting to note that the miniaturization of the VHDs is an effective method to enhance sensitivity and reduce noise. To increase the sensitivity and signal-to-noise ratio, the design is optimized based on the device miniaturization though it may introduce a larger offset. For the two side N+ contacts, they have no obvious effect on Hall current because they just act as the signal transmission nodes. The geometry, such as the position and size of the central N+ contact, as well as the distance between two N+ contacts, will have an important influence on FSVHD performance. To investigate the effect, two variables, namely, the width of central N+ contacts (L_n) and the distance between the two adjacent N+ contacts (L_d) are selected. We will optimize the sensitivity of the FSVHD by analyzing the effect of each variable based on TCAD simulation.

A two-dimensional device simulation of the FSVHD has been implemented in 0.18-μm standard CMOS technology utilizing the Silvaco Atlas tool. Appropriate models, such as the magnetic model, Shockley–Read–Hall recombination, low-field mobility, etc., are applied in the TCAD simulation. Firstly, the influence of the width (L_n) of the central N+ contacts on the sensitivity was simulated at the fixed distance (L_d) between the central and the two side N+ contacts. Fig. 4(a) compares the voltage-related sensitivity of the FSVHD as a function of bias voltage for three different sizes of Ln when a magnetic field of 0.1 T is applied. It is found that at the bias of 2 V, the sensitivity is reduced from 0.9 %/T to 0.68 %/T when the width of L_n is increased from 0.42 to 0.8 μm. This is because for the central N+ sense contact, the smaller the width, the higher the geometry factor, leading to the larger sensitivity. Limited by the design rule of the 0.18 μm CMOS technology, the minimum width of the central N+ implantation is only allowed to be 0.42 μm, thus, it is designed to be 0.42 μm for maximum sensitivity. Secondly, the distance (L_d) is changed from 0.8 to 2.1 μm to investigate the variation of the sensitivity when the width of L_n is fixed at 0.42 μm. Fig. 4(b) shows the voltage-related sensitivity as a function of bias voltage at three different distances of L_d. It is seen that the shorter L_d leads to higher sensitivity, which is due to the reduction of the short circuit effect of the FSVHDs. Consequently, the central N+ contacts need to be as close to the two side N+ contacts as possible. However, the shorter distance L_d will lead to a larger offset. Considering the offset limit, the distance L_d is selected to 1.5 μm, not the minimum size.

2.2. Four-phase spinning current switches

To better eliminate the offset and 1/*f* noise of the FSVHD,

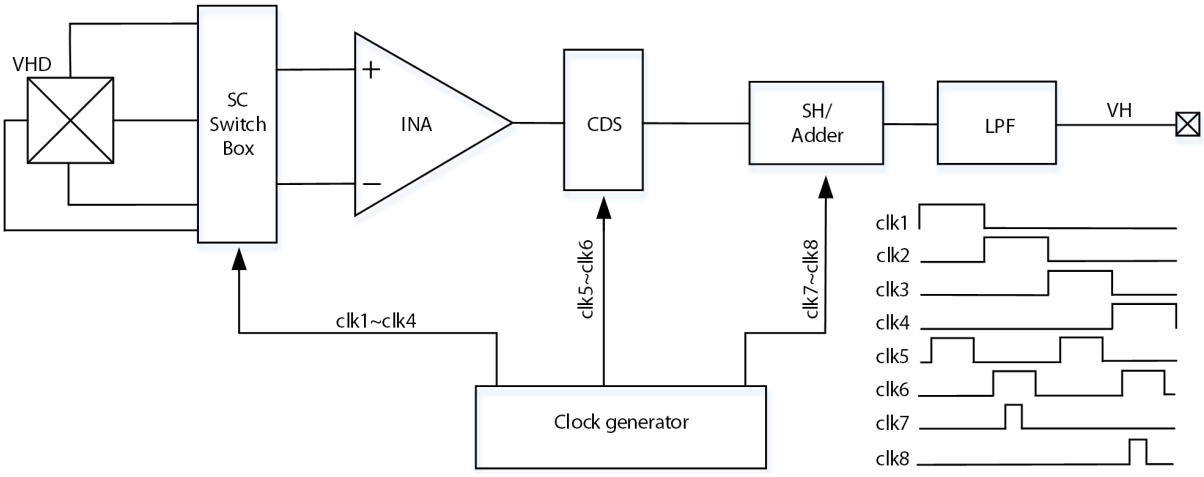

Fig. 2. The block diagram of the proposed vertical Hall sensor.

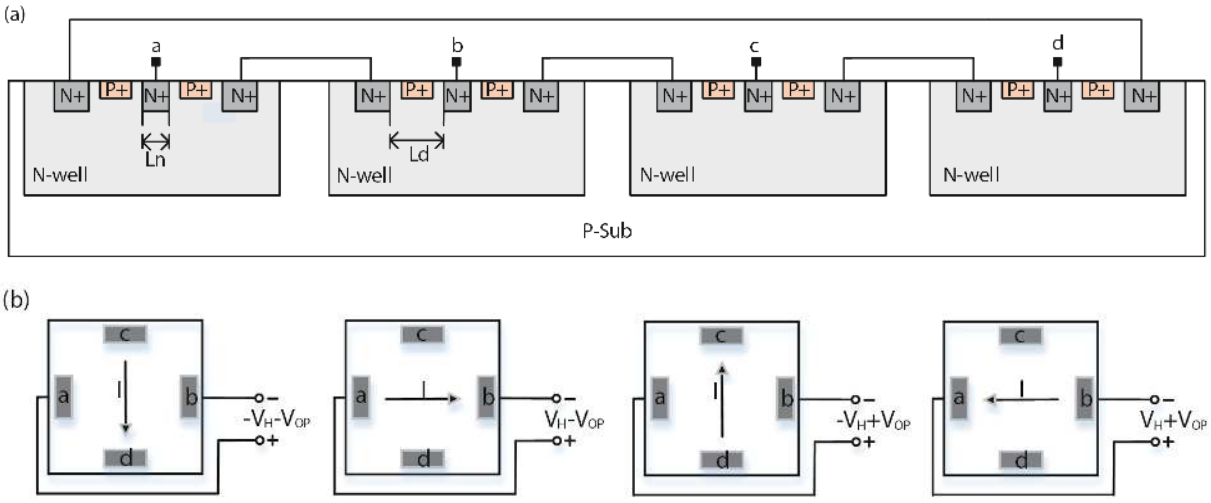

Fig. 3. Schematic of (a) the FSVHD consisting of four interconnected 3CVHEs and (b) the four operating modes in the four-phase spinning technique.

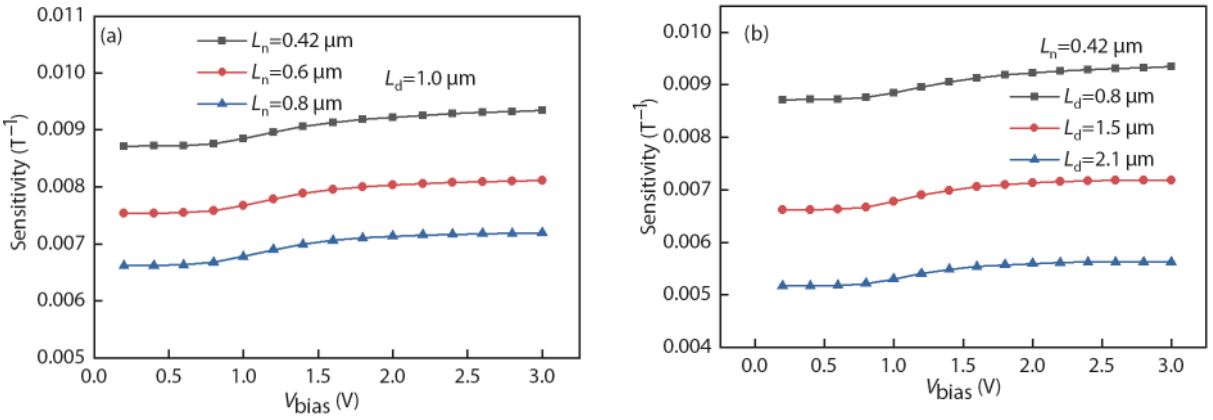

Fig. 4. (Color online) TCAD simulation results for the FSVHD sensitivity. Sensitivity as a function of (a) L_n and (b) L_d.

a novel four-phase SC circuit that consists of 16 NMOS switches is proposed in Fig. 5(a). The SC circuit is based on the periodic interchangeability of the biasing and sensing terminals of the FSVHD under the control of four-phase sequential clocks, enabling the polarity change of Hall voltage and offset, as depicted in Fig. 5(b). When clk_1 and clk_2 go high successively, the polarity of the output Hall voltage changes periodically, while the polarity of the offset voltage remains unchanged[23]. Therefore, the output voltages in the first two-phase SC are given by

$$V(0^\circ) = -V_H - V_{OP1}, \quad (1)$$

$$V(90^\circ) = V_H - V_{OP2}, \quad (2)$$

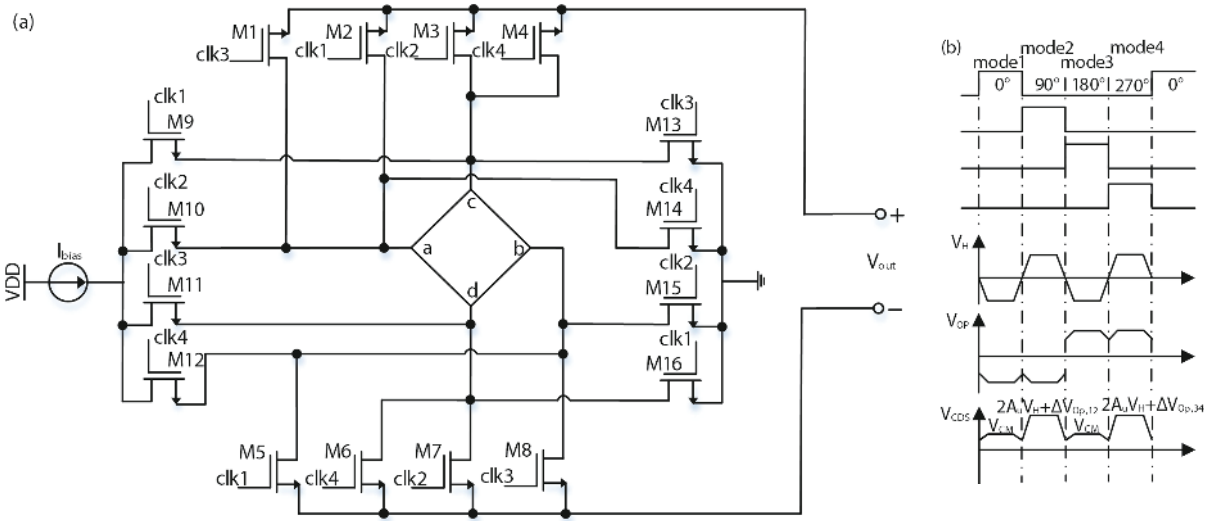

Fig. 5. Schematic diagram of (a) the switched vertical Hall device using four-phase spinning current operation and (b) the output Hall voltage and offset voltage corresponding to the four-phase sequence clocks.

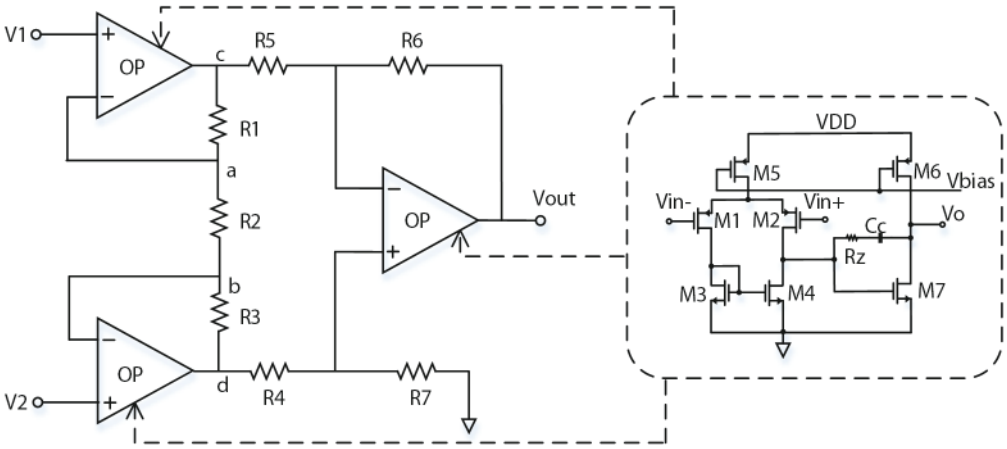

Fig. 6. The schematic diagram of the bridge instrumentation amplifier.

where the V_H and V_{OP} are the Hall and offset voltages of the FS-VHD, respectively.

Similarly, when clk_3 and clk_4 turn high in the order, the FS-VHD is operated in the second two-phase SC stage. The polarity change of the output Hall voltage is the same as that in the first two-phase SC stage. Note that the polarity of the offset voltage is not changed in the second two-phase SC, but it is the opposite of the first two-phase SC. The output voltage can be expressed as

$$V(180^\circ) = -V_H + V_{OP3}, \tag{3}$$

$$V(270^\circ) = V_H + V_{OP4}. \tag{4}$$

It can be seen that after the four-phase SC modulation, the output Hall voltage can be distinguished from the offset voltage, which facilitates subsequent dynamic offset elimination.

2.3. Signal conditioner

After four-phase SC modulation, the mixing signals including Hall and offset voltages are input into the instrumentation amplifier for magnitude amplification. Fig. 6 schematically shows the bridge instrumentation amplifier configuration with resistive voltage feedback and three same two-stage operational amplifiers (op-amps). Among them, the op-amp adopts a two-stage amplifier with a PMOS differential input pair, which enables the circuit to work normally at a lower common-mode level, and it also has a high ability to suppress common-mode interference signals.

The amplified signals are then demodulated by the correlated double sampling (CDS) circuit, the S/H, and the adder, as shown in Fig. 7. The inset of Fig. 5(b) schematically shows the output waveform of the CDS circuit. When the clk_5 and clk_6 are high, respectively, the mixed input signals corresponding to the first and the second SC stages are sampled twice, and then we can obtain the CDS output voltage that equals the second sampling value minus the first sampling value:

$$V_{CDS1} = A_u\left[V(90^\circ) - V(0^\circ)\right] = 2AV_H + \Delta V_{OP,12}, \tag{5}$$

where the A_u denotes the total voltage gain of the front-end vertical Hall sensor, and $\Delta V_{OP,12} = A_u(V_{OP1} - V_{OP2})$.

In the same way, when the input signals corresponding to the third and fourth SC stages are sampled by the CDS circuit, we can also obtain:

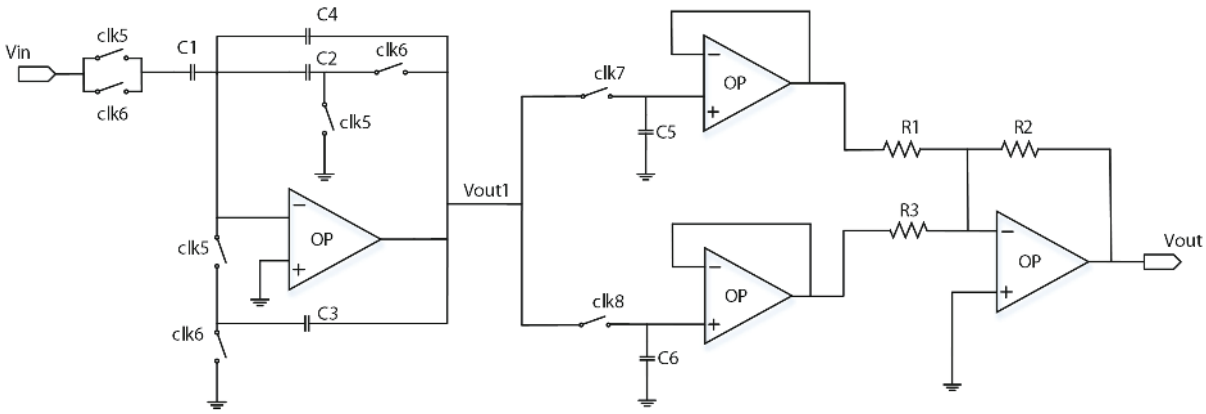

Fig. 7. The schematic diagram of the CDS demodulation circuit.

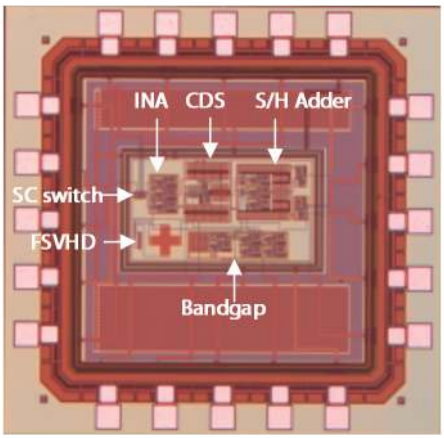

Fig. 8. (Color online) Hall sensor microphotograph: whole chip including pads with an active area with the back-annotated layout of main circuital blocks.

$$V_{CDS2} = A_u\left[V\left(270^\circ\right) - V\left(180^\circ\right)\right] = 2AV_H + \Delta V_{OP,34}, \quad (6)$$

where $\Delta V_{OP,34} = A_u(V_{OP4} - V_{OP3})$.

Next, under the control of the clk_7 and clk_8, the output signals of the CDS circuit are sampled and maintained by two S/H circuits. The output voltages of the CDS are fed into the adder to obtain the final Hall output voltage:

$$V_{out} = V_{CDS1} + V_{CDS2} = 4A_uV_H + \Delta V_{OP}. \quad (7)$$

Here, $\Delta V_{OP} = A_u(V_{OP1} - V_{OP2} - V_{OP3} + V_{OP4})$, which determines the residual offset of the Hall sensor.

Since the offset voltages from two S/H circuits have the opposite polarity, the offset and $1/f$ noise can be further eliminated by the add operation. Finally, a low residual offset is obtainable, meanwhile, the spectrum of the Hall signal is demodulated back to the baseband.

3. Measurement results and discussions

The prototype of the proposed vertical Hall sensor was fabricated in a low-voltage 0.18 μm 2-poly 6-metal CMOS technology. Fig. 8 displays the micrographs of the sensor chip, which occupies 1.24 × 1.24 mm^2, including the I/O pads and coupling capacitors.

The performance of the vertical Hall sensor was measured by applying a magnetic field parallel to the chip. Fig. 9 shows the experimental setup for the sensor microsystem, which consists of a Gauss meter, a high-precision nano voltmeter, a semiconductor parameter analyzer, a magnetic field generator, and a power supply. The linear magnetic field is produced by a magnetic field generator driven by a power supply. After bonding, the vertical Hall devices and sensor chip were placed in the center of the magnetic field generator where the magnetic field intensity was calibrated by a Gaussian meter. Firstly, the offset voltage and the noise power spectral density of FSVHDs were tested without applying a magnetic field. Then, the Hall voltage of FSVHDs was measured in the magnetic field range from 0 to 200 mT by adjusting the output current of the power supply. Here, the Hall voltage including offset was tested by the high-precision nano voltmeter, and the noise of the FSVHD was characterized by the FS-PRO semiconductor parameter analyzer. Finally, the front-end vertical Hall microsystem response to a magnetic field was measured. The four-phase sequential clocks and the CDS sampling clocks required for the vertical Hall sensor chip were provided by an external FPGA development board. Under the control of the four-phase sequential clocks, the four-phase SC box outputs modulated signals, including Hall, and offset voltages with different polarities. After the mixed signals are amplified by the instrumentation amplifier, they are sampled during the second and fourth SC stages by the CDS demodulated circuit, respectively, and then the two sampled voltages are summed by the adder. As a result, the Hall voltage is demodulated back to the low-frequency signal, meanwhile, the offset and $1/f$ noise are dynamically removed and a low residual offset can be achieved.

Fig. 10 illustrates the output Hall voltage of the optimized FSVHD (L_n = 0.42 μm and L_d =1.5 μm) as a function of the magnetic field at a bias of 2 V. It is found that the output Hall voltage is linearly increased with the magnetic field intensity in the range from 0 to 100 mT. At the magnetic field of 100 mT, the measured Hall voltage of the optimized FSVHD is about 1.415 mV, thus the voltage-related sensitivity is calculated as 0.71 %/T. By comparison, the initial FSVHD without optimization with a larger size (L_{n2} = 0.6 μm and L_d = 2.89 μm) has a lower sensitivity of 0.46 %/T. It is indicated that the miniaturization of the device is very helpful to improve the sensitivity of the FSVHD.

Fig. 11(a) illustrates the offset of the optimized FSVHDs operated at the four-phase spinning current modes. It is found that the offset voltages increase with the bias voltage. The offset voltages at mode 1 and mode 3 are electronically symmet-

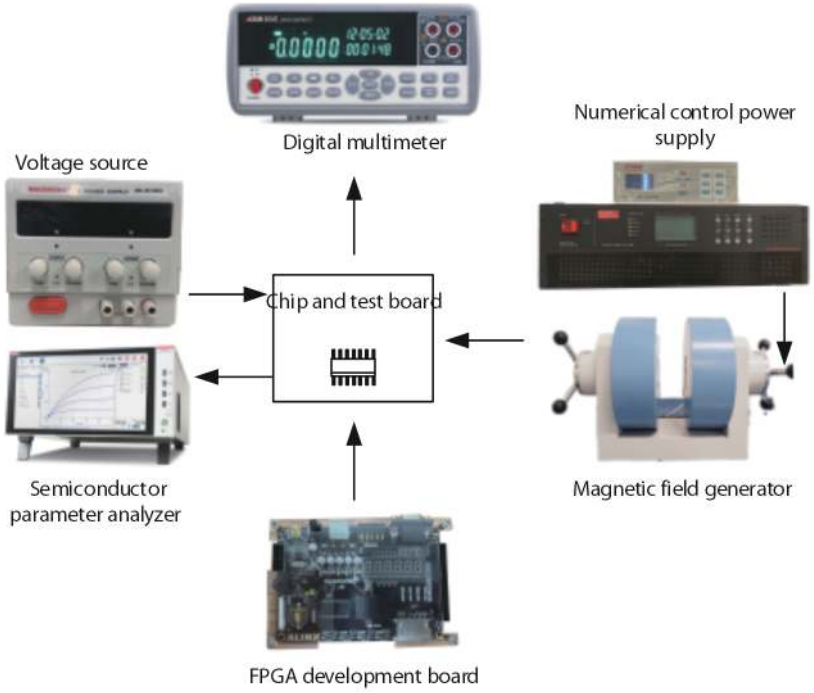

Fig. 9. (Color online) Experimental setup.

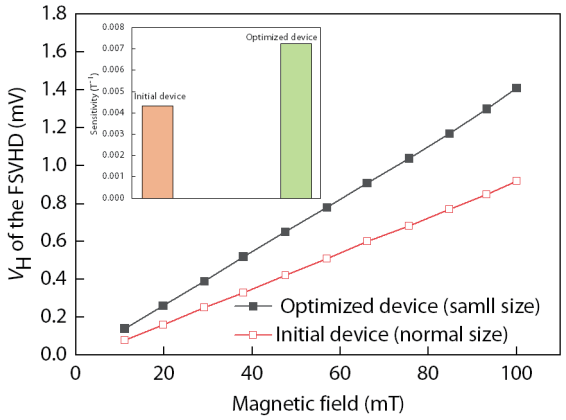

Fig. 10. (Color online) Test Hall voltages as a function of in-plane magnetic field for two FSVHDs. The inset picture shows the voltage-related sensitivity of two FSVHDs.

rical. Similarly, modes 2 and 4 also have symmetrical offset voltages. At the bias of 2 V, the absolute value of the initial offset is about 3 mV, but the mean offset is only 15 μV for the four modes. Therefore, the four-phase SC technique can effectively eliminate the offset of the FSVHD. The measurement results of the noise power spectrum are illustrated in Fig. 11(b). The presented FSVHD shows dominating 1/f noise at low frequencies. It is observed that the 1/f noise level is increased with the bias voltage and the corner frequency quickly shifts to higher values. At the bias of 0.6 V, the corner frequency is about 100 kHz. As the bias is increased to 2 V, it is moved to about 1 MHz. In fact, at the 1 MHz corner frequency, the 1/f noise is reduced to a small level of 2 nV/$\sqrt{\text{Hz}}$. The 1/f noise of the device can also be removed by the SC technique[19, 24].

Fig.12 shows the output Hall voltage versus magnetic field amplitude for the front-end vertical Hall sensor chip. The Hall output voltage is linearly increased with the magnetic field. The linearity reaches 99.9% in the magnetic field range from −200 to 200 mT and the sensor system sensitivity was determined to be 1.22 V/T. Thanks to the application of the four-phase SC modulation and a CDS demodulation technique, a low residual offset of 60 μT is obtained. In contrast, the residual offset is larger than 200 μT in the vertical Hall sensor using the conventional two-phase SC technique. Additionally, the 1/f noise at low frequency is also reduced by a factor of 5 compared with the vertical Hall sensor without the application of the four-phase SC method.

Table 1 summarizes the principal characteristics of this work compared to the state of the art[2, 24–26]. The front-end Hall microsystem exhibits outstanding advantages of low residual offset, high linearity, and low power consumption. Unlike the other reported four-phase SC offset cancellation technique[23, 24], the applied four-phase SC modulation circuit works in conjunction with the CDS modulation circuit. The output signals of the four-phase SC circuit are sampled twice by the CDS circuit, respectively, and finally, the offset voltages corresponding to four-phase SC stages are subtracted from each other through the adder. The tested low residual offset of 60 μT proves the strong ability to eliminate offset originating from the Hall device and electronics. Moreover, the proposed dynamic offset cancellation circuit has simpler structures, which are easily implemented. Also, the vertical Hall sensor microsystem achieves a very low nonlinearity of 0.1 %, which is due to the adoption of the new signal conditioner based on the bridge instrumentation amplifier and CDS circuit. In addition, the low static power dissipation of 4.5 mW is obtainable under the supply voltage of 3.3 V and the working bandwidth is up to about 30 kHz.

4. Conclusions

A front-end CMOS vertical Hall sensor microsystem fabricated in a low-voltage 0.18 μm CMOS technology has been presented. A fully symmetric vertical Hall device (FSVHD) with a minimum size design has been optimized to increase the

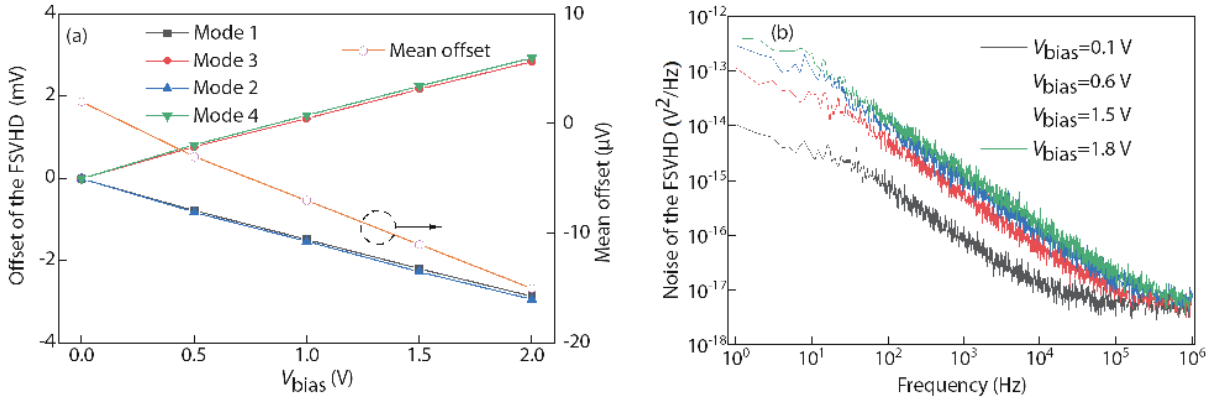

Fig. 11. (Color online) Tested results of the optimized FSVHD. (a) Offset as a function of bias voltage and (b) 1/*f* noise at the various bias voltages.

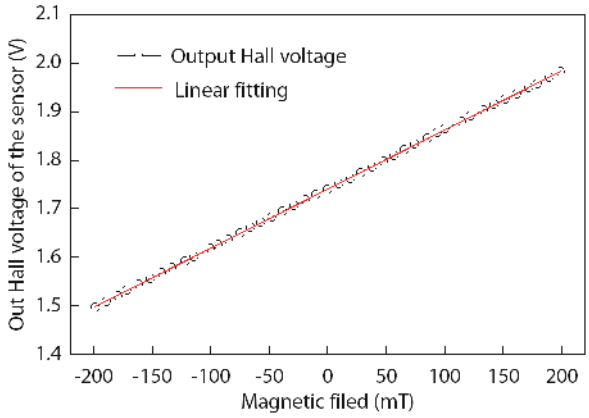

Fig. 12. (Color online) Measured differential output voltages of the vertical Hall sensor as a function of a magnetic field.

Table 1. Performance Summary and Comparison Table of This Work With The Reported Ones.

Reference	This work	Ref. [2]	Ref. [24]	Ref. [25]	Ref. [26]
CMOS technology	0.18 μm	0.35 μm	0.35 μm	0.18 μm	0.18 μm
Sensor type	VHD	HHD	VHD	HHD	HHD
Supply voltage (V)	3.3	3.3	3.3	5	1.8
System sensitivity	1.22 V/T	50 mA/T	1.67 V/T	11 V/T	19.9 V/T
Spinning frequency (kHz)	100	20	10	–	250
Measurement range (mT)	200	40	–	300	10
Chip area (mm^2)	2.3	11.55	–	5.29	1.16
Residual offset (μT)	60	50	–	270	50
Linearity (%)	99.9	99.9	–	98.3	>99.8
Bandwidth (kHz)	30	500	1.6	30	10
Static power (mW)	4.5	40	2.72	50	0.12

magnetic sensitivity and to reduce the offset and noise. The new four-phase SC modulation technique and the CDS demodulation technique are employed to dynamically remove the device offset and 1/*f* noise. The test results reveal that the sensor sensitivity is 1.22 V/T, and the residual offset is less than 60 μT and the output Hall voltage linearity is up to 99.9% in the magnetic field range from –200 to 200 mT. Therefore, the presented vertical Hall sensor is very suitable for the low-cost system-on-chip (SOC) integration of 2D or 3D magnetic sensors.

Acknowledgements

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