REVIEWS

Journal of Semiconductors
(2022) 43, 023101
doi: 10.1088/1674-4926/43/2/023101

A review of compact modeling for phase change memory

Feilong Ding[1], Baokang Peng[1], Xi Li[2], Lining Zhang[1, †], Runsheng Wang[3], Zhitang Song[2], and Ru Huang[3]

[1]School of Electronic and Computer Engineering, Peking University, Shenzhen 518055, China

[2]Shanghai Institute of Micro-System and Information Technology, Chinese Academy of Sciences, Shanghai 200050, China

[3]Institute of Microelectronics, Peking University, Beijing 100871, China

Abstract: Phase change memory (PCM) attracts wide attention for the memory-centric computing and neuromorphic computing. For circuit and system designs, PCM compact models are mandatory and their status are reviewed in this work. Macro models and physics-based models have been proposed in different stages of the PCM technology developments. Compact modeling of PCM is indeed more complex than the transistor modeling due to their multi-physics nature including electrical, thermal and phase transition dynamics as well as their interactions. Realizations of the PCM operations including threshold switching, set and reset programming in these models are diverse, which also differs from the perspective of circuit simulations. For the purpose of efficient and reliable designs of the PCM technology, open issues and challenges of the compact modeling are also discussed.

Key words: phase change memory; compact model; macro model; physics-based model

Citation: F L Ding, B K Peng, X Li, L N Zhang, R S Wang, Z T Song, and R Huang, A review of compact modeling for phase change memory[J]. *J. Semicond.*, 2022, 43(2), 023101. http://doi.org/10.1088/1674-4926/43/2/023101

1. Introduction to PCM and its modeling

Phase change memory[1–3] has been one important non-volatile memory among several emerging technologies such as RRAM, MRAM and FeRAM, etc. It relies on the switching between amorphous state (high resistance) and crystalline state (low resistance) for memory applications. In general, phase change memory (PCM) is one type of memristor. The need to handle massive amount of data in the era of big data drives the extensive research and developments of these memory technologies. Among various applications, the storage-class-memory (SCM)[4] calls for candidates with high capacity and high band-width to fill the gap between DRAM and NAND Flash in the state-of-the-art memory hierarchy. PCM is one of the strong candidates for SCM applications[1, 3].

As of today, PCM has entered the market of standalone memory, for example the 3D XPoint memory by Intel[5, 6] and embedded non-volatile memory (eNVM), for example, that of STMicroelectronics[7–9]. This comes from years of research and development all around the world. The original concept of phase change memory was proposed early in 1970s[10]. With the success of phase change material $Ge_2Sb_2Te_5$ in the optical storage, utilizing the phase change material for electrical storage revived in later 1990s[11]. Several milestones in the process include the mushroom-type PCM realized with 180 nm CMOS technology[12], the line type PCM with 90 nm technology node[13], the embedded 90 nm 1 transistor 1 resistor PCM technology[14], the dash-type confined PCM with sub-20 nm technology[15], and the stackable cross point PCM with the Ovinic threshold switching (OTS) selector[5], and the two-deck cross point PCM for 128 Gb SCM[16]. With the advancement of technology scaling and material innovations, the state-of-the-art PCM features $4F^2$ cell area, tens of nanoseconds set time, 100 μA reset current, 10^{12} endurance cycles, 10 years' retention at temperatures higher than 120 °C. Fig. 1 shows the schematics of two typical PCM cell structures: the mushroom type and the confinement type. Alternative applications of PCM are also emerging, such as the multi-level cell (MLC) and analog memories[17–20]. One key factor is to program the PCM into intermediate states between the highest resistance and lowest resistance states. Both SET and RESET processes could be utilized for this purpose. As it takes some time to complete the phase change process, intermediate states are then possible by partial phase changes[20]. The analog memory properties are being used to represent an electrical synapse with plasticity or an electrical neuron for neuromorphic computing[21–25] systems. In most cases, the PCM cells are connected together with CMOS devices, especially for realizations of the spiking neuron network.

Along with advancements of the PCM technology, their compact models had been playing important roles. Memory device models are needed for the same purpose of all other device models: to be used for circuit simulations. Although the memory cells are generally repeated in an array or a chip and the reading operation is more or less regarded as a single cell operation, a memory model is still necessary for the memory technology development[26]. A PCM cell works with a selector device to form the basic bit unit, and a simulation with models facilitates the device matching. The neighboring effects from adjacent PCM cells, as well as the parasitic effects, are accounted for in the model-based simulations. Further, the circuitry besides of the memory array including the sense amplifiers, are designed taking into consideration with the cell properties and the word/bit line voltage drops, etc. Memory reliability[27] is another concern that could be ad-

Correspondence to: L N Zhang, eelnzhang@pku.edu.cn
Received 24 AUGUST 2021; Revised 16 OCTOBER 2021.
©2022 Chinese Institute of Electronics

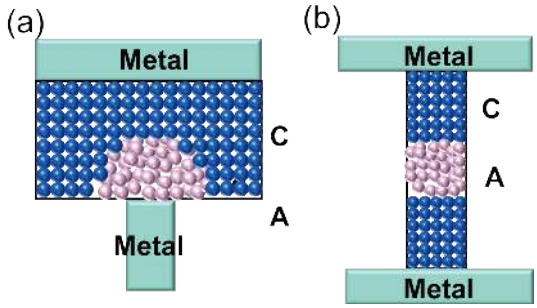

Fig. 1. (Color online) Schematics of two typical PCM cell structures: (a) the mushroom type and (b) the confinement type. In between the metal electrodes are the phase change materials, which show the crystalline phase (blue atoms in color) and amorphous phase (silver atoms in color).

dressed in circuit simulations with memory models. In the era of neuromorphic computing[28] with the analog phase change memories, the need for a compact memory model becomes even stronger. The model needs to reproduce not only the high/low resistance states, but also the intermediate states, the state transition time, their voltage dependence, and so on. Reproductions of these properties with the model allow evaluations of the analog cell characteristics, as well as the co-evaluations with the CMOS transistors for analog-type circuits. For advanced technologies, device-technology co-optimizations (DTCO) of the PCM-based computing applications are also essential. All these require a dedicated compact model supporting SPICE circuit simulations.

In this work we review compact models of the phase change memory. Device physics and principle operations as the basis of compact modeling are explained in Section 2. Then reported compact models of different categories from behavior macro models, to physics-based models with different approximations are reviewed in Section 3. Finally, further challenges on PCM modeling and our perspective are explained in Section 4.

2. Basic principle of PCM operations

There are three distinct states in the operations of PCM as shown in Fig. 2(a): the crystalline state (C), the amorphous state (A) and the melted liquid state (M), although only two of them (C and A) are possible at room temperature. The transition from state A to C is called crystallization. The transition from state C to A is not a direct process but via the state M, and is usually called amorphization. Fig. 2(b) shows the programing temperature for crystallization (also called SET) and amorphization (also called RESET). The SET process is triggered by increasing the temperature above the crystallization temperature (T_{cryst} or simply T_c). There are two possibilities in the process, a nucleation kinetics and a growth kinetics, that re-arrange atoms to form an ordered structure. The RESET process is triggered by increasing the temperature above the melting temperature (T_{melt} or simply T_m) and then quenching, i.e., decreasing the temperature within a short period. In the process the crystalline structure is melted with the chemical bonds broken, and the atoms re-arrange forming a disordered structure. For memory applications, the energy in the SET and RESET process comes from the Joule heat of the electrical pulse. Some further details in addition to the above essential ones of PCM operations are reported in excellent reviews[5, 29–31].

Another key property for the SET process is the threshold switching. It refers to an increase in the conductance after the voltage across the amorphous region reaches a critical value. Only with the threshold switching property, Joule heating for increasing the temperature above T_c happens with a reasonable voltage, which otherwise will be too large for applications. In the current–voltage curves, a snap-back is defined as the region with decreasing voltage and increasing current, i.e., a negative differential resistance. The threshold switching effect provides a dynamic resistance which is comparable to the crystalline resistance to enable the SET process. While the physics of threshold switching is still yet to be fully investigated, there are a few proposals such as a thermal model[33], an impact ionization model[34], and a thermal runaway model[35].

A popular theory for the crystallization is the classical nucleation and growth (CNG) theory[36, 37]. In this theory framework, the crystallization is composed of two processes: a nucleation process and a growth process, which have different temperature dependence. The nucleation pictures the formation of a nucleus with a critical size r_c: after the nucleus is larger than this size, it becomes stable and further grows without dissolution. As a result, the nucleation is indeed a stochastic process. With a surface energy γ, and a bulk free energy gain dg due to the supercooling, the energy of a nucleus with the critical size r_c is:

$$\Delta G = \frac{16}{3}\frac{\pi\gamma^3}{dg^2}. \tag{1}$$

The nucleation probability P_n[36, 38, 39] during a time interval Δt is then expressed with the activation energy at the surface E_{a1}:

$$P_n = \alpha\Delta t \exp\left[-\beta\left(E_{a1} + \Delta G\right)\right], \tag{2}$$

in which α is a frequency factor, $\beta = 1/(kT)$ with k the Boltzmann constant and T the temperature. Detailed derivations have been reported in the literature[39]. Fig. 3(a) plots a schematic energy diagram for the nucleation process.

A deterministic model, which can be regarded as a variant of the above probabilistic model, has a similar formulation of the phase transition rate[40] based on the maximum transition frequency r_0^N.

$$c_N = r_0^N \exp\left[-\beta\left(E_{a1} + \Delta G\right)\right]. \tag{3}$$

At the same time, the stabilized nucleus grows at any interface between the crystalline and amorphous. The growth is regarded as a combination of an atom diffusion Arrhenius process (with the activation energy E_{a2}) and a bi-directional process of liquid-solid transition. As a result, the growth velocity is given by[36, 39]:

$$v_g = fa_0\alpha\left[1 - \exp\left(-\beta\left|dg\right|\right)\right]\exp\left(-\beta E_{a2}\right), \tag{4}$$

in which a_0 is the atomic jump distance, and f is a temperature-dependent parameter. In the probabilistic picture, the growth probability during a time interval Δt is:

$$P_g = pa\Delta t\left[1 - \exp\left(-\beta\left|dg\right|\right)\right]\exp\left(-\beta E_{a2}\right), \tag{5}$$

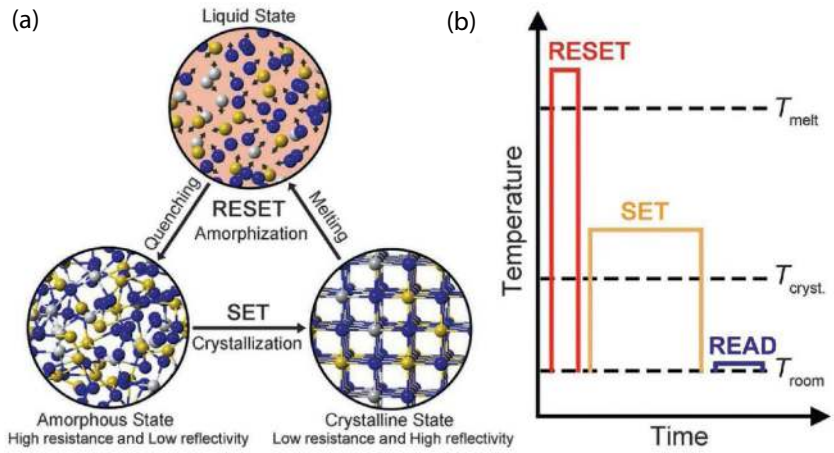

Fig. 2. (Color online) (a) Stable phase states and the atomistic structures. (b) The phase change dynamics with RESET/SET/READ pulses. Reprinted by permission from Springer Nature Customer Service Centre GmbH: Springer Nature MRS Bulletin, Phase-change materials in electronics and photonics, Wei Zhang *et al.*[32], 2019.

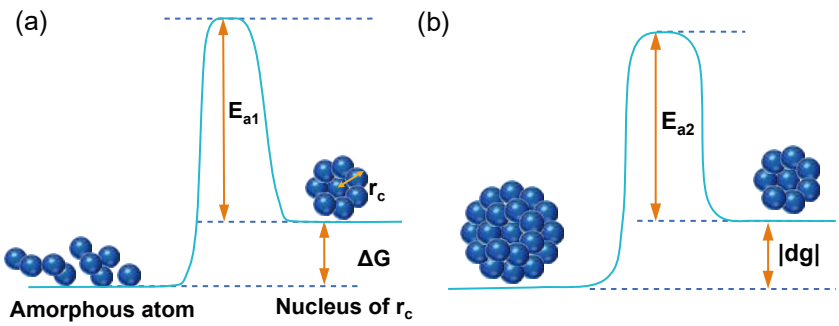

Fig. 3. (Color online) Schematic diagram of the crystallization from the energy perspective. (a) The nucleation is described as a process with energy barrier of E_{a1} plus the energy of nucleus ΔG with the critical size r_c. (b) The growth is described as a bi-directional process with a barrier of E_{a2} and a barrier of $|dg|$.

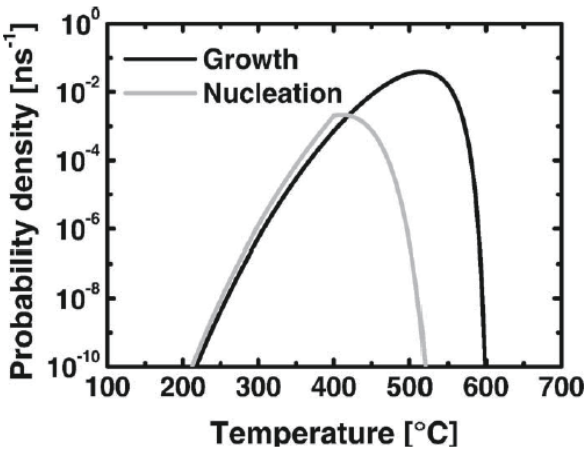

Fig. 4. Probability densities of nucleation and growth per nanosecond as given by the above CNG model. The bell-shaped characteristics have been widely used in PCM simulations in literature. Reprinted from Ref. [39], with the permission of AIP Publishing.

which is transformed from Eq. (4) with f replaced by an exponential factor, and p is a fitting parameter. Fig. 3(b) plots a schematic energy diagram for the growth process. Alternatively, the growth rate similar to the above nucleation rate is derived:

$$c_G = r_0^G \left[1 - \exp(-\beta |dg|)\right] \exp\left(-\beta E_{a2}\right), \tag{6}$$

in which r_0^G is the frequency factor.

The above Eqs. (2) and (5) have been used in a probabilistic framework[38], and Eqs. (3) and (6) have been used in a deterministic and local framework[40]. Fig. 4 plots the nucleation and growth rate which show peaks with non-monotonic temperature dependences.

Based on the CNG model, a phase space framework has been reported[40] covering all the three phases as shown in Figs. 5(a) and 5(b). At the same time, it is noted that the melting, either from crystalline state or amorphous state, is usually treated as a simultaneous process. When the temperature is raised above the melting temperature T_m, the state is transformed to molten state without a noticeable delay. This is reflected in the phase space framework as shown in Fig. 5(b) with sudden increases of the transition rates of A-to-M and C-to-M.

Another theory to describe the crystallization is the Johnson–Mehl–Avrami–Kolmogorov (JMAK) theory[41–43]. It assumes isothermal and isokinetic (same temperature dependence of nucleation and growth) conditions, and describes the transformed fraction $X(t)$:

$$X(t) = 1 - \exp\left[-(At)^n\right], \tag{7}$$

$$A(T) = w \exp\left(-\frac{E_a}{kT}\right), \tag{8}$$

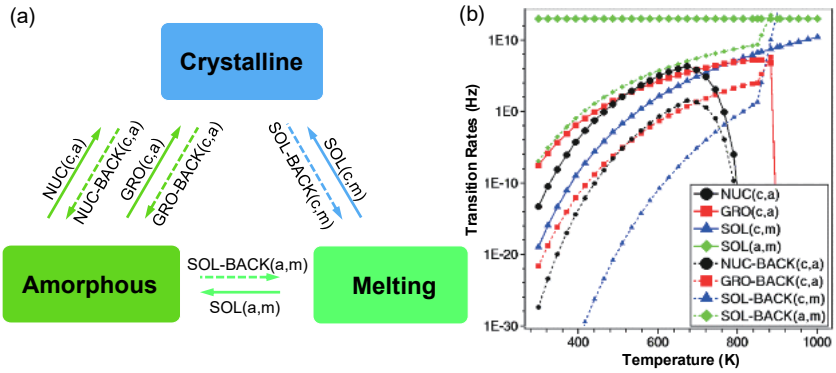

Fig. 5. (Color online) (a) Schematic diagram of three phases and their transitions and (b) dependence of the phase transition rates on temperature. © [2008] IEEE. Reprinted with permission from Ref. [40].

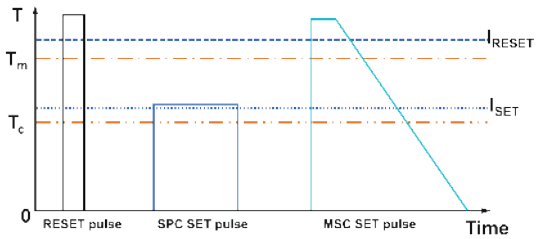

Fig. 6. (Color online) Schematic for the memory programing with desired temperature pulses. For a SET there can be two themes: a "solid phase crystallization" (SPC) and a "melting and slow cooling" (MSC). The slow cooling corresponds to a crystallization process below the melting temperature.

in which w is a frequency factor and n is the Avrami coefficient, E_a is the activation energy. The JMAK theory may be regarded as an approximation of the CNG theory in a specific temperature range.

The PCM state, either SET, partial SET or RESET, can be achieved by designing the melting and cooling (usually termed as quenching) process. The RESET to high resistance can be done by a "melting and fast cooling" process after melting the memory active region, as shown in Fig. 2. Noticing the quenching time-dependent chalcogenide atoms re-organizations, the SET to low resistance can be done by a "melting and slow cooling" (MSC) method[44]. It means by controlling the quenching time for atoms reorganizations partial or full SET states can be achieved. Fig. 6 also repeats the traditional "solid phase crystallization" (SPC) method of Fig. 2, in comparison with the MSC method.

3. Current status of PCM modeling

In this section, models with different approaches and different levels of abstractions are described, from the macro models, to more physics-oriented models.

3.1. Macro models

One key feature of the PCM is the switching from the amorphous state to crystalline state, or from the amorphous state to a dynamic on state. In the most common current–voltage characteristics, the above switching shows a snap-back. One essential starting point for a macro model is to find an appropriate representation for the device, either a pure mathematic one or a physics-based one for other well-studied devices. In the latter case, a lumped SPICE model may be generated by borrowing the formulations of devices with similar I–V and the switching.

3.1.1. Cobley's model

A macro model of PCM was reported[45]. The core block of the model is shown in Fig. 7(a), and extensions to this block to include the 'conductive on' and transient simulation capability were also reported. There are also variations to the core block in latter models, but the main idea is clearly reflected in Fig. 7(a). Including in the 'word circuit', interlinked switches are included in the Zin part, determining its outputs (Vset, and Vreset) to the RSff which is a flip-flop. When the input to the Zin part is a lower voltage, Vset is high and Vreset is low. The RSff part generates a high voltage, which is used to control the 'Zmodel'. For a high Vffout, the switches S1 and S2 respond correspondingly: S1 closed and S2 open. As a result, the resistance sensed from the Isense terminal is different depending on the state of switches. In the S1 branch, the amorphous resistance is included, together with another compensation resistance, to form the high-resistance PCM state. In the S2 branch, the crystalline resistance is included, and another diode is also included, to form the low resistance PCM state which shows a non-linear dependence. The memory state changes when the input to the Zin part goes high, as the flip-flop RSff outputs a low Vffout and the switches S1 and S2 changes their status. As is seen, the macro model used the flip-flop logic for the core memory function, and switches to control the transitions between PCM resistive states.

To model the snap-back, a silicon-controlled rectifier (SCR) type formulation was used for a softer transition from the high-resistance to low-resistance state. Some considerations on the transition smoothness are incorporated in the model with additional circuit components. Fig. 7(b) shows the I–V curves from the macro model in comparisons with the experimental data. For transient simulation, it is necessary to account for the duration of the input pulse, especially for the SET process. An extension to the Word circuit with an integrator is included to detect the input amplitude and duration, and only activates the switching when the crystallization/amorphization is expected to finish after a period.

3.1.2. Wei's model

A similar macro model was reported[46] with a similar approach but extended features. Fig. 8 shows the flow chart of the macro model. A thermal circuit and a crystallization mod-

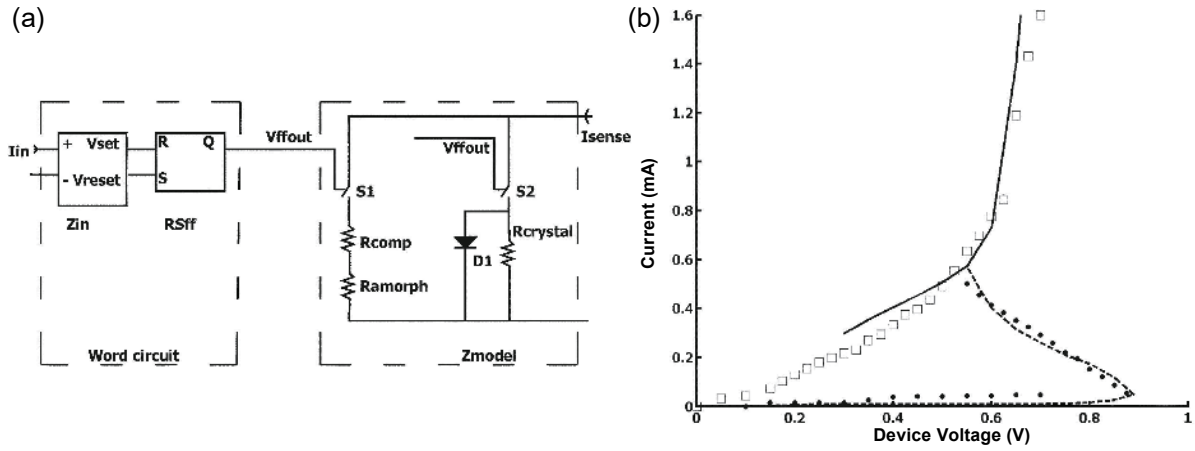

Fig. 7. (a) Core block of the model. (b) *I–V* curves from the macro model (line) in comparisons with the experimental data(dots). © [2006] IEEE. Reprinted with permission from Ref. [45].

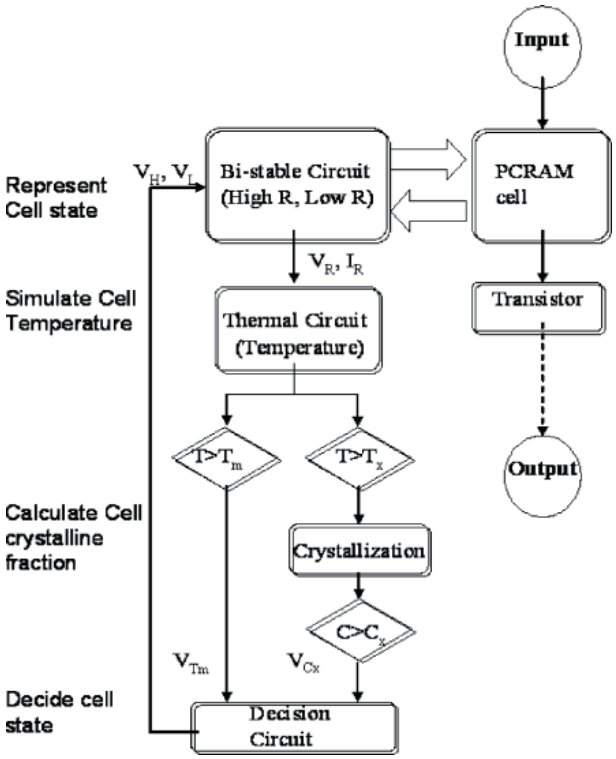

Fig. 8. Flowchart of the binary macro model with different modules to decide the temperature and the phase. © [2006] IEEE. Reprinted with permission from Ref. [46].

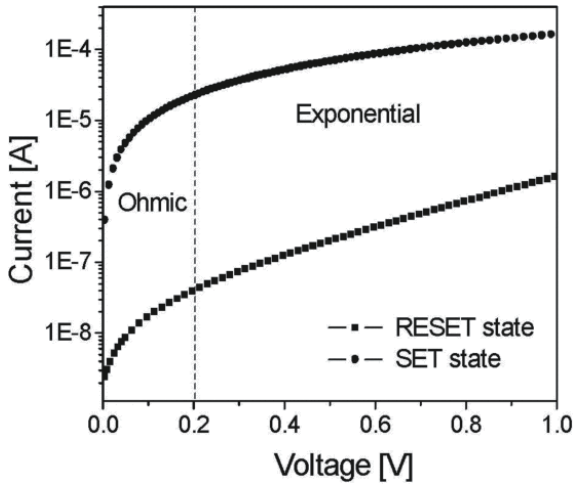

Fig. 9. *I–V* characteristics of RESET and SET state, with temperature dependence following the Arrhenius law. The threshold switching is realized by a versatile function *F* which provides a smooth transition from the high-resistance to low-resistance state. © [2006] IEEE. Reprinted with permission from Ref. [50].

ule were introduced on top of the bi-stable circuit. The two modules were both implemented with circuit macros like amplifiers based on the physics of Joule heating and crystallization kinetics. The Joule heat is calculated for the temperature, which is fed into the crystallization module for a trace of the crystal fraction. As a result, multi-level storage is supported in addition to the binary storage for the previous model. The trade-off between pulse height and width for programming was demonstrated. Similar macro models were reported in the literature[29, 47–49]. It is interesting to note that the macro model[48] is used to demonstrate a spiking neuron circuit based on PCM.

Macro models are relatively straightforward to be developed without knowing the device physics. As seen above, existing circuit blocks are connected to reproduce the observed PCM properties. The PCM macro models have been assisting the technology development at the early stage. One general drawback of macro models is a high complexity and long computational time. Thus physics-based models are usually pursued when the technology becomes more mature.

3.2. Physics-based model

3.2.1. Fantini's model

A single piece model was reported[50] for the first time. The model description of the conduction in the amorphous and crystalline phases are both based on the avalanche of chalcogenide materials, Eq. (9). n_{status} is a multiplication factor in the unit of V^{-1}, and R_0 describes the low field resistance. Both are regarded as functions of the phase change material status, i.e., the crystalline fraction. For lower voltages, Eq. (9) is simplified as $I = V_1/R_0$, hence linear. For higher voltages, the current depends on voltage exponentially. The current equation (9) takes the temperature dependence into consideration, which satisfies the Arrhenius law. T_{ref} is reference temperature. $E_{a,status}$ is the activation energy which can be extracted from the temperature measurement. Fig. 9 plots the *I–V*

characteristics with two states.

$$I_a(V_1, V_{\text{status}}) = \frac{1}{n_{\text{status}} R_0(V_{\text{status}}) \cdot \exp\left[\frac{E_{\text{a,status}}}{k}\left(\frac{1}{T} - \frac{1}{T_{\text{ref}}}\right)\right] \times [\exp(n_{\text{status}} V_1) - 1]}. \quad (9)$$

A smooth function $F(x, x_t)$ is proposed for the threshold switching behavior. It can be any function which switches from 0 to 1 around a threshold value $x = x_t$. In practice, a Fermi-like function is a good option. For the PCM modeling, a parameter of threshold current (I_{th}) is used to represent the critical condition of threshold switching, and the current–voltage relationship is described by Eq. (10). Starting from the high resistance (e.g. fully amorphous) state, the current is given by Eq. (9) before it reaches I_{th}. Once the current reaches I_{th}, the smoothing $F(I_1, I_{\text{th}})$ goes from zero to one, and the PCM switches to the crystalline state. The conduction is then described by the on state current I_{on}, which is part of the $I_{a\text{SET}}$. The 'versatile' function provides a flexible description of the threshold switching, which is also termed as a voltage snap-back. Anyway, the current always increases, unlike the voltage drop across the PCM.

$$I_1 = I_a(V_1, C_x) + F(I_1; I_{\text{th}}) \cdot [-I_a(V_1, C_x) + F(V_1; V_{\text{hold}}) \cdot I_{\text{on}}(V_1)]. \quad (10)$$

The cross point of the snap-back branch and the $I_{a\text{SET}}$ branch is (V_{hold}, I_{hold}), which satisfies the crystalline state $I_{a\text{SET}}$ of Eq. (9) as well as the load line below:

$$I = -\frac{V}{R_{\text{load}}} + \frac{V_{\text{th}}}{R_{\text{load}}}, \quad (11)$$

in which R_{load} is the PCM load resistance (the resistance in series, e.g. the heater resistance). V_{th} is the threshold voltage. In the implementation, the PCM together with a given load resistance R is treated as a voltage controlled current source (VCCS). At the threshold voltage, the passing current changes from the $I_{a\text{RESET}}$ to I_{on}.

The model[50] implemented a mechanism to monitor the quenching time after melting temperature has been reached for the MSC method in Fig. 6. Auxiliary circuits including several blocks are proposed for this purpose. A table lookup approach is used to determine the SET resistance according to the quenching time. Advantages include the ability to model the multi-level cell (MLC) operation. Note that for partial SETs the parameter of V_{status} between that of the RESET and full SET goes into Eq. (9) to determine the high-resistance current conduction. The threshold swing is chosen to be reorganized by a constant threshold current I_{th}, which means a reduced threshold voltage for partial SET PCM.

3.2.2. Ventrice's model

An improved model without involving the table-based approach for crystallization was reported[51]. A more physics meaningful crystal fraction C_x is used instead of V_{status} to represent the degree of crystalline state. The time evolution of C_x, i.e. the crystallization kinetics, is developed as follows with a temperature-dependent time constant τ:

$$C_x = 1 - \exp\left(-\frac{t}{\tau}\right). \quad (12)$$

It is indeed identical to the JMAK theory with Avrami coefficient $n = 1$. The phase change material resistance is determined with C_x:

$$R_x = R_{0c} + (R_{0a} - R_{0c})(1 - C_x), \quad (13)$$

in which R_{0c} and R_{0a} the resistance of state which are completely crystallized and amorphized, respectively.

Fig. 10 shows that Eq. (12) agrees well with the experimental data of resistance evolution in the time domain under a certain temperature. With Eqs. (12) and (13), the crystallization process can be described step-by-step with the temperature at each step. For the implementation, auxiliary circuits in Fig. 11 to integrate for the crystal fraction C_x is introduced. A temperature circuit calculates the heat and obtains the temperature. Taking the temperature as inputs, the timer circuit accumulates time when the temperature is between the crystallization temperature T_c and melting temperature T_m. The crystal fraction circuit implements the Eq. (12) with inputs from the timer circuit. At the same time, C_x goes to zero once the tem-

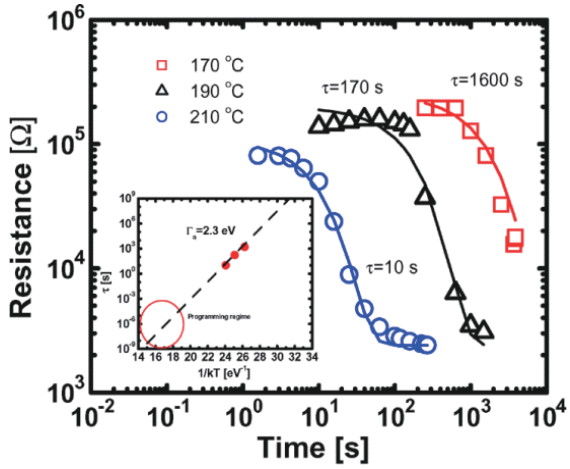

Fig. 10. (Color online) Crystallization dynamics as given by the JMAK theory and the experimental data under different temperatures. Temperature dependence of the time constant follows approximately the Arrhenius law. © [2007] IEEE. Reprinted with permission from Ref. [51].

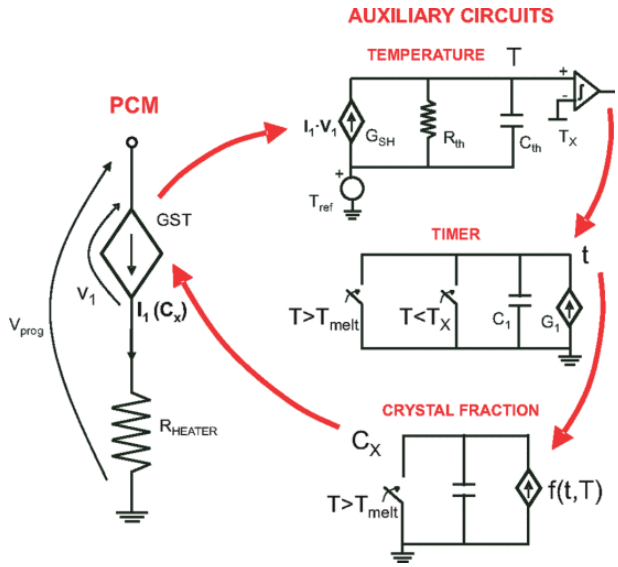

Fig. 11. (Color online) Auxiliary circuits are introduced to implement the crystallization kinetics of Eq. (12). © [2007] IEEE. Reprinted with permission from Ref. [51].

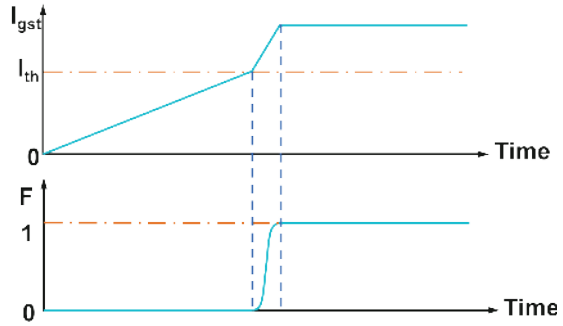

Fig. 12. (Color online) A dynamic "versatile" function F for descriptions of the threshold switching process in the time domain.

perature reaches T_m. The crystal fraction C_x is fed back into the current–voltage equations, and a self-consistency loop is implemented in the model.

With the model[51] pioneering the physics-based PCM modeling, both SET programming themes of MSC and SPC are in principle supported. Compared to macro models, the model calculation efficiency is highly enhanced due to the reduced complexity. There are variations in this model category, for example, with or without switches in the implementations.

3.2.3. Sonoda's model

A model with rate equations of crystallization and amorphization was reported[52]. For the dynamic phase transitions, the threshold swing was modeled not only in the voltage/current domain but also in the time domain. By observing a switching time in the range of τ_f = 0.15 ns, a dynamic version of the "versatile" function, Eq. (14) was developed. It is playing a role of smoothing in the transient simulations of the PCM, i.e. the setting process. When I_{gst} crosses the threshold current I_{th}, the variable F asymptotically approaches zero or one in the time domain. Fig. 12 plots the waveforms of the PCM voltage, current as well as the variable F.

$$\frac{\mathrm{d}F}{\mathrm{d}t} = -\frac{F - \theta\left(I_{gst} - I_{th}\right)}{\tau_f}, \tag{14}$$

in which $\theta(x)$ is the step function, which is zero or one when $x < 0$ or $x > 0$.

The amorphous volume V_a is formulated with the classical nucleation theory instead of the crystallization kinetics Eq. (12) of the JMAK theory used before. In a nucleation-driven case, the crystallization rate is given by $P_n V_n V_a/V_m$, where P_n is the nucleation probability per unit time, V_m is the volume of a monomer, and V_n is the volume of a nucleus. In a growth-driven case the crystallization rate is given by $S_a v_g$, where S_a is the area of amorphous/crystalline interface, v_g is the growth velocity. For the purpose of model simplicity, the nucleation and growth processes are not treated as successive but concurrent processes. By summing these two crystallization processes, a kinetic equation for C_a is developed in the model with:

$$\left(\frac{\mathrm{d}V_a}{\mathrm{d}t}\right)_c = -\left(P_n V_n \frac{V_a}{V_m} + S_a v_g\right). \tag{15}$$

The model is also self-limited, and the RHS approaches zero when V_a comes from 1 to 0. If the growth term is ignored, the above Eq. (15) resembles the JMAK-type formulation of Eq. (12), where the term $\tau = V_m/(P_n V_n)$ characterizes the time constant of the nucleation process (e.g. the time needed for the amorphous volume to change the amount of a monomer V_m).

$$\left(\frac{\mathrm{d}V_a}{\mathrm{d}t}\right)_c = -\frac{V_a}{\tau}. \tag{16}$$

In principle, the total growth frontier is the summation of that of the scattered nucleus and that of the amorphous/crystalline regional interface. For simplicity, only the later area enters into the growth term of Eq. (15). The advantage of using the rate equation is to capture the essential temperature dependence in the crystallization process.

At the same time, the amorphization process is also modeled with a rate equation. Considering that the temperature difference between the PCM local temperature and the melting temperature is the driving force for the amorphization (melting then quenching), the rate equation is given by:

$$\left(\frac{\mathrm{d}V_a}{\mathrm{d}t}\right)_a = \frac{T_a - T_m}{R_t \Delta h_1}, \tag{17}$$

in which Δh_1 is the latent heat of solid-to-liquid transition and T_a is the temperature at the amorphous/crystalline interface.

Assuming an initial state of full crystallization ($V_a = 0$), the reset current raises the BE/PCM interface temperature T_b, which is also T_a at the moment, above T_m. Then the RHS drives the melting region interface towards the TE. With a larger V_a hence a new melting/crystalline interface, T_a evaluated at the interface decreases (roughly $T_a = (T_b - T_{ref}) \times (1 - V_a/V_{amax}) + T_{ref}$) with a linear temperature profile), also the melting rate decreases. Assuming the peak temperature T_b is constant, the melting region frontier moves until T_a is equal to T_m, which eventually determines the size of the amorphous region. Hence, in the rate formulation the term $P_a = (T_a - T_m)/R_t$ can be regarded as the frontier local melting power, with Δh_1 the heat of fusion (unit of J/cm^3). As a result, the formation time of melting volume is $\Delta h_1/P_a$. The rate equation is also made self-limiting by a theta function, as the maximum V_a is fixed for a technology. The two rate equations, Eqs. (15) and (17), are combined as a unified rate equation Eq. (18) for the phase dynamics. Eq. (18) is evaluated in a time evolution manner. Together with the other equations, the phase change memory operations including read, set and reset, are modeled.

$$\frac{\mathrm{d}V_a}{\mathrm{d}t} = \left(\frac{\mathrm{d}V_a}{\mathrm{d}t}\right)_c \theta\left(T_m - T_a\right) + \left(\frac{\mathrm{d}V_a}{\mathrm{d}t}\right)_a \theta\left(T_a - T_m\right). \tag{18}$$

Compared to previous models, Sonoda's model formulates the threshold switching and memory switching in the form of rate-equations. It also considers the different temperature dependences in the nucleation and growth process. With these, the model marks a reference for later rate-equation based models.

3.2.4. Pigot's model

Later, another rate-equation based model was reported[53]. Three variables, the crystalline fraction F_c, the amorphization fraction F_a, and the melting fraction F_m, are used to represent the state of the PCM cell, with F_m the new

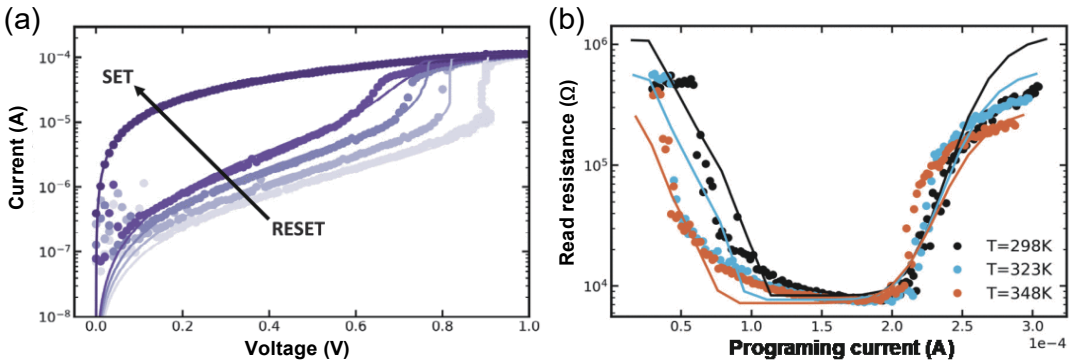

Fig. 13. (Color online) (a) Current of the PCM versus voltage with vary amorphization fraction F_a. Dots (experiments), lines (simulations). (b) R–I curve of PCM under different temperature. Dots (experiments), lines (simulations). © [2018] IEEE. Reprinted with permission from Ref. [53].

variable compared to the previous models. The melting fraction increases and may come closer to 1 in a dynamic process depending on the temperature above the melting T_m. When the temperature goes below T_m, the rate equation also describes the process of quenching, i.e. F_m decreases and comes closer to zero. It is noted that the fractions above are not corresponding to the PCM cell physics state. For the three-dimensional active region of the mushroom type, the fractions are in fact calculated assuming a one-dimensional profile. The resistance calculations are also done in a one-dimensional way without going to the details of current distributions in the 3D structure.

The rate equation for F_m is given by:

$$\tau_m \frac{\partial F_m}{\partial t} + F_m = \left[1 + \exp\left(\frac{T_m - T}{\sigma_m}\right)\right]^{-1}, \tag{19}$$

in which τ_m is melting time constant. While σ_m is treated as a fitting parameter. When the temperature T goes beyond T_m, Eq. (19) gives the transition of F_m from zero to non-zero depending on σ_m. Thus, the parameter σ_m is also used to control the abruptness of the reset resistance of the R–I curve. A larger σ_m decreases the melting fraction F_m for a given temperature T, which then becomes the amorphous fraction F_a after the reset.

The rate equation for F_c follows the theory of JMAK. As the melting fraction is introduced, the differential version of Eq. (20) is revised a bit and goes as follows:

$$\tau_c \frac{\partial F_c}{\partial t} + F_c = 1 - F_m, \tag{20}$$

in which τ_c is the characteristic time of crystallization.

Lastly, the fraction of amorphization F_a is the remaining part besides of the crystalline and melting fractions.

$$F_a = 1 - F_m - F_c. \tag{21}$$

After considering the non-Arrhenius crystallization, Eq. (20) is revised to the following with a fitting parameter b:

$$\tau_{set} \frac{\partial F_c}{\partial t} = F_a b \exp\left(1 - bF_a\right), \tag{22}$$

in which τ_{set} is the temperature-dependent crystallization time. It is used to compensate the simplification of using the highest temperature for the crystallization rate. As the F_a is decreasing, RHS of Eq. (22) first increases then decreases with a peak at a certain F_a. Further, to account for the non-Arrhenius crystallization the set time τ_{set} is revised by including to activation energy:

$$\tau_{set} = \tau_{HT} + \tau_{LT} = \tau_{0HT}\exp\left(\frac{E_{AHT}}{kT}\right) + \tau_{0LT}\exp\left(\frac{E_{ALT}}{kT}\right), \tag{23}$$

in which τ_{LT} and τ_{HT} are crystallization time for low temperature and high temperature, τ_{0LT} and τ_{0HT} are crystallization time prefactor for low temperature and high temperature, E_{ALT} and E_{AHT} are activation energy for low temperature and high temperature.

At the same time, caution is needed to handle the three-variable system as none of F_c, F_a and F_m can be negative, and reduction of F_c in the reset process is not reflected with Eq. (20) or (22). In Ref. [53], the current is modeled with a Poole–Frenkel conduction by assuming a complete voltage drop across the amorphous part.

$$I_{PF} = A_{kPF} F\left(-\frac{\Phi_{PF} - \beta_{PF}\sqrt{F}}{kT}\right), \tag{24}$$

in which A_{kPF}, Φ_{kPF} and β_{kPF} are fitting parameters.

And the barrier dependence on temperature is given by:

$$\Phi_{PF} = E_{a0} - \frac{a_{va}T^2}{b_{va} + T}, \tag{25}$$

in which E_{a0} is the activation energy at 0 K, considered as a fitting parameter, a_{va} and b_{va} are the thermal parameters.

By increasing the voltage, the current first increases with only the barrier lowering term as the heat is not significant. After the current goes above a certain level, the temperature rising comes into the picture and the transport barrier is reduced upon the heat. As a result, the current increases sharply with the voltage, or the voltage required to maintain the current is reduced for a snapback behavior. Fig. 13(a) plots the sharp switching from the amorphous state to crystalline state. With the core model equations Eqs. (19)–(25), the model captures the R–I characteristics as shown in Fig. 13(b).

Compared to previous models, Pigot's model implements a physics-based threshold switching module, and a simplified crystallization module with rate-equations. The model incorporates related parameters for its flexibility, and has been verified by the industry's PCM data in STMicroelectronics.

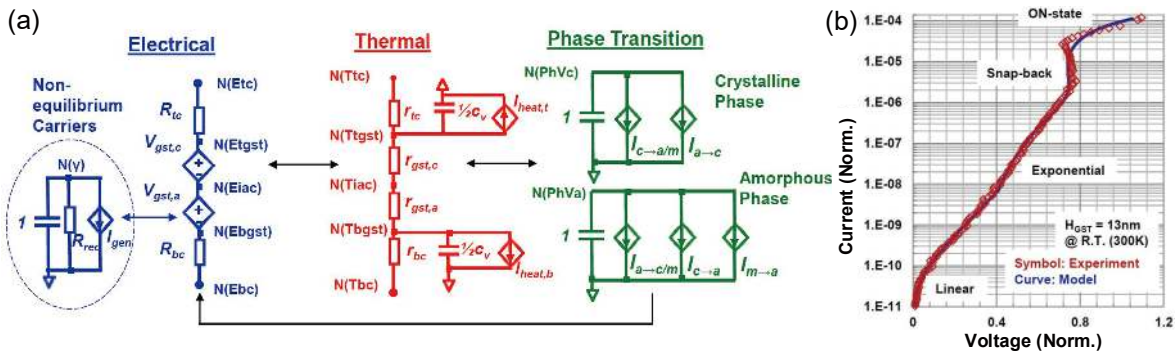

Fig. 14. (Color online) (a) Equivalent circuit model, including all the modules: the transport module, the thermal module and phase transition module. (b) Model compared with experiment data on *I–V* characteristic. © [2016] IEEE. Reprinted with permission from Ref. [54].

3.2.5. Xu's model

A model incorporating the phase transitions between three possible states was reported[54]. The key rate equation used for the phase transitions is Eq. (26), with c the capture rate and e the emission rate. Similar to Figs. 5(a) and 5(b)[40], the normalized ratios of three phase states are given first following the Arrhenius law. The transition rates including those from amorphous to crystalline, from crystallization to melting, and from melting to amorphous are explicitly given. The rates in the opposite directions are calculated from the equilibrium cases. Based on these rates, the dynamic transition equations form the governing equation set for the phase transition:

$$\frac{\mathrm{d}\Omega_i}{\mathrm{d}t} = \sum_{i\neq j}\sum_{e,c\in P}\left(c_{j\to i}\Omega_j - e_{i\to j}\Omega_i\right), \tag{26}$$

in which Ω_i is the normalized ratio of phase state i.

The resistance module incorporates an energy gain theory[35] based on the Poole–Frenkel transport. Two trap states, a shallow trap state n_{T2} and a deep trap state n_{T1}, are considered with possible re-populations between them. With a low field, the two states are generally conductive separately. With increasing the field, electrons in the deep trap state are possibly transmitted to the shallow trap states with tunneling, forming the non-equilibrium carriers n_{T2}'. The key equations of the current are summarized:

$$I = 2eA\frac{\Delta z}{\tau_0}\left[n_{T1}\exp\left(-\frac{E_c - E_{T1}}{kT}\right) + (n_{T2} + n_{T2}')\exp\left(-\frac{E_c - E_{T2}}{kT}\right)\right] \times \sinh\left(\frac{dU}{kT}\right), \tag{27}$$

$$H_{a,OFF} = \frac{E_{T2} - E_{T1}}{kT}, \tag{28}$$

$$H_{a,ON} = H_{gst,a} - H_{a,OFF}, \tag{29}$$

$$V = F_{OFF}H_{a,OFF} + F_{ON}H_{a,ON}, \tag{30}$$

in which E_{T1} is deep trap energy and E_{T2} is shallow trap energy, and Δz is trap distance.

The increase of the electron population in the shallow trap states increase the conduction current significantly. In the process, positive feedback is indeed happening. An increase of the current in the non-equilibrium region increases the electric field in the equilibrium region, which then increases the electron tunneling rate into the shallow trap states, and leads to a further increase of the current. This positive feedback is observed as a switching from the high resistance amorphous state to the dynamic low resistance state. In the model implementations, a current-controlled voltage source is used with simulation convergence considered. For the Joule-heating, the thermal resistance of different regions including those at the interfaces are all considered. Fig. 14(a) shows the schematic of the developed model including all the modules: the transport module, the thermal module and phase transition module, and Fig. 14(b) plots the comparisons between the models and experimental data.

Compared to previous models, Xu's model implements a physics-based threshold switching, as well as a dynamic phase-transition model of Fig. 5. The model has been used for cross-point memory array simulations in Samsung.

4. Challenges and perspectives

Towards a fully-functional PCM model for circuit designs especially neuromorphic circuits, there are still some challenges ahead. From our perspective, these challenges include at least three parts: modeling for scaled PCM, modeling for variations[55], and modeling for reliability.

4.1. Modeling for scaled PCM

The models in Section 3 are mainly developed for the classical mushroom PCM cells. Along with the technology scaling, alternative memory cell structures are developed such as the confined one[5, 15, 16] with high integration density. The thermal boundary has changed significantly, for example, the temperature profile peaks at completely different locations in the cross-point PCM[56]. The crystallization speed also changes due to absence of crystal seeds when a full reset of the confined region is triggered. These changes call for extensions of the current models or new generations of PCM models. It is in some sense similar to the scenarios of CMOS modeling which evolves with device geometry changes from planar to FinFET and gate-all-around structures. A PCM model that covers different cell geometries is highly desirable.

Relaxation oscillations in PCMs have been observed[57–60]. The voltage across a PCM cell shows an oscillation, which features a current dependent frequency. Furthermore, the peak voltages are being relaxed in the process. A conductive filament theory[61] was proposed to describe the oscillation in

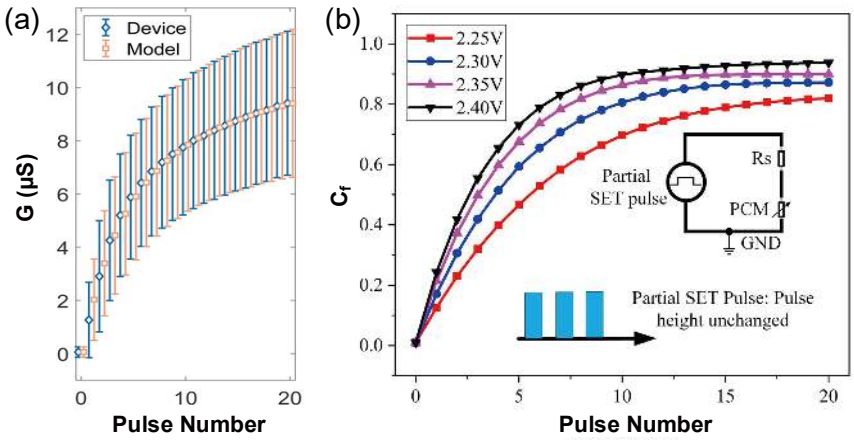

Fig. 15. (Color online) (a) The distribution of conductance values as a function of the number of partial SET pulses. Reprinted from Ref. [67], with the permission of AIP Publishing. (b) Modeling the gradual SET process where the crystalline ratio C_f of the PCM is recorded after each pulse.

chalcogenide OTS devices, which are nowadays used as selectors[62–65]. Although PCM is based on totally different chalcogenide glass which could undergo rapid crystallization, the relaxed oscillation may be explained with a similar reason. Later, the voltage/current dependent frequency was explained with a simple RC circuit assuming a holding current[57]. A field-induced nucleation theory was proposed[59] to describe the threshold voltage and holding voltages, as functions of material and geometry parameters. To utilize the oscillation properties of PCM in circuits for example the neuromorphic circuits, a further extension of the PCM model[66] is to be developed by incorporating the related theories.

For a complete compact model, its parameter extractions are also needed to represent the technology with a process design kit. Different from the MOSFET model in which the parameters are extracted based on the DC and frequency domain properties, the PCM model requires an extraction also from the time domain properties such as the crystallization dynamics. Thermal-related parameters like the thermal resistance and thermal boundary resistance in a possible thermal network, are also to be extracted. An extraction strategy together with algorithms should be figured out.

4.2. Modeling for variations of PCM and circuits

A statistical model in an evolutionary manner for PCM conductance in the SET process has been developed[67]. The model is intended to capture the statistical characteristics of PCM crystallization. Statistical properties are experimentally characterized: a pulse train is applied to a group of PCM cells with their initial conductance set as a high resistance state 0.1 μS. The first observation is that the increment of conductance after a programming pulse is decreased, as seen in Fig. 15(a). The same trend has been captured well in a physics-based model, as shown in Fig. 15(b)[68]. It is understood from the JMAK equation, suggesting that the crystallization rate decreases with the accumulation of crystal fraction. At the same time, experimental characterizations also reveal a significant variation of the conductance among the PCM cells. Fig. 15(a) shows, for example, after the first partial SET pulse of some PCM cells does not further crystallize though the average conductance seems following the physics-based model prediction. It is speculated that this originates from the randomness of the crystallization process, e.g. the nucleation randomness as explained in Section 2. The statistical nature of PCM programming[69], sometimes termed as a cycle-to-cycle variation, is not covered in previous compact models.

The model developed by Nandakumar *et al.*[67] is summarized as Eqs. (31)–(34). The subscript N denotes the Nth programming pulse. The incremental conductance is a sampling of a Gaussian distribution, with the distribution parameters, the average and standard deviation, given by Eqs. (31) and (32), which are also evolving with the conductance itself. While the other parameters are for the purpose of fitting, χ represents a Gaussian random number of mean zero and variance 1, the variable P_{mem} is used to capture the programming history effect. The model reproduces very well the variations of measured PCM conductance as shown in Fig. 15(a).

$$\mu_{\Delta G_N} = m_1 G_{N-1}(t_0) + (c_1 + A_1 P_{\text{mem}}), \tag{31}$$

$$\sigma_{\Delta G_N} = m_2 G_{N-1}(t_0) + (c_2 + A_2 P_{\text{mem}}), \tag{32}$$

$$\Delta G_N = \mu_{\Delta G_N} + \sigma_{\Delta G_N} \chi, \tag{33}$$

$$G_N(t_0) = G_{N-1}(t_0) + \Delta G_N. \tag{34}$$

While this model has been used for a two-PCM based spiking neural network, it is not directly applicable to CMOS-PCM integrated circuit simulations. Examples of the CMOS-PCM integrated neuromorphic computing circuits are reported[19] for unsupervised SNN learning with the spiking time-dependent plasticity (STDP). In the example, the spiking time difference between the pre-synaptic and post-synaptic neurons are translated into the voltage pulse amplitude which induces the different amount of conductance change. A statistical transistor model, together with a statistical PCM model, will favor the design and simulations of neuromorphic circuits in a similar way as CMOS circuits. The transistor model has been in use for long but such a statistical PCM model is not yet available. At the same time, it is interesting to note that circuit level innovations are also being proposed to mitigate the variations, for example, by the multi-memristive synapse[70]. It has been shown that the SNN classification performance is largely improved with the developed approach. However, variations cannot be fully eliminated. A further exten-

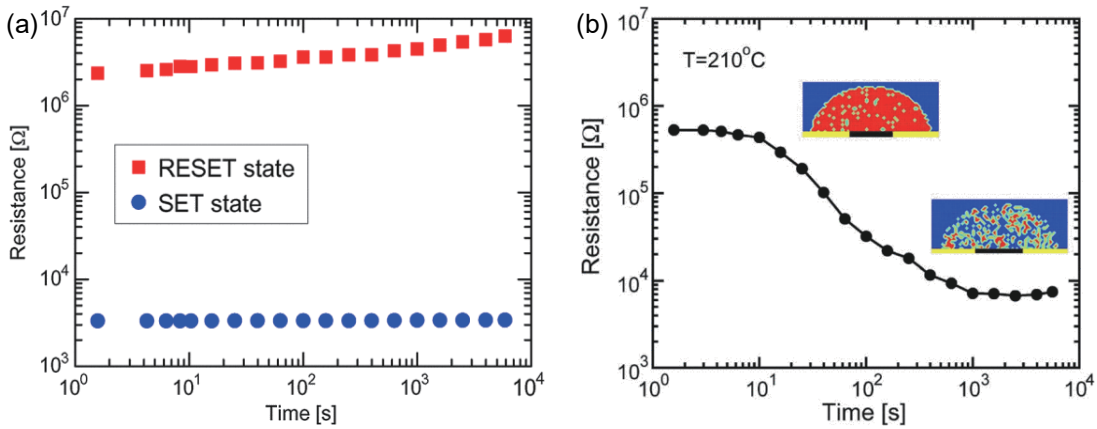

Fig. 16. (Color online) (a) Resistance as a function of time for the amorphous (reset) and crystalline (set) states of a PCM device. © [2010] IEEE. Reprinted with permission from Ref. [72]. (b) Resistance versus time for a reset cell. The two insets represent the mixed-phase structure for relatively short (top left) and long (bottom right) times during the bake experiment. © [2006] IEEE. Reprinted with permission from Ref. [73].

sion to incorporate the variation and stochastic crystallization is essential for the circuit evaluations, based on a physics-based device-level model of current–voltage characteristics such as those in Section 3. That will be one possible next step for the PCM compact modeling.

4.3. Modeling for reliability of PCM and circuits

PCM conductance drifts after programming, especially after the RESET. Fig. 16(a) shows that the high resistance increases with time, while the low resistance does not change much. Physics-based models[71] and statistical models[72] have been developed to describe the resistance drift behaviors, in the single cell and PCM array levels. It is attributed to the structural relaxation after quenching, where the further rearrangement of local atomic structure leads to change of local states with the long-range disorder. A power law dependence of the resistance is empirically used with t_1 as reference time t of PCM programming[71]:

$$R(t) = R_1\left(\frac{t}{t_1}\right)^v, \tag{35}$$

in which R_1 is the resistance value at $t = t_1$ and v is the power-law exponent. The physics meaning of the exponential factor v is derived[71], which is related to the increase of action energies for structure relaxation and conduction with time. The theory also explains the resistance dependent v factor observed in Fig. 16(a). Experimental characterizations in Ref. [72] further verifies the empirical expression, and a read noise is also included in the statistical model.

In additional to the resistance increase due to structural relaxation, resistance decrease[74] due to spontaneous crystallization is another concern of PCM reliability. For memory array application, a long-term data retention at 85 °C is required. Fig. 16(b) shows the high-resistance retention under accelerated test conditions. For a binary or multi-level cell, it is usually a no-or-yes issue, with the retention failure or not. For the neuromorphic circuits, whether and to how much extent the resistance shifts changes circuit performances require further considerations. Other observed reliability issues include cycle endurance, thermal disturbance, and switching threshold voltage drifts. Cycle endurance describes the capacity to re-write in a PCM cell without failure[75]. The PCM cell may not be programmed into the high resistance from the SET state, or may remain a high resistance without successful SET. Possible mechanisms are the change of intrinsic chalcogenide material properties after undergoing high temperature[76]. The thermal disturbance is spontaneous crystallization due to heat from neighbor cells' operations[77]. Finally, threshold voltage shift also happens[78], which is expected to be correlated to the resistance shifts. As stated earlier, analog memory property is used to represent the synapse connectivity in neuromorphic circuits. The resistance/threshold voltage shifts in the time domain, i.e. the change in synapse weight, in principle shifts the circuit characteristics like accuracy.

Innovative device level designs such as a projected PCM[79] are also being excitingly explored to suppress the resistance shifts. The active phase change region is projected to non-phase-change materials for the high resistance state. With it, the reliability of the PCM-based cross-bar network is greatly enhanced. Based on the working principle, the high-resistance state eventually degrades when the resistance shifts in the amorphous region increase to an extent altering the current bypass. Moreover, projected PCM has been implemented in a single-layer neural network[80], which could keep a high classification accuracy at elevated temperatures without temperature compensated way. Generally, for reliability-aware neuromorphic circuit designs reliability modeling of PCM cells[81] deserves further effort.

5. Conclusion

Phase change memory has been on the stage of emerging memory technologies for some time, and recently promises applications in neuromorphic computing. In this work, we review the developments of PCM compact models, and try to provide an analysis of the challenges from our perspective. Generally, developing a compact model based on the device physics is a trend, especially when the device variations and reliability are important considerations. We start from the basic operation principles of PCM, and describe the known theoretical framework of crystallization (including nucleation and growth) and amorphization. Then we explain the evolution of the PCM models from macro models to more physics-oriented models, with different approximations in the

model development. While the state-of-the-art PCM models provide a basis for circuit simulations, future model developments are facing challenges from the statistical modeling, to design-for-reliability models to facilitate the PCM applications in neuromorphic circuits.

Acknowledgements

This work is supported in part by the National Natural Science Foundation of China (62074006, 91964204), in part by the Major Scientific Instruments and Equipment Development (61927901), the Shenzhen Science and Technology Project (GXWD20201231165807007-20200827114656001), Strategic Priority Research Program of the Chinese Academy of Sciences (XDB44010200), Science and Technology Council of Shanghai (19JC1416801), the Shanghai Research and Innovation Functional Program (17DZ2260900), and in part by the 111 Project (B18001).

References

[1] Kim T, Lee S. Evolution of phase-change memory for the storage-class memory and beyond. IEEE Trans Electron Devices, 2020, 67, 1394

[2] Le Gallo M, Sebastian A. An overview of phase-change memory device physics. J Phys D, 2020, 53, 213002

[3] Gong N B. Multi level cell (MLC) in 3D crosspoint phase change memory array. Sci China Inf Sci, 2021, 64, 1

[4] Lee S H. Technology scaling challenges and opportunities of memory devices. 2016 IEEE International Electron Devices Meeting (IEDM), 2016, 1.1.1

[5] Kau D, Tang S, Karpov I V, et al. A stackable cross point phase change memory. 2009 IEEE International Electron Devices Meeting, 2009, 1

[6] https://www.anandtech.com/show/14437/intel-announces-optane-memory-m15-3dxpoint-on-m2-pcie-30-x4

[7] Arnaud F, Zuliani P, Reynard J P, et al. Truly innovative 28nm FD-SOI technology for automotive micro-controller applications embedding 16MB phase change memory. 2018 IEEE International Electron Devices Meeting (IEDM), 2018, 18.4.1

[8] Cappelletti P, Annunziata R, Arnaud F, et al. Phase change memory for automotive grade embedded NVM applications. J Phys D, 2020, 53, 193002

[9] https://newsroom.st.com/media-center/press-item.html/p4269.html

[10] Neale R G, Nelson D L, Moore G E. Nonvolatile and reprogramable, read-mostly memory is here. Electronics, 1970, 43, 56

[11] Tyson S, Wicker G, Lowrey T, et al. Nonvolatile, high density, high performance phase-change memory. 2000 IEEE Aerospace Conference, 2000, 385

[12] Lai S, Lowrey T. OUM – A 180 nm nonvolatile memory cell element technology for stand alone and embedded applications. International Electron Devices Meeting, 2001, 36.5.1

[13] Oh J H, Park J H, Lim Y S, et al. Full integration of highly manufacturable 512Mb PRAM based on 90nm technology. 2006 International Electron Devices Meeting, 2006, 1

[14] Annunziata R, Zuliani P, Borghi M, et al. Phase change memory technology for embedded non volatile memory applications for 90nm and beyond. 2009 IEEE International Electron Devices Meeting, 2009, 1

[15] Im D H, Lee J I, Cho S L, et al. A unified 7.5nm dash-type confined cell for high performance PRAM device. 2008 IEEE International Electron Devices Meeting, 2008, 1

[16] Kim T, Choi H, Kim M, et al. High-performance, cost-effective 2z nm two-deck cross-point memory integrated by self-align scheme for 128 Gb SCM. 2018 IEEE International Electron Devices Meeting, 2018, 37.1.1

[17] Chien W C, Ho Y H, Cheng H Y, et al. A novel self-converging write scheme for 2-bits/cell phase change memory for storage class memory (SCM) application. 2015 Symposium on VLSI Technology, 2015, T100

[18] Gong N, Idé T, Kim S, et al. Signal and noise extraction from analog memory elements for neuromorphic computing. Nat Commun, 2018, 9, 2102

[19] Kim S, Ishii M, Lewis S, et al. NVM neuromorphic core with 64k-cell (256-by-256) phase change memory synaptic array with on-chip neuron circuits for continuous *in situ* learning. 2015 IEEE International Electron Devices Meeting, 2015, 17.1.1

[20] Bedeschi F, Fackenthal R, Resta C, et al. A bipolar-selected phase change memory featuring multi-level cell storage. IEEE J Solid State Circuits, 2009, 44, 217

[21] Suri M N, Bichler O, Querlioz D, et al. Phase change memory as synapse for ultra-dense neuromorphic systems: Application to complex visual pattern extraction. 2011 International Electron Devices Meeting, 2011, 4.4.1

[22] Suri M N, Bichler O, Querlioz D, et al. Physical aspects of low power synapses based on phase change memory devices. J Appl Phys, 2012, 112, 054904

[23] Tuma T, Pantazi A, Le Gallo M, et al. Stochastic phase-change neurons. Nat Nanotechnol, 2016, 11, 693

[24] Wright C D, Hosseini P, Diosdado J A V. Beyond von-Neumann computing with nanoscale phase-change memory devices. Adv Funct Mater, 2013, 23, 2248

[25] Wang Q, Niu G, Ren W, et al. Phase change random access memory for neuro-inspired computing. Adv Electron Mater, 2021, 7, 2001241

[26] Pavan P, Larcher L, Marmiroli A. Floating gate devices: Operation and compact modeling. IEEE Circuits and Devices Magazine, 2004, 120

[27] Xu Z H, Sutaria K B, Yang C G, et al. Hierarchical modeling of Phase Change memory for reliable design. 2012 IEEE 30th International Conference on Computer Design, 2012, 115

[28] Sebastian A, Le Gallo M, Burr G W, et al. Tutorial: Brain-inspired computing using phase-change memory devices. J Appl Phys, 2018, 124, 111101

[29] Wong H S P, Raoux S, Kim S, et al. Phase change memory. Proc IEEE, 2010, 98, 2201

[30] Raoux S, Wełnic W, Ielmini D. Phase change materials and their application to nonvolatile memories. Chem Rev, 2010, 110, 240

[31] Zhang W, Mazzarello R, Wuttig M, et al. Designing crystallization in phase-change materials for universal memory and neuro-inspired computing. Nat Rev Mater, 2019, 4, 150

[32] Zhang W, Mazzarello R, Ma E. Phase-change materials in electronics and photonics. MRS Bull, 2019, 44, 686

[33] Eaton D L. Electrical conduction anomaly of semiconducting glasses in the system As-Te-I. J Am Ceram Soc, 1964, 47, 554

[34] Pirovano A, Lacaita A L, Benvenuti A, et al. Electronic switching in phase-change memories. IEEE Trans Electron Devices, 2004, 51, 452

[35] Ielmini D. Threshold switching mechanism by high-field energy gain in the hopping transport of chalcogenide glasses. Phys Rev B, 2008, 78, 035308

[36] Peng C B, Cheng L, Mansuripur M. Experimental and theoretical investigations of laser-induced crystallization and amorphization in phase-change optical recording media. J Appl Phys, 1997, 82, 4183

[37] Lacaita A L, Ielmini D, Mantegazza D. Status and challenges of phase change memory modeling. Solid State Electron, 2008, 52, 1443

[38] Li Z J, Jeyasingh R G D, Lee J, et al. Electrothermal modeling and design strategies for multibit phase-change memory. IEEE Trans Electron Devices, 2012, 59, 3561
[39] Redaelli A, Pirovano A, Benvenuti A, et al. Threshold switching and phase transition numerical models for phase change memory simulations. J Appl Phys, 2008, 103, 111101
[40] Schmithusen B, Tikhomirov P, Lyumkis E. Phase-change memory simulations using an analytical phase space model. 2008 International Conference on Simulation of Semiconductor Processes and Devices, 2008, 57
[41] Weinberg M C, Birnie D P III, Shneidman V A III. Crystallization kinetics and the JMAK equation. J Non Cryst Solids, 1997, 219, 89
[42] Johnson W A, Mehl R F. Reaction kinetics in processes of nucleation and growth. Trans Amn Instit Mining Metall Eng, 1939, 135, 416
[43] Senkader S, Wright C D. Models for phase-change of $Ge_2Sb_2Te_5$ in optical and electrical memory devices. J Appl Phys, 2003, 95, 504
[44] Chen Z Q, Tong H, Cai W, et al. Modeling and simulations of the integrated device of phase change memory and ovonic threshold switch selector with a confined structure. IEEE Trans Electron Devices, 2021, 68, 1616
[45] Cobley R A, Wright C D. Parameterized SPICE model for a phase-change RAM device. IEEE Trans Electron Devices, 2006, 53, 112
[46] Wei X Q, Shi L P, Walia R, et al. HSPICE macromodel of PCRAM for binary and multilevel storage. IEEE Trans Electron Devices, 2006, 53, 56
[47] Cobley R A, Wright C D, Vázquez Diosdado J A. A model for multilevel phase-change memories incorporating resistance drift effects. IEEE J Electron Devices Soc, 2015, 3, 15
[48] Cobley R A, Hayat H, Wright C D. A self-resetting spiking phase-change neuron. Nanotechnology, 2018, 29, 195202
[49] Kwong K C, Li L, He J, et al. Verilog-A model for phase change memory simulation. 2008 9th International Conference on Solid-State and Integrated-Circuit Technology, 2008, 492
[50] Fantini P, Benvenuti A, Pirovano A, et al. A compact model for Phase Change Memories. 2006 International Conference on Simulation of Semiconductor Processes and Devices, 2006, 162
[51] Ventrice D, Fantini P, Redaelli A, et al. A phase change memory compact model for multilevel applications. IEEE Electron Device Lett, 2007, 28, 973
[52] Sonoda K, Sakai A, Moniwa M, et al. A compact model of phase-change memory based on rate equations of crystallization and amorphization. IEEE Trans Electron Devices, 2008, 55, 1672
[53] Pigot C, Bocquet M, Gilibert F, et al. Comprehensive phase-change memory compact model for circuit simulation. IEEE Trans Electron Devices, 2018, 65, 4282
[54] Xu N, Wang J, Deng Y X, et al. Multi-domain compact modeling for GeSbTe-based memory and selector devices and simulation for large-scale 3-D cross-point memory arrays. 2016 IEEE International Electron Devices Meeting, 2016, 7.7.1
[55] Calderoni A, Ferro M, Ventrice D, et al. Physical modeling and control of switching statistics in PCM arrays. 2011 3rd IEEE Int Mem Work IMW, 2011, 1
[56] Yoo S, Lee H D, Lee S, et al. Electro-thermal model for thermal disturbance in cross-point phase-change memory. IEEE Trans Electron Devices, 2020, 67, 1454
[57] Ielmini D, Mantegazza D, Lacaita A L. Voltage-controlled relaxation oscillations in phase-change memory devices. IEEE Electron Device Lett, 2008, 29, 568
[58] Nardone M, Karpov V G, Karpov I V. Relaxation oscillations in chalcogenide phase change memory. J Appl Phys, 2010, 107, 054519
[59] Nardone M, Karpov V G, Jackson D C S, et al. A unified model of nucleation switching. Appl Phys Lett, 2009, 94, 103509
[60] Hu H F, Liu D Y, Chen X H, et al. A compact phase change memory model with dynamic state variables. IEEE Trans Electron Devices, 2020, 67, 133
[61] Schmidt P E, Callarotti R C. Theoretical and experimental study of the operation of ovonic switches in the relaxation oscillation mode. I. The charging characteristic during the off state. J Appl Phys, 1984, 55, 3144
[62] Anbarasu M, Wimmer M, Bruns G, et al. Nanosecond threshold switching of $GeTe_6$ cells and their potential as selector devices. Appl Phys Lett, 2012, 100, 143505
[63] Burr G W, Shenoy R S, Virwani K, et al. Access devices for 3D cross-point memory. J Vac Sci Technol B, 2014, 32, 040802
[64] Lee M J, Lee D, Kim H, et al. Highly-scalable threshold switching select device based on chaclogenide glasses for 3D nanoscaled memory arrays. 2012 International Electron Devices Meeting, 2012, 2.6.1
[65] Ren K, Duan X, Xiong Q Q, et al. Constructing reliable PCM and OTS devices with an interfacial carbon layer. J Mater Sci: Mater Electron, 2019, 30, 20037
[66] Chen X H, Ding F L, Huang X Q, et al. A robust and efficient compact model for phase-change memory circuit simulations. IEEE Trans Electron Devices, 2021, 68, 4404
[67] Nandakumar S R, Le Gallo M, Boybat I, et al. A phase-change memory model for neuromorphic computing. J Appl Phys, 2018, 124, 152135
[68] Chen X H, Hu H F, Huang X Q, et al. A SPICE model of phase change memory for neuromorphic circuits. IEEE Access, 2020, 8, 95278
[69] Le Gallo M, Tuma T, Zipoli F, et al. Inherent stochasticity in phase-change memory devices. 2016 46th European Solid-State Device Research Conference, 2016, 373
[70] Boybat I, Le Gallo M, Nandakumar S R, et al. Neuromorphic computing with multi-memristive synapses. Nat Commun, 2018, 9, 2514
[71] Boniardi M, Ielmini D. Physical origin of the resistance drift exponent in amorphous phase change materials. Appl Phys Lett, 2011, 98, 243506
[72] Boniardi M, Ielmini D, Lavizzari S, et al. Statistics of resistance drift due to structural relaxation in phase-change memory arrays. IEEE Trans Electron Devices, 2010, 57, 2690
[73] Russo U, Ielmini D, Redaelli A, et al. Intrinsic data retention in nanoscaled phase-change memories—part I: Monte Carlo model for crystallization and percolation. IEEE Trans Electron Devices, 2006, 53, 3032
[74] Kim K, Ahn S J. Reliability investigations for manufacturable high density PRAM. 2005 IEEE International Reliability Physics Symposium, 2005, 157
[75] Gleixner B, Pellizzer F, Bez R. Reliability characterization of phase change memory. 2009 10th Annual Non-Volatile Memory Technology Symposium, 2009, 7
[76] Yang T Y, Cho J Y, Park Y J, et al. Effects of dopings on the electric-field-induced atomic migration and void formation in $Ge_2Sb_2Te_5$. 18th IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits, 2011, 1
[77] Pirovano A, Lacaita A L, Benvenuti A, et al. Scaling analysis of phase-change memory technology. 2003 IEEE International Electron Devices Meeting, 2003, 29.6.1
[78] Pirovano A, Lacaita A L, Pellizzer F, et al. Low-field amorphous state resistance and threshold voltage drift in chalcogenide materials. IEEE Trans Electron Devices, 2004, 51, 714
[79] Koelmans W W, Sebastian A, Jonnalagadda V P, et al. Projected phase-change memory devices. Nat Commun, 2015, 6, 1
[80] Giannopoulos I, Sebastian A, Le Gallo M, et al. 8-bit precision in-memory multiplication with projected phase-change memory. 2018 IEEE International Electron Devices Meeting, 2018, 27.7.1
[81] Redaelli A, Ielmini D, Russo U, et al. Intrinsic data retention in nanoscaled phase-change memories—part II: Statistical analysis and

prediction of failure time. IEEE Trans Electron Devices, 2006, 53, 3040

Feilong Ding is currently pursuing a master's degree with Peking University, China. His research interests include phase change memory modeling and simulation.

Baokang Peng received a BS degree in Electronic Science and Technology, in 2021, from Xidian University, Xian, China. He is currently working toward a PhD degree in microelectronics and solid state electronics at Peking University. His research interests include modeling and simulation of semiconductor devices.

Lining Zhang is an assistant professor with Peking University Shenzhen. He is currently a senior member of IEEE, and a member of IEEE EDS Technical Committee (Compact Modeling). His research interests include semiconductor device physics, compact modeling, circuit simulation algorithm and neuromorphic computing.