ARTICLES

Journal of Semiconductors
(2022) 43, 122802
doi: 10.1088/1674-4926/43/12/122802
JOS

A 4H-SiC semi-super-junction shielded trench MOSFET: p-pillar is grounded to optimize the electric field characteristics

Xiaojie Wang[1], Zhanwei Shen[2, †], Guoliang Zhang[1], Yuyang Miao[1], Tiange Li[1], Xiaogang Zhu[1], Jiafa Cai[1], Rongdun Hong[1, 3], Xiaping Chen[1], Dingqu Lin[1], Shaoxiong Wu[1], Yuning Zhang[1], Deyi Fu[1], Zhengyun Wu[1], and Feng Zhang[1, 4, †]

[1]College of Physical Science and Technology, Xiamen University, Xiamen 361005, China

[2]Key Laboratory of Semiconductor Material Sciences, Institute of Semiconductors, Chinese Academy of Sciences, Beijing 100083, China

[3]Shenzhen Research Institute of Xiamen University, Shenzhen 518057, China

[4]Jiujiang Research Institute of Xiamen University, Jiujiang 332000, China

Abstract: A 4H-SiC trench gate metal–oxide–semiconductor field-effect transistor (UMOSFET) with semi-super-junction shielded structure (SS-UMOS) is proposed and compared with conventional trench MOSFET (CT-UMOS) in this work. The advantage of the proposed structure is given by comprehensive study of the mechanism of the local semi-super-junction structure at the bottom of the trench MOSFET. In particular, the influence of the bias condition of the p-pillar at the bottom of the trench on the static and dynamic performances of the device is compared and revealed. The on-resistance of SS-UMOS with grounded (G) and ungrounded (NG) p-pillar is reduced by 52% (G) and 71% (NG) compared to CT-UMOS, respectively. Additionally, gate oxide in the GSS-UMOS is fully protected by the p-shield layer as well as semi-super-junction structure under the trench and p-base regions. Thus, a reduced electric-field of 2 MV/cm can be achieved at the corner of the p-shield layer. However, the quasi-intrinsic protective layer cannot be formed in NGSS-UMOS due to the charge storage effect in the floating p-pillar, resulting in a large electric field of 2.7 MV/cm at the gate oxide layer. Moreover, the total switching loss of GSS-UMOS is 1.95 mJ/cm^2 and is reduced by 18% compared with CT-UMOS. On the contrary, the NGSS-UMOS has the slowest overall switching speed due to the weakened shielding effect of the p-pillar and the largest gate-to-drain capacitance among the three. The proposed GSS-UMOS plays an important role in high-voltage and high-frequency applications, and will provide a valuable idea for device design and circuit applications.

Key words: breakdown voltage; specific on-resistance; silicon carbide; switching energy loss; super-junction-shield (SS); trench gate MOSFET; grounded (G); ungrounded (NG)

Citation: X J Wang, Z W Shen, G L Zhang, Y Y Miao, T G Li, X G Zhu, J F Cai, R D Hong, X P Chen, D Q Lin, S X Wu, Y N Zhang, D Y Fu, Z Y Wu, and F Zhang, A 4H-SiC semi-super-junction shielded trench MOSFET: p-pillar is grounded to optimize the electric field characteristics[J]. *J. Semicond.*, 2022, 43(12), 122802. https://doi.org/10.1088/1674-4926/43/12/122802

1. Introduction

As one of the representatives of the wide bandgap semiconductor materials, silicon carbide (SiC) has competitive advantages such as, high critical breakdown electric field, high thermal conductivity and high electron mobility compared with the traditional material of silicon (Si). In addition, the maturity of SiC technology makes it more and more recognizable and available for academia and industry. Therefore, SiC is one of the promising candidates to replace Si and is widely used in power semiconductor devices, such as metal–oxide–semiconductor field effect transistor (MOSFETs), insulated gate bipolar transistor (IGBTs), etc[1, 2].

In particular, SiC MOSFETs have the characteristics of easy driving, high switching frequency, and low loss, enabling them show great advantages in new energy vehicles and charging facilities[3–5]. Power MOSFET includes two kinds of prototypes, namely vertical double-diffused MOSFET (VDMOSFET) and trench MOSFET (UMOSFET). It is attributed to the reason that SiC UMOSFET has the advantages of small cell and high channel mobility compared to the VDMOSFET. Accordingly, the investigation into SiC UMOSFET is gaining more and more attention in the power electronics field[6].

However, there are also many potential challenges, such as electric field accumulation at the corner of the trench, unreliability of the gate oxide layer, and instability of the threshold voltage[7, 8], hindering their practical use for SiC UMOSFET. One of the critical issues is solved by adding a p-shield layer under the trench to reduce the maximum electric field ($E_{ox\text{-}max}$) at the trench corner of the gate oxide. However, the p-shield brings the junction field effect transistor (JFET) effect, which increases the overall on-resistance of the device[9–13]. Generally, there is a trade-off between the on-resistance of the device and the electric field of the gate oxide. The reduction of the electric field of the gate oxide is at the expense of increasing the on-resistance or power loss of the device[14]. With regard to the switching losses, large miller capacitance (C_{GD}) introduced by the gate-drain overlap has become the dominated challenge, affecting the high-frequency

Correspondence to: Z W Shen, zwshen@semi.ac.cn; F Zhang, fzhang@xmu.edu.cn

Received 2 MAY 2022; Revised 6 SEPTEMBER 2022.

©2022 Chinese Institute of Electronics

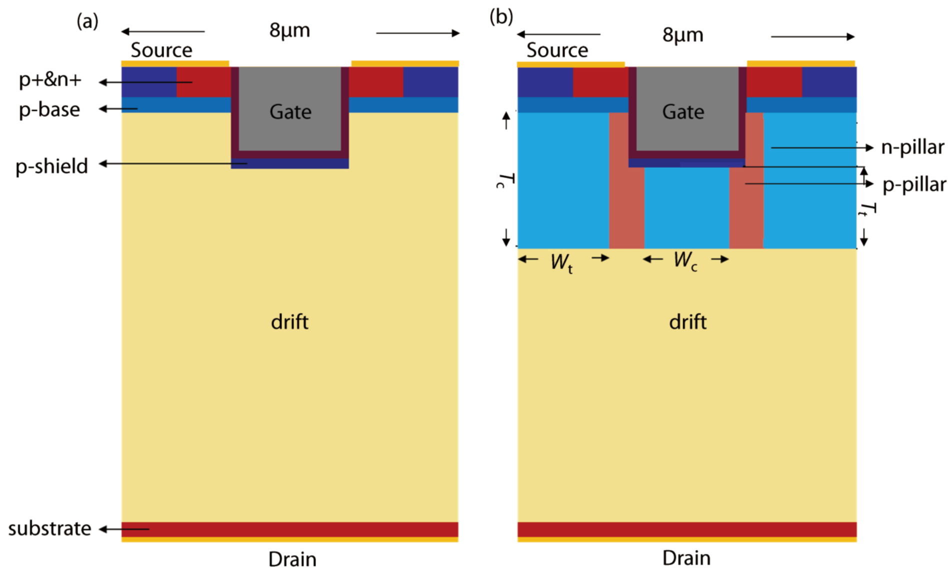

Fig. 1. (Color online) Schematic cross-sections of (a) the CT-UMOS and (b) proposed SS-UMOS (G & NG) (Please refer to Table 1 for detailed parameters).

Table 1. Device parameters for CT-UMOS and SS-UMOS (G & NG).

Device parameter	CT-UMOS	SS-UMOS
p-body junction depth (μm)	0.5	0.5
p+ junction depth (μm)	0.2	0.2
Gate trench depth (μm)	1.8	1.8
Thickness of n-drift (μm)	12	12
n-pillar depth (T_t) (μm)	–	1.5
p-pillar depth (T_t) (μm)	–	1.5
n-pillar depth (T_c) (μm)	–	2.8
p-pillar depth (T_c) (μm)	–	2.8
p-pillar width (W_c) (μm)	–	2.2
p-pillar width (W_t) (μm)	–	1.6
Width of trench (μm)	2.0	2.0
n-drift doping concentration (10^{15} cm^{-3})	1.0	1.0
p-body doping concentration (10^{17} cm^{-3})	1.0	1.0
p-pillar doping concentration (10^{16} cm^{-3})	–	3.0
n-pillar doping concentration (10^{16} cm^{-3})	–	2.0

power consumptions in a single period interval. Therefore, a new work needs to be proposed to ensure that the device has low C_{GD} and $E_{ox\text{-}max}$, which can make the device separately attain low switching loss and high breakdown voltage. Herein, adding a super-junction structure to a trench MOSFET can alleviate the negative effects of the trench structure while maintaining the advantages of the trench structure. Thus, it achieves a superior trade-off between the static and dynamic performances of SiC trench MOSFET[15–24].

As shown in Fig. 1, a semi-super-junction UMOSFET structure (SS-UMOS), with p-pillars and n-pillars added under the channels and trench regions, is proposed in this paper[25, 26]. All the devices are simulated by TCAD. In addition to the comparison with CT-UMOS, this work also presents the effect of p-pillar's bias conditions (grounded or ungrounded) on the electrical characteristics of SS-UMOS on the device. The detailed simulation parameters of the structure are listed in Table 1. The physical models of Shockley-Read-Hall, Auger, and incomplete dopants are involved in all structures. In addition, the 1×10^{12} cm^{-2} positive charge captured at the SiC–SiO_2 interface is included in the devices[27–29]. The simulation results show that SS-UMOS has lower on-resistance, higher breakdown voltage and smaller switching losses compared with the conventional UMOSFETs (CT-UMOS). A discussion of possible manufacturing processes is described in detail. The parameters used in the simulation have been carefully optimized to achieve low $E_{ox\text{-}max}$ and $R_{on,sp}$, and improve the dynamic performance of the device[29–31].

2. Structures and manufacturability

The manufacturability of the proposed SiC UMOSFET relies on advanced photolithographic and etching technique. Based on the process-related experiences obtained by other research groups[23, 25, 26], the primary analysis of the process flow is beneficial for the proposed device to achieve a manufacturable solution in the future. Fig. 2 shows a process flow of the proposed structure in this paper. It can be seen from Fig. 2(a) that the sandwich p–n epitaxial layers, from bottom to top, are epitaxially grown on the SiC substrate, which are the first epitaxial layer and the second epitaxial layer, with doping concentration of 1×10^{15} and 3×10^{16} cm^{-3}, respectively. Next, periodically arranged trenches with depth of 2.8 μm were etched with HF in the p-pillar, as shown in Fig. 2(b). Then, as shown in Fig. 2(c), epitaxial backfill is performed to form n-pillars, with doping concentration of 2×10^{16} cm^{-3}. Afterwards, as shown in Fig. 2(d), the third epitaxial layer is grown on the p- and n-pillars to form p-base with thickness of 0.7 μm and doping concentration of 1×10^{17} cm^{-3}. Besides, in Fig. 2(e), high-energy ion implantation is performed to form n+ and p+ source region. The source doping is 1×10^{19} cm^{-3}. Then, the gate trench is etched by reactive ion etching (RIE). The p-shield layer is formed on the surface of the p–n pillars at the bottom of the trench by multiple high-energy implants, as shown in Fig. 2(f). Subsequently, gate oxidation is performed by high temperature thermal oxidation to form an oxide layer with a thickness of 50 nm at the bottom of the trench. Also, NO annealing is conducted to increase the channel mobility and reduce the interface state density. As shown in Fig. 2(g), the polysilicon is formed by low pressure chemical vapor deposition, and the doped polysilicon is

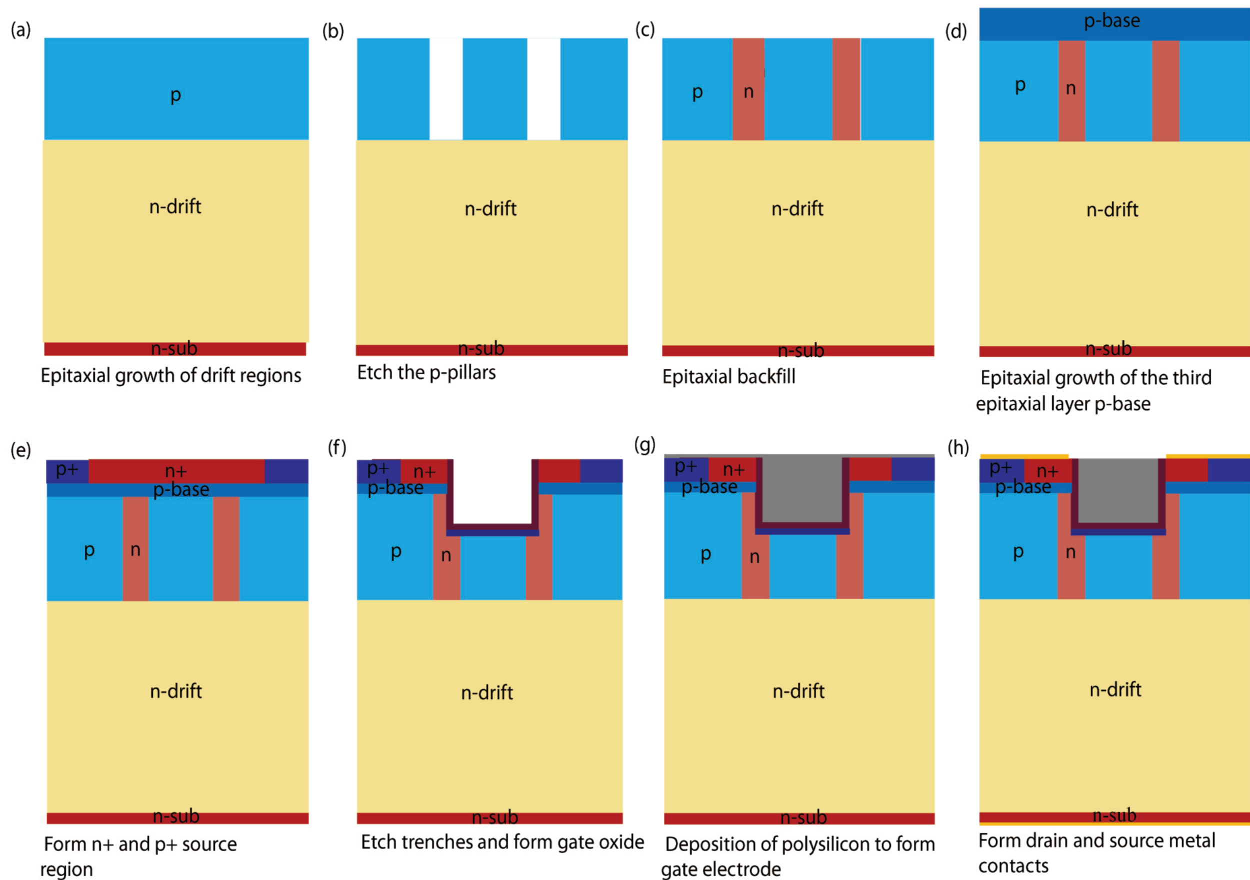

Fig. 2. (Color online) Process flow of the proposed SS-UMOS (G & NG) structure of SiC MOSFET.

deposited by etch back and planarization process. Finally, the source and drain are defined by ohmic alloys and are metallized to form source and drain contacts, as shown in Fig. 2(h).

3. Simulation results and discussion

3.1. Static characteristics

The transfer characteristics of the two structures are shown in Fig. 3. Then the threshold voltage (V_T) is determined by finding linear extrapolation of the static transfer drain current curve at its maximum first derivative (slope) point. V_T of them shows approximately the same, value of 5 V, due to the identical channel dopants and oxide condition. As shown in Fig. 1(b), the current conduction path of SS-UMOS is narrower compared with that of CT-UMOS. Because the higher electron concentration occurs in the accumulation layer, leading to higher saturation current density in the proposed structure (G & NG).

Fig. 3(b) shows the output characteristics of the two structures. The drain current versus drain voltage curves are given at the gate voltage (V_{GS}) of 15 V. From the figure, it can be concluded that the on-resistance of CT-UMOS is 6.2 mΩ·cm^2, while the specific on-resistance ($R_{on,sp}$) of GSS-UMOS and NGSS-UMOS are 3 and 1.8 mΩ·cm^2, respectively, when the gate voltage is 15 V and the drain current density (I_{DS}) is 500 A/cm^2. The on-resistance of SS-UMOS is reduced by 52% (G) and 71% (NG) compared to CT-UMOS. Due to the contact resistance, channel resistance and substrate resistance of the proposed device are approximately the same as those of the CT-UMOS. The difference in the on-resistance of the two structures mainly comes from the resistance near the JFET regions. Due to the proposed structure has highly doped n-pillars, it can simultaneously provide higher density electrons in the accumulated layer of the gate surface and higher density conduction electrons in the JFET region, a lower specific on-resistance is achieved in the SS-UMOS[32]. Additionally, for the on-state of the GSS-UMOS, the positive charges move toward the bottom of the p-shield regions and attract a large number of electrons near the p-pillar region under the trench bottom. Then the recombination of the carrier process occurs in the grounded electrodes. Therefore, a quasi-intrinsic region is formed at the trench bottom, reducing the conduction path of the JFET regions in the device. However, this phenomenon does not occur in NGSS-UMOS. Thus, GSS-UMOS has the larger on-resistance than the NGSS-UMOS. Figs. 3(c) and 3(d) show the comparisons of current density of the two structures at the gate voltage of 15 V, drain voltage (V_{DS}) of 20 V. The SS-UMOS (G and NG) has higher total current density in the drift and channel regions, demonstrating good agreement with the aforementioned results. Therefore, the device has superior forward conduction characteristics in comparison to the CT-UMOS[15, 33].

Fig. 4(a) shows the breakdown characteristic of the two structures. The breakdown voltage of the traditional structure is 1240 V. However, compared to the CT-UMOS , the breakdown voltage of the SS-UMOS has been increased by 23% (NG) and 41% (G), and the corresponding avalanche breakdown occurred at 1530 and 1750 V, respectively. Furthermore, Figs. 4(b) and 4(c) show the electric field distribution of the CT-UMOS and GSS-UMOS at 1200 V. It can be seen from the figure that the peak electric field ($E_{ox\text{-}max}$) of the tradition-

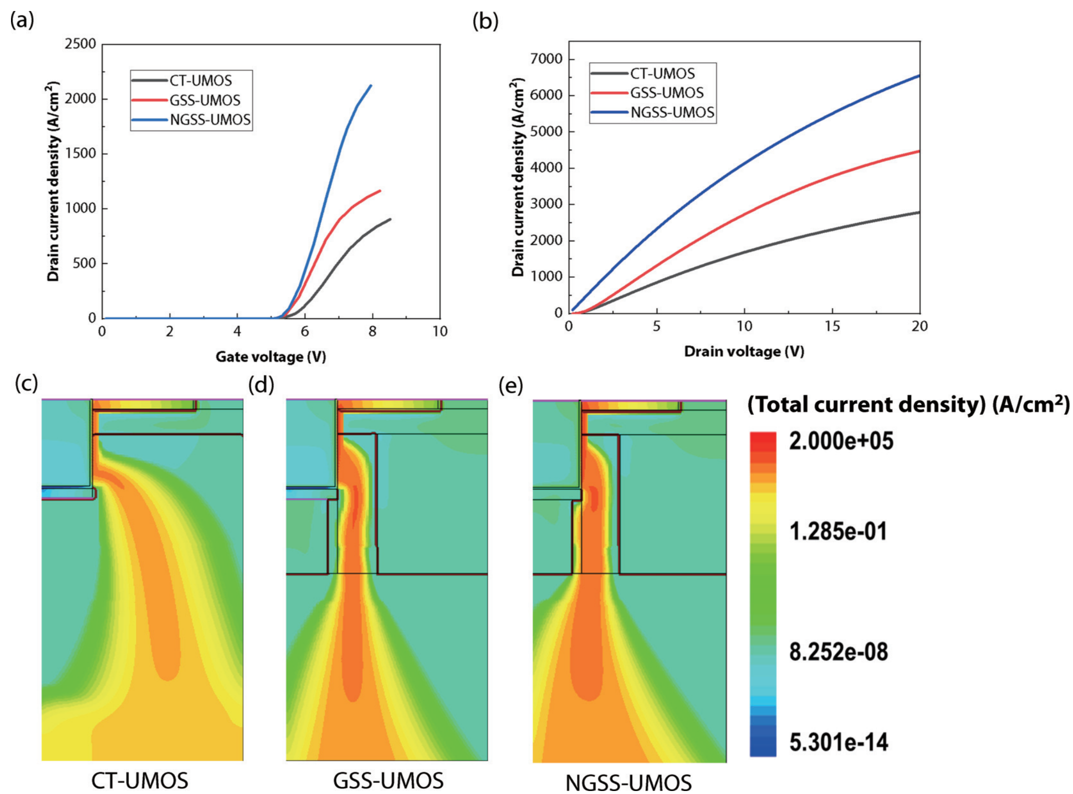

Fig. 3. (Color online) (a) The transfer characteristic curves (V_{DS} = 5 V), (b) output characteristic curves and current density of (c) CT-UMOS, (d) GSS-UMOS, (e) NGSS-UMOS. (V_{GS} = 15 V, V_{DS} = 20 V)

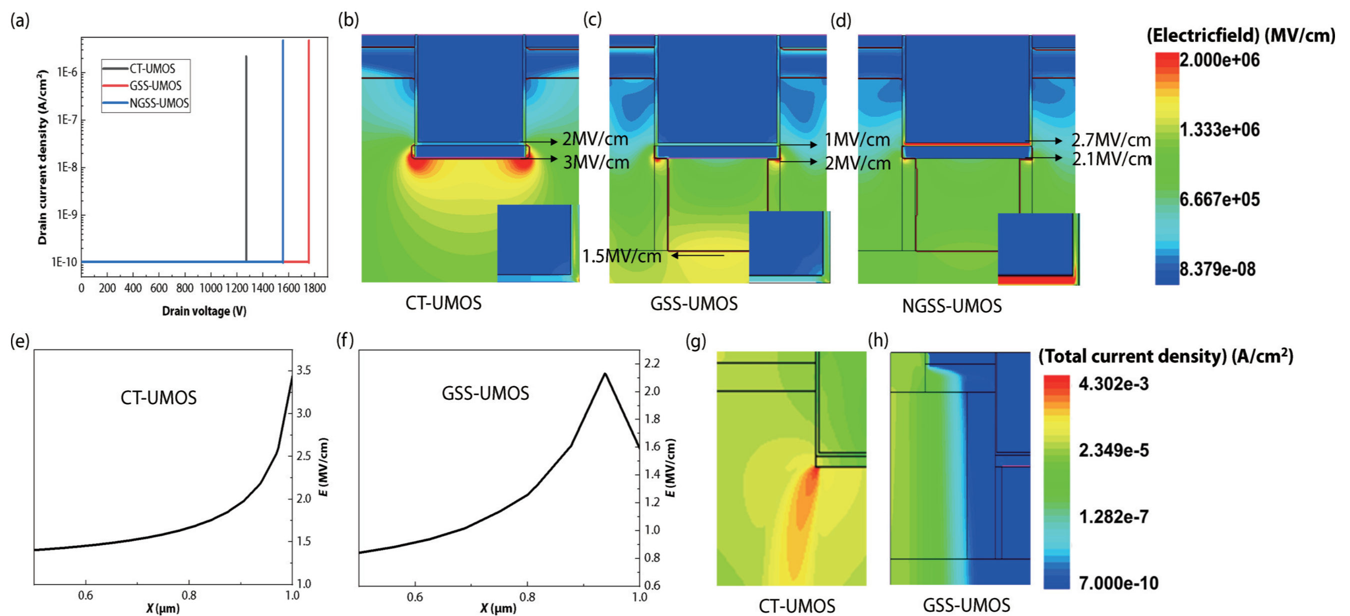

Fig. 4. (Color online) (a) Breakdown characteristic curves, (b–d) corresponding electric field distributions (V_{GS} = 0 V, V_{DS} = 1200 V), two-dimensional electric fields of (e) CT-UMOS and (f) GSS-UMOS (V_{GS} = 0 V, V_{DS} = 1200 V), and current density distribution of (g) CT-UMOS and (h) GSS-UMOS at breakdown voltage.

al structure, with a value of 3 MV/cm, occurs at the corner of the p-shield under the trench. The peak electric field of the GSS-UMOS emerges in the same location and the maximum electric field drops to 2 MV/cm. Owing to the super-junction structure under the p-shield layer establishes new charge balance, weakening the influence of interfacial parasitic charges, the electric field crowding effect at the corners is alleviated. Then it completely depletes the pillar region to form an intrinsic semiconductor region, leading to the formation of the strong lateral shielding field under the trench. In the avalanche breakdown region, it has a smoother transverse electric field lines as shown in Figs. 4(e) and 4(f). Thus, the breakdown voltage of GSS-UMOS is higher. Besides, Fig. 4(d) shows the electric field distribution of the device when it is not grounded at 1200 V. When the p-pillar is floating, the coupling effect between the n-pillar and the p-pillar is weakened, resulting in a decrease in the degree of depletion of the p-pillar at the bottom of the trench compared to that in the grounded

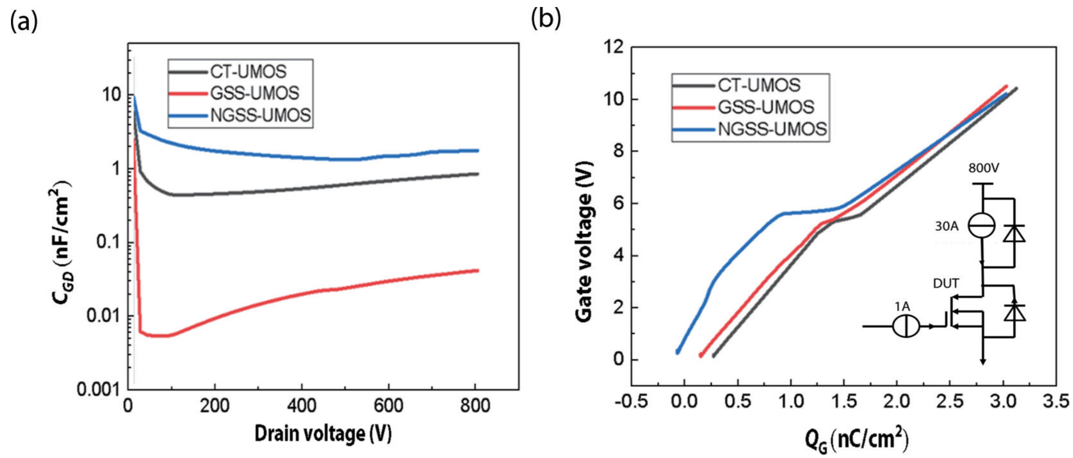

Fig. 5. (Color online) (a) Feedback capacitance C_{GD} as a function of drain voltage V_{DS} at gate voltage V_{GS} = 0 V and (b) voltage V_{GS} as a function of gate charge Q_G and the inset is the testing circuit for Q_G.

device. Thus, the shielding effect of the trench corner oxide is weakened in NGSS-UMOS[34].

Meanwhile, it can be seen from Figs. 4(b) and 4(c) that the critical gate oxide electric field (E_{ox}) of the GSS-UMOS is about 1 MV/cm, which is lower than that of the CT-UMOS with the value of approximately 2 MV/cm. The reduction of the gate oxide electric field in GSS-UMOS is due to the fact that the additional p-pillars under the p-shield layer of the proposed structure can act as terminal centers for the electric field lines, thereby reducing the electric field crowding effect at the oxidized corners[9]. Figs. 4(g) and 4(h) show the current density at breakdown voltage. It is worth noting that the current density lines in GSS-UMOS are more concentrated between p-pillars and n-pillars compared to CT-UMOS. From the perspective of device reliability, strong protection effect of trenches can be achieved in GSS-UMOS. Since hot carriers may be injected into the corner oxide layer of CT-UMOS, this will have a negative impact on the long-term reliability of the device. In consideration of these results, the proposed GSS-UMOS can effectively prevent device failure and improve the avalanche capability of the device, owing to the improved thermal relaxation ability at the corner of the trench[35–38].

3.2. Dynamic characteristics

The following section mainly compares the dynamic performance of the devices. Fig. 5(a) shows the feedback capacitance (C_{GD}) of the two structures by utilizing AC simulation. When the device is grounded, the super-junction structure at the bottom of the trench is completely depleted to form intrinsic semiconductor with strong shielding effect, which greatly weakens the coupling between the gate and drain electrodes. Therefore, the feedback capacitance of GSS-UMOS is greatly reduced. For NGSS-UMOS, the depletion of positive and negative charges in the super-junction structure is incomplete due to the effect of device doping. The device is affected by parasitic charges, resulting in significant decrease in the shielding effects which is even worse than the CT-UMOS. In addition, the parasitic capacitance of the high-voltage super-junction structure has relatively sudden change during the switching transient. It can be quickly reduced at a lower drain–source voltage, which allows the device to exhibit extremely fast dV/dt and dI/dt characteristics, turn-off delay is improved. Thus, a reduced switching loss can be achieved due to short gate charging time, corresponding to short cross-coupling time intervals between the drain current and voltage[39–42].

The gate charges (Q_G) are obtained by using the mix-mode simulation. Testing circuit for Q_G is shown in the Fig. 5(b). The gate charge is one of the key parameters affecting the switching speed of the MOSFET. Especially, the gate–drain charge (Q_{GD}) is the charge required for the MOSFET to pass the "amplification process" during the transition from on-state to off-state or from off-state to on-state, and it significantly influences the switching losses of the devices. At the same gate–source voltage, the NGSS-UMOS shows maximum plateau charge (Q_{GD}) of about 450 nC/cm^2, which is consistent with the aforementioned large increase in C_{GD}. In addition, the Q_{GD} of GSS-UMOS is 80 nC/cm^2 and is 65% lower than that of CT-UMOS with a value of 250 nC/cm^2, thereby reducing the switching loss of the device[43]. Firstly, the reduction of the gate capacitance decreases the charge and discharge of the gate under the same driving current and time. Secondly, when the MOSFET is turned off, the high doping of the p+ region can quickly recombine with the carrier electrons, resulting in a faster decrease in the carrier concentration[44].

Fig. 6(a) shows the double-pulse testing circuit used to conduct the simulations of switching characteristics. The area of the SiC MOSFET is set to be 0.02 cm^2. Several parameters in simulation design are given as follows: The gate resistor (R_G) is 1 Ω, the supply voltage is V_{DD} = 800 V, an inductive load (L_L) is 100 μH, and the wire resistance (R) is 1 Ω. The amplitude of the gate voltage is switched between 0 and 20 V in order to turn-on and turn-off the device[45, 46]. Fig. 6(b) is the waveforms of the voltage and current. It can be seen that the device is turned on at the time of 1 μs, and the turn-on process is completed when the drain voltage waveform drops to a horizontal state. While the device is turned off at 5 μs at 33 kHz (4 μs at 50 kHz; 7 μs at 75 kHz) and the turn-off process is completed when the drain voltage rises to a horizontal voltage of 800 V. In addition, the current will have a spike when the device is turned on. Due to the resonance caused by the influence of parasitic inductance, trace inductance, etc. in high-frequency fast switching.

Fig. 6 also shows corresponding turn-on and turn-off transients at different switching frequencies. Fig. 6(c) shows a de-

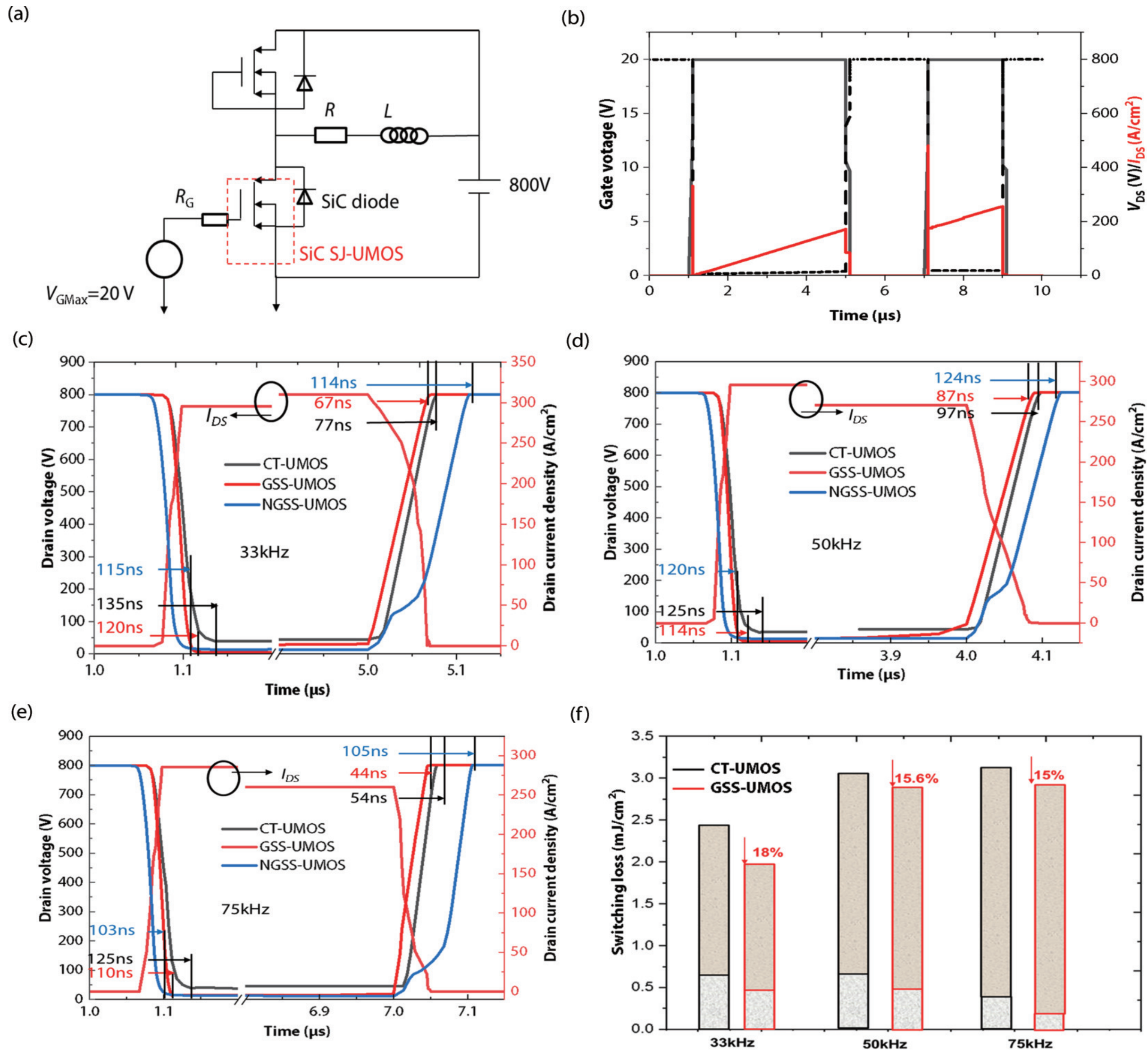

Fig. 6. (Color online) (a) Test circuit of switch characteristics, (b) voltage and current characteristic of the GSS-UMOS in the switching transients, (c) detailed comparisons of the turn-on and turn-off transients for the CT-UMOS and SS-UMOS (G & NG) at switching frequency of 33 kHz, (d) the switching frequency is 50 kHz, (e) the switching frequency is 75 kHz, (f) comparison of the switching loss at different switching frequencies.

tailed comparison of turn-on and turn-off transients of the two structures at 33 kHz. The turn-on time (T_{on}) of the CT-UMOS and GSS-UMOS are 135 and 120 ns, respectively. Likewise, the GSS-UMOS exhibits shorter turn-off time (T_{off}) of 67 ns than that of 77 ns in the CT-UMOS, which is due to the fact that the carriers in the super-junction can be depleted both laterally and vertically. Moreover, the GSS-UMOS has less gate charges and gate capacitances compared to the CT-UMOS so that faster switching transients can be attained, which reduces turn-on and turn-off time and power dissipation[47]. Besides, switching transients are affected by changing the doping concentrations of the p- and n-pillars of the super-junction structure. When the negative charge in the n-pillars is much higher than the positive charge in the p-pillars, the turn-on time of the device decreases and the turn-off transient of the device is delayed. Conversely, the turn-off transient can be improved, but it is detrimental to the decrease of turn-on time of the device. Therefore, the super-junction structure plays important role in realizing the switching transient trade-off[48].

Fig. 6(d) is the comparison of the turn-on transients and turn-off transient comparisons at 50 kHz. It can be seen that when the switching frequency is 50 kHz, the turn-on and turn-off times of CT-UMOS are 125 and 97 ns, respectively, and the corresponding times of GSS-UMOS are 114 and 87 ns, respectively. Meanwhile, GSS-UMOS has faster switch response time at 75 kHz corresponding comparison of switching loss is given in Fig. 6(e). However, in the switching transients for different frequencies, it can be seen that the turn-on time of NGSS-UMOS is about 5 μs faster than that of GSS-UMOS. The turn-off time period rises substantially, and the total switching time is even larger than that of CT-UMOS. This is attributed to the reason that NGSS-UMOS has larger feedback transfer capacitance and platform charge than CT-UMOS and GSS-UMOS. It can be further concluded that grounding is an indispensable step for the optimization of device design.

Fig. 6(f) plots the total switching loss (E_{total}) comparison of the two structures at different switching frequencies. E_{total} includes the turn-on loss (E_{on}) and the turn-off loss (E_{off}) which are listed in Table 2. The turn-on and turn-off losses of CT-UMOS are 1.7 and 0.7 mJ/cm^2, respectively. However, they

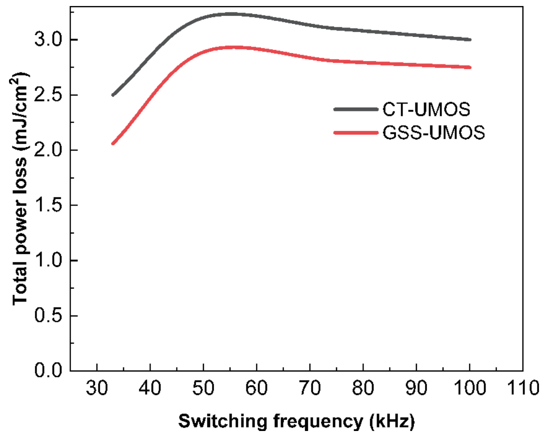

Fig. 7. (Color online) The relationship between the total power loss and switching frequency.

are 1.5 and 0.45 mJ/cm^2, respectively in GSS-UMOS. The total switching loss has been reduced by approximately 18%.

The switching characteristics obtained by the dynamic simulations in this paper are in approximately identical order of magnitude with those of reported literature and measurement results of MOSFET products[17, 49–51]. Therefore, the error of this work is within the allowable range. The switching losses of proposed structure at the switching frequencies of 33, 50 and 75 kHz are 1950, 2800 and 2730 μJ/cm^2, respectively. It can be seen that the switching losses of the device do not increase with the switching frequency. However, as the switching frequency increases, the improvement in device's switching losses decreases. This is because the increment in switching frequency leads to decrease of the conversion efficiency for the device. In addition to the losses caused by the turn-on and turn-off transients of the device, the device will also produce Ein when it is turned on. The corresponding calculation formula can be obtained as follows (IRMS is the inductor effective current). According to the formula, it is obvious that the conduction loss of the GSS-UMOS per unit time is smaller than that of CT-UMOS, and it increases in proportion to the time intervals[1–3].

$$E_{\rm ON} = \int_{T_1}^{T_2} V_{\rm DS}(t)\, I_{\rm DS}(t)\, {\rm d}t,$$

$$E_{\rm OFF} = \int_{T_3}^{T_4} V_{\rm DS}(t)\, I_{\rm DS}(t)\, {\rm d}t,$$

$$E_{\rm IN} = I_{\rm RMS}^2 R_{\rm ON} T.$$

Therefore, the total power losses are not only related to turn-on and turn-off losses, but are also affected by conduction losses. As shown in Fig. 7, the total power loss of the proposed device shows a decreasing trend after 50 kHz. However, excessive switching frequency can cause reduced conversion efficiency and EMI of the device. In general, SiC MOSFETs operate between 85 and 125 kHz. Therefore, a certain switching frequency in the range from 50 to 125 kHz is acceptable for the operation frequency of the proposed MOSFET's, so as to achieve a compromise between switching frequency and switching loss in practical work. Anyway, the optimal operating frequency of the device can also be obtained by testing the device depending on the real applications[49].

Table 2. Comparisons of the characteristics for the CT-UMOS and the SS-UMOS (G & NG).

Parameter	CT-UMOS	GSS-UMOS	NGSS-UMOSr
$I_{\rm sat}$ (kA/cm^2)	2.40	3.90	6.70
$R_{\rm on,sp}$ (mΩ·cm^2)	6.20	3.00	1.80
BV (V)	1240	1750	1530
$E_{\rm ox\text{-}max}$ (MV/cm)	3.00	2.20	2.70
$E_{\rm ox}$ (MV/cm)	1.50	1.00	2.70
$E_{\rm total}$ (mJ/cm^2)	2.40	1.95	–
FOM (kV^2/(mΩ·cm^2))	0.26	0.90	1.30
$Q_{\rm GD}$ (nC/cm^2)	245	80	450
$Q_{\rm G}$ (nC/cm^2)	3028	2922	2980
$C_{\rm iss}$ (nF/cm^2)	67	30	108
$Q_{\rm GD}$·$R_{\rm on,sp}$ (mΩ·nC)	1550	240	810

Table 2 gives the comparison of the electrical characteristics of the CT-UMOS and SS-UMOS (G & NG). $I_{\rm sat}$ is obtained at $V_{\rm DS}$ = 20 V and $V_{\rm GS}$ = 15 V; $R_{\rm on,sp}$ is obtained at $V_{\rm GS}$ = 10 V and $I_{\rm DS}$ = 500 A/cm^2; $Q_{\rm G}$ is obtained at $V_{\rm DS}$ = 20 V and $V_{\rm GS}$ = 10 V; $C_{\rm iss}$ is obtained at $V_{\rm DS}$ = 0 V. It can be seen from the Table 2 that the higher saturation current density at gate voltage of 15 V is obtained due to the presence of the highly doped n-pillar, leading to the decreased on-resistance. The existence of the super-junction structure relieves the electric field crowding effect at the corners of the p-shield layer, which enables it to have a higher breakdown voltage. The strong shielding effect of the super-junction structure weakens the coupling between the gate and drain electrodes, thus reducing the feedback capacitance and gate charge in the device. Also, the charge compensation effect of the super-junction also helps to reduce excessive gate charges in the device. Therefore, switching losses are reduced with decreased capacitance and platform charge in the GSS-UMOS.

4. Summary

This article proposes a 4H-SiC UMOSFET with alternating p-pillars and n-pillars under the trench and p-base regions. Simulated results demonstrated that the specific on-resistance of the GSS-UMOS is 52% lower than the CT-UMOS. The breakdown voltage is increased by 41% with respect to the CT-UMOS, avoiding the premature breakdown caused by the excessively high electric field at the corner of the gate oxide. Furthermore, the dynamic characteristics of the GSS-UMOS have also been improved. The total switching loss of the GSS-UMOS is 1.95 mJ/cm^2, which is 18% lower than that of the traditional structure. Although NGSS-UMOS has the lowest on-resistance, the floating p-pillars has a significant impact on the voltage withstand capability of the device and the reliability of the gate oxide layer, and greatly increase the switching losses of the device. These results show that the p-shield grounding is very important for the accuracy of the device design, and the performance of GSS-UMOS has been comprehensively improved.

Acknowledgements

This work was supported by the National Natural Science Foundation of China (Grant No. 62104222), the Natural

Science Foundation of Fujian Province of China for Distinguished Young Scholars (Grant No. 2020J06002), the Science and Technology Project of Fujian Province of China (Grant No. 2020I0001), the Science and Technology Key Projects of Xiamen (Grant No. 3502ZCQ20191001), Shenzhen Science and Technology Program (Grant No. JSGG20201102-155800003), Jiangxi Provincial Natural Science Foundation (Grant No. 20212ACB212005).

References

[1] Shin G, Lee W C. High frequency switching inverter using Si and SiC. J Korean Institute Illumin Electr Instal Eng, 2017, 31, 45

[2] Hatakeyama T, Watanabe T, Shinohe T, et al. Impact ionization coefficients of 4H silicon carbide. Appl Phys Lett, 2004, 85, 1380

[3] Gao Y, Huang A, Krishnaswami S, et al. Comparison of static and switching characteristics of 1200V 4H-SiC BJT and 1200V Si-IGBT. Conf Rec IAS Annu Meet IEEE Ind Appl Soc, 2006, 1, 325

[4] Hosseini Aghdam G. Comparison of Si and SiC power semiconductor devices in power electronics converters to be used in plug-In hybrid electric vehicles. EPE J, 2012, 22, 20

[5] Jordan J, Esteve V, Sanchis-Kilders E, et al. A comparative performance study of a 1200 V Si and SiC MOSFET intrinsic diode on an induction heating inverter. IEEE Trans Power Electron, 2013, 29, 2550

[6] Nayak P, Hatua K. Parasitic inductance and capacitance-assisted active gate driving technique to minimize switching loss of SiC MOSFET. IEEE Trans Ind Electron, 2017, 64, 8288

[7] Wang D B, Feng Q Y, Chen X P, et al. Failure analysis and improvement of 60 V power UMOSFET. Microelectron Reliab, 2014, 54, 2782

[8] Juang M H, Chen W T, Ou-Yang C I, et al. Fabrication of trench-gate power MOSFETs by using a dual doped body region. Solid State Electron, 2004, 48, 1079

[9] Kim T, Kim K. High breakdown voltage and low on-resistance 4H-SiC UMOSFET with source-trench optimization. ECS J Solid State Sci Technol, 2019, 8, Q147

[10] Onishi Y, Hashimoto Y. Numerical analysis of specific on-resistance for trench gate superjunction MOSFETs. Jpn J Appl Phys, 2015, 54, 024101

[11] Wang Y, Lan H, Cao F, et al. A novel power UMOSFET with a variable *K* dielectric layer. Chin Phys B, 2012, 21, 068503

[12] Wang Y, Ma Y C, Hao Y, et al. Simulation study of 4H-SiC UMOSFET structure with p^+-polySi/SiC shielded region. IEEE Trans Electron Devices, 2017, 64, 3719

[13] Zou X, Wu Z M, Wang W P, et al. Optimized design of 4H-SiC UMOSFET for high breakdown voltage. Proc SPIE 11567, AOPC 2020: Optical Sensing and Imaging Technology, 2020, 11567, 939

[14] Jozi M, Orouji A A, Fathipour M. Control of electric field in 4H-SiC UMOSFET: Physical investigation. Phys E, 2016, 83, 107

[15] Roig J, Stefanov E, Morancho F. Thermal behavior of a superjunction MOSFET in a high-current conduction. IEEE Trans Electron Devices, 2006, 53, 1712

[16] Chen Y, Liang Y C, Samudra G S, et al. Progressive development of superjunction power MOSFET devices. IEEE Trans Electron Devices, 2008, 55, 211

[17] Xia Y, Chen W J, Sun R Z, et al. A superjunction MOSFET with ultralow reverse recovery charge and low switching losses. J Electron Mater, 2021, 50, 6297

[18] Goh J, Kim K. Low on-resistance 4H-SiC UMOSFET with local floating superjunction. J Comput Electron, 2020, 19, 234

[19] Saito W, Omura I, Aida S, et al. Semisuperjunction MOSFETs: New design concept for lower on-resistance and softer reverse-recovery body diode. IEEE Trans Electron Devices, 2003, 50, 1801

[20] Saxena R S, Kumar M J. Polysilicon spacer gate technique to reduce gate charge of a trench power MOSFET. IEEE Trans Electron Devices, 2012, 59, 738

[21] Wang Y, Liu Y J, Yu C H, et al. A novel trench-gated power MOSFET with reduced gate charge. IEEE Electron Device Lett, 2015, 36, 165

[22] Feng H, Yang W T, Onozawa Y, et al. A new fin p-body insulated gate bipolar transistor with low miller capacitance. IEEE Electron Device Lett, 2015, 36, 591

[23] Kim S G. Fabrication of superjunction trench gate power MOSFETs using BSG-doped deep trench of p-pillar. ETRI J, 2013, 35, 632

[24] Huang Q Y, Huang A Q. Hybrid low-frequency switch for bridgeless PFC. IEEE Trans Power Electron, 2020, 35, 9982

[25] Huh Y Y, Choi J M, Kim J M, et al. A study on the optimization of deep-trench super junction metal oxide semiconductor field-effect transistor. J Nanoelectron Optoelectron, 2021, 16, 781

[26] Saito W, Omura I, Aida S, et al. Over 1000V semi-superjunction MOSFET with ultra-low on-resistance below the Si-limit. The 17th International Symposium on Power Semiconductor Devices and ICs, 2005, 27

[27] Vudumula P, Kotamraju S. Design and optimization of SiC superjunction MOSFET using vertical variation doping profile. IEEE Trans Electron Devices, 2019, 66, 1402

[28] Wang Y, Hu H F, Yu C H, et al. High-performance split-gate enhanced UMOSFET with p-pillar structure. IEEE Trans Electron Devices, 2013, 60, 2302

[29] Kobayashi Y, Kyogoku S, Morimoto T, et al. High-temperature performance of 1.2 kV-class SiC super junction MOSFET. 2019 31st International Symposium on Power Semiconductor Devices and ICs, 2019, 31

[30] Masuda T, Saito Y, Kumazawa T, et al. 0.63 $m\Omega\cdot cm^2$/1170 V 4H-SiC super junction V-groove trench MOSFET. 2018 IEEE International Electron Devices Meeting, 2018

[31] Okada M, Kyogoku S, Kumazawa T, et al. Superior short-circuit performance of SiC superjunction MOSFET. 2020 32nd International Symposium on Power Semiconductor Devices and ICs, 2020, 70

[32] Shen P, Wang Y, Li X J, et al. Improved 4H-SiC UMOSFET with super-junction shield region. Chin Phys B, 2021, 30, 058502

[33] Cha K, Kim K. 3.3 kV 4H-SiC DMOSFET with a source-contacted dummy gate for high-frequency applications. J Semicond, 2021, 42, 062801

[34] Luo X R, Liao T, Wei J, et al. A novel 4H-SiC trench MOSFET with double shielding structures and ultralow gate-drain charge. J Semicond, 2019, 40, 052803

[35] Wei J, Zhang M, Jiang H P, et al. Superjunction MOSFET with dual built-In Schottky diodes for fast reverse recovery: A numerical simulation study. IEEE Electron Device Lett, 2019, 40, 1155

[36] Kang H, Lee J, Lee K, et al. Trench angle: A key design factor for a deep trench superjunction MOSFET. Semicond Sci Technol, 2015, 30, 125008

[37] Wang Y D, Duan B X, Zhang C, et al. AC-SJ VDMOS with ultra - low resistance. Micro Nano Lett, 2020, 15, 230

[38] Tian R, Ma C, Wu J M, et al. A review of manufacturing technologies for silicon carbide superjunction devices. J Semicond, 2021, 42, 061801

[39] Shen Z W, Zhang F, Yan G G, et al. High-frequency switching properties and low oxide electric field and energy loss in a reverse-channel 4H-SiC UMOSFET. IEEE Trans Electron Devices, 2020, 67, 4046

[40] Kim M, Forbes J J, Hirsch E A, et al. Evaluation of long-term reliability and overcurrent capabilities of 15-kV SiC MOSFETs and 20-kV SiC IGBTs during narrow current pulsed conditions. IEEE Trans Plasma Sci, 2020, 48, 3962

[41] Appaswamy A, Chakraborty P, Cressler J D. Influence of interface traps on the temperature sensitivity of MOSFET drain-current variations. IEEE Electron Device Lett, 2010, 31, 387

[42] Chen R Z, Wang L X, Jiu N X, et al. Simulation and result analysis of split gate resurf stepped oxide UMOFSET with floating elec-

trode for improved performance. Electronics, 2019, 8, 1553
[43] Yoon J, Kim K. A 3.3 kV 4H-SiC split gate MOSFET with a central implant region for superior trade-off between static and switching performance. J Semicond, 2021, 42, 062803
[44] Chen R Z, Wang L X, Zhang H K, et al. A new split gate resurf stepped oxide UMOSFET structure with high doped epitaxial layer for improving figure of merit (FOM). Appl Sci, 2020, 10, 7895
[45] Wang Y, Hu H F, Wang L G, et al. Split gate resurf stepped oxide UMOSFET with p-pillar for improved performance. IET Power Electron, 2014, 7, 965
[46] Ahmad S S, Narayanan G. Double pulse test based switching characterization of SiC MOSFET. 2017 National Power Electronics Conference, 2017, 319
[47] Wang Y, Jiao W L, Hu H F, et al. Split-gate-enhanced power UMOSFET with soft reverse recovery. IEEE Trans Electron Devices, 2013, 60, 2084
[48] Liu Q, Wang Q, Liu H, et al. Low on-resistance 1.2 kV 4H-SiC power MOSFET with $R_{on, sp}$ of 3.4 mΩ· cm^2. J Semicond, 2020, 41, 062801
[49] Han Z, Song G, Bai Y, et al. A novel 4H-SiC MOSFET for low switching loss and high-reliability applications. Semicond Sci Technol, 2020, 35, 085017
[50] Tian K, Hallén A, Qi J W, et al. An improved 4H-SiC trench-gate MOSFET with low ON-resistance and switching loss. IEEE Trans Electron Devices, 2019, 66, 2307
[51] An J J, Hu S D. Heterojunction diode shielded SiC split-gate trench MOSFET with optimized reverse recovery characteristic and low switching loss. IEEE Access7, 2019, 7, 28592

Xiaojie Wang is a graduate student at the School of Physical Science and Technology, Xiamen University. His current research interests are the design, simulation and fabrication of SiC MOSFET devices, as well as the corresponding research on radiation resistance.

Zhanwei Shen is currently an Assistant Professor with Institute of Semiconductors, Chinese Academy of Sciences. His research and development activities include SiC-based power device design, gate-oxide growth and characterization, and relevant device fabrication.

Feng Zhang is currently a professor at the School of Physical Science and Technology, Xiamen University. His current interests include power devices such as wide bandgap semiconductor SiC MOSFETs, IGBT, and ultraviolet photodetectors and deep level defects and minority carrier lifetime in wide bandgap semiconductors.