NEWS AND VIEWS

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Super high maximum on-state currents in 2D transistors

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Two-dimensional (2D) materials have been recognized as a type of potential channel material to replace silicon in future field-effect transistors (FETs) by the International Technology Roadmap for Semiconductors (ITRS) and its succesor the International Roadmap for Devices and Systems (IRDS)[1–4]. Substantial first principle quantum transport simulations have predicted that many 2D transistors, including those with MoS_2, WSe_2, phosphorene, and Bi_2O_2Se channels, own excellent device performance and are able to extend Moore's law down to the sub-10 nm scale[4]. However, the actual 2D transistors suffer from poor contact and dielectric[4]. As a result, the maximum on-state currents (I_{on}^{max}) or saturation currents (I_{sat}) of the fabricated 2D transistors are even generally lower than the on-state current (I_{on}) (>1200 μA/μm) of the most advanced silicon transistors. As we know, the on-state current is one of the most critical figure of merit of a FET required by ITRS and IRDS, and a large on-state current implies a fast switching speed.

Due to lack of reliable and sustainable doping technique, 2D semiconductors often need to contact metal electrods directly. Schottky barrier is often generated at the metal–semiconductor interface, resulting a poor contact. Schottky barrier originates from the the Fermi level pinng (FLP), which is caused by metal-induced gap states (MIGS)[3]. Because the Fermi level of semimetal Bi aligns with the conduction of the monolayer (ML) MoS_2, the MIGS and thus FLP are greatly depressioned at the interface between Bi and ML MoS_2[5]. With semimetal Bi as electrodes, Ohmic contact with ultra-low contact resistance of 123 $\Omega\cdot\mu$m and an I_{on}^{max} up to 1135 μA/μm are obtained in a ML MoS_2 transistor by Kong *et al.* from MIT in 2021[5]. Compared with the ML MoS_2, bilayer (BL) MoS_2 has a narrower bandgap and higher electron density, which is beneficial for the on-state current enhancement. Recently, Wang's group from Najing University has fabricated the BL MoS_2 field-effect transistors with Bi as electrodes, and the mobility has improved by 37.9% and reached 122.6 $cm^2/(V\cdot s)$, and I_{on}^{max} is further increased to 1270 μA/μm[6]. The I_{on}^{max} values of these MoS_2 transistors are consistent with that (~1200 μA/μm) predicted based on the ab initio quantum transport simulation for the ML MoS_2 transistor by Lu *et al.* from Peking University[7].

Very recently, a record I_{on}^{max} of 1720 μA/μm among all the current 2D-material transistors (Fig. 1) accompanied by a small on-state resistance of 500 $\Omega\cdot\mu$m is achieved by Duan's group from Hunan Univeristy in the 20 nm-channel-length BL WSe_2 transistor with van der Waals (vdW) VSe_2 contact[8]. I_{on}^{max} is 1360 μA/μm under V_{ds} = 0.8 V, which is also close to a prediction (~ 1500 μA/μm) for the ML WSe_2 MOSFET at V_{ds} = 0.72 V based on the ab initio quantum transport simulation by Lu *et al.*[9]. Such a high performance can be ascribed to depression of the FLP in weak vdW contact[3].

Although such I_{on}^{max} values in the 2D MoS_2 and WSe_2 transistors are comparable with or even exceeds I_{on} in the Si transistors, it does not imply that the 2D transistors have outperformed the Si transistors as the carbon nanotube transistors do, reported by Peng *et al.*[10]. The reason lies in the fact that the high I_{on}^{max} values of the best 2D WSe_2 and MoS_2 transistors are generated in a rather high gate swing (20–60 V)[6, 8]. However, the Si FETs required in ITRS or IRDS operate under a small supply voltage V_{dd} (about 0.7 V)[11, 12], and I_{on} is measured under a gate swing no more than this V_{dd}. To be specific, I_{on} is obtained under a bias V_{ds} and gate swing of V_g(on) – V_g(off) defined by V_{dd} (Namely, $V_{ds} = V_g(on) - V_g(off) = V_{dd}$). Given the same criterion, not only I_{on} but also the closely related maximum transconductance g_m of the best 2D WSe_2 and MoS_2 transistors remain much smaller than those of the Si transistors under the similar V_{dd} [0.15–5 (MoS_2 and WSe_2) vs 1000 μA/μm (Si) in I_{on} and 0.13–20 (MoS_2 and WSe_2) vs 3000 μS/μm (Si) in g_m][6, 8, 13].

The improvement method is to use the high-κ dielectric with ultrathin thickness and obtain an ultrasmall equivalent oxide thickness (EOT)[1]. Duan *et al.* have tried to reduce the EOT of the bilayer WSe_2 FETs by using the 3-nm Al_2O_3/6-nm HfO_2 dielectric layer. The corresponding gate swing is

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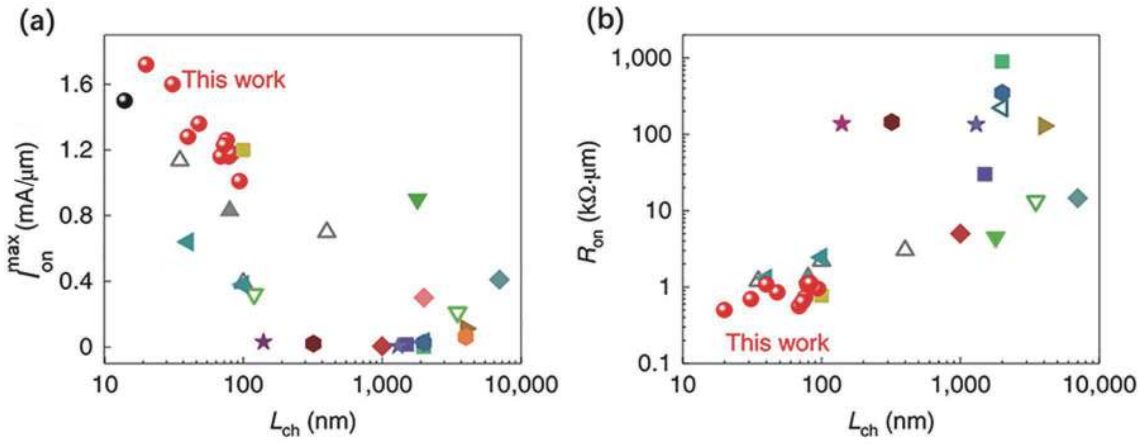

Fig. 1. (Color online) Benchmarking sub-100-nm bilayer WSe_2 transistors (red ball) against the (a) I_{on}^{max} for 2D semiconductor transistors (b-P, b-As, b-AsP, MoS_2, MoS_2-0.7 nm, WSe_2-0.7 nm, WS_2, WS_2-0.7 nm, $MoTe_2$, GeAs, InSe, SnSe, ReS_2, $PtSe_2$, $ZrSe_2$, $HfSe_2$) and I_{on} of 2021 silicon transistor (black ball) reported in ITRS, and (b) the R_{on}^{min} (lowest on-state resistance) with those reported in the literature[8]. Reproduced with permission from Springer Nature, copyright 2022.

significantly decreased from 40 to below 5 V, I_{on}^{max} remains over 1 mA/μm[8], and g_m is significantly improved from 0.13 to 150 μS/μm. Very recently, Peng *et al.* from Peking University have successfully fabricated the sub-0.5-nm EOT (2.3-nm β-Bi_2SeO_5) in the 2D Bi_2O_2Se FETs, realizing ultralow leakage current[14]. This achievement overcomes the challenges in depositing the ultra-thin gate dielectric on the dangling-bond-free 2D semiconductors, making it promising for the development of 2D transistors with high I_{on} and g_m.

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