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# A deep trench super-junction LDMOS with double charge compensation layer

**Lijuan Wu†, Shaolian Su, Xing Chen, Jinsheng Zeng, and Haifeng Wu**

Hunan Provincial Key Laboratory of Flexible Electronic Materials Genome Engineering, School of Physics & Electronic Science, Changsha University of Science & Technology, Changsha 410114, China

**Abstract:** A deep trench super-junction LDMOS with double charge compensation layer (DC DT SJ LDMOS) is proposed in this paper. Due to the capacitance effect of the deep trench which is known as silicon–insulator–silicon (SIS) capacitance, the charge balance in the super-junction region of the conventional deep trench SJ LDMOS (Con. DT SJ LDMOS) device will be broken, resulting in breakdown voltage (BV) of the device drops. DC DT SJ LDMOS solves the SIS capacitance effect by adding a vertical variable doped charge compensation layer and a triangular charge compensation layer inside the Con. DT SJ LDMOS device. Therefore, the drift region reaches an ideal charge balance state again. The electric field is optimized by double charge compensation and gate field plate so that the breakdown voltage of the proposed device is improved sharply, meanwhile the enlarged on-current region reduces its specific on-resistance. The simulation results show that compared with the Con. DT SJ LDMOS, the BV of the DC DT SJ LDMOS has been increased from 549.5 to 705.5 V, and the $R_{on,sp}$ decreased to 23.7 mΩ·cm$^2$.

**Key words:** double charge compensation layer; super-junction; deep trench; SIS capacitance

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## 1. Introduction

Super-junction (SJ) technology has become a milestone in the history of power devices because it has broken the "silicon limit"[1, 2]. However, because the traditional LDMOS relies on a large cell pitch to sustain surface voltage, the benefit brought by SJ is limited. This problem is solved by the deep-trench (DT) technique, in which a DT filled with dielectric is utilized to sustain most of the surface voltage[3–8]. However, in the Con. DT SJ LDMOS, due to the existence of the SIS capacitance, the charge balance in the SJ region is broken, which causes damage of the performance of the device[9–12].

This paper develops a solution by adding vertical variable doping layer at the source end of the $SiO_2$ trench and an inverted triangular charge compensation layer at the drain end to compensate the unbalanced charge in the SJ region caused by the SIS capacitance effect on both sides of the $SiO_2$ dielectric trench, and optimize the surface electric field of the device. The SJ region on the source side of the DC DT SJ LDMOS is a P–N–P type super junction structure. The introduction of this P–N–P SJ structure adds a new voltage-resistant junction compared to the Con. P–N SJ structure to modulate the internal electric field and produces a new electric field peak which raises the internal electric field of the device.

## 2. Structure and mechanism

The structure of the DC DT SJ LDMOS is shown as Fig. 1(a). $t_{sj}$, $t_{drift}$, and $t_{sub}$ represent the thickness of the SJ, the thickness of the bottom drift region and the thickness of the substrate respectively, $W_{sj}$ represents the width of the super junction on both sides of the $SiO_2$ dielectric trench, and the width of the compensation layer is equal to the width of the SJ region. $W_{trench}$ is the width of the $SiO_2$ dielectric trench. $N_{drift}$ and $N_{sub}$ are the doping concentration of the drift region at the bottom of the $SiO_2$ dielectric trench and the doping concentration of the substrate, respectively. The doping concentration of the P–N–P type SJ region under the source is the same, $N_{A1} = N_{D1} = N_{sj}$. The doping concentration of the triangle-like SJ region under the drain level is the same, $N_{A2} = N_{D2} = N_{sj2}$. The concentration of the triangular charge compensation layer on the left side of the $SiO_2$ dielectric trench is $N_{TB}$. The charge compensation layer on the right side of the $SiO_2$ dielectric trench is vertical variable-doped, and the doping concentration gradually decreases from the top to the bottom, which is represented by $N_{VB}$.

As can seen from the Fig. 1(a), the DC DT SJ LDMOS device structure has a triangular charge compensation layer on the left side of the $SiO_2$ dielectric trench. The addition of the triangular charge compensation layer makes the conventional P-pillar and N-pillar SJ structure with equal width and equal concentration become a triangular-like SJ structure. The inverted triangle form of the charge compensation layer fully compensates the charge accumulated by the SIS parallel plate capacitance generated on both sides of the $SiO_2$ dielectric trench. The right-hand side of the $SiO_2$ dielectric trench adopts the P-type charge compensation layer in the form of vertical variable doping. The P-type gradient compensation layer can also fully compensate the charge generated by the SIS capacitor, and the SJ region returns to the charge balance state. The SJ region at the source side of the $SiO_2$ dielectric trench is a P–N–P type SJ structure. The addition of a new voltage-resistant junction improves the BV of the

Correspondence to: L J Wu, 305719669@qq.com
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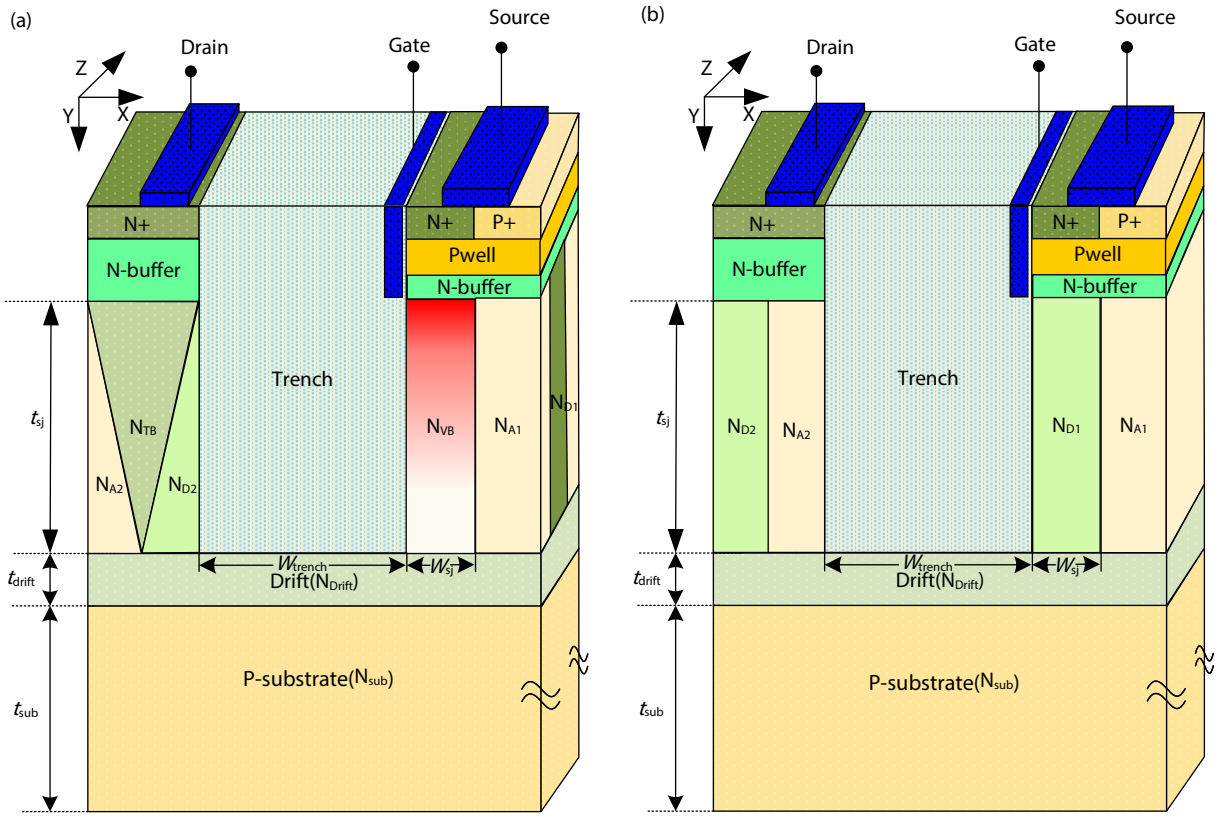


Fig. 1. (Color online) The structure of (a) DC DT SJ LDMOS and (b) Con. DT SJ LDMOS.

Table 1. Key parameters used in simulation.

| Parameter | Symbol | DC DT SJ LDMOS | Con. DT SJ LDMOS | Unit |
|---|---|---|---|---|
| Width of $SiO_2$ trench | $W_{trench}$ | 10 | 10 | $\mu$m |
| Width of PN pillar | $W_{sj}$ | 2 | 2 | $\mu$m |
| Thickness of PN pillar | $t_{sj}$ | 17 | 17 | $\mu$m |
| Thickness of drift region | $t_{drift}$ | 2 | 2 | $\mu$m |
| Thickness of substrate | $t_{sub}$ | 38 | 38 | $\mu$m |
| Doping concentration of N/P pillar at source | $N_{D1}/N_{A1}(N_{sj})$ | Optimized | Optimized | $cm^{-3}$ |
| Doping concentration of triangular-like SJ N/P pillar at drain | $N_{D2}/N_{A2}(N_{sj2})$ | Optimized | Optimized | $cm^{-3}$ |
| Doping concentration of inverted triangular charge compensation layer | $N_{TB}$ | Optimized | – | $cm^{-3}$ |
| Vertical variable doping concentration | $N_{VB}$ | Optimized | – | $cm^{-3}$ |
| Doping concentration of N drift region | $N_{drift}$ | Optimized | Optimized | $cm^{-3}$ |

device in both horizontal and vertical directions. The structure of the Con. DT SJ LDMOS is shown in Fig. 1(b).

The main parameters of the device structure of DC DT SJ LDMOS are shown in Table 1.

Fig. 2 shows the charge compensation principle of the DC DT SJ LDMOS. The vertical variable-doped P pillar at the source side and the inverted triangular N pillar at the drain side are used to compensate for the vertically distributed charges accumulated on both sides of the trench $SiO_2$ capacitor. The triangular-like SJ structure at the source side and the PNP structure at the drain side can deplete each other and maintain charge balance, so that the device reaches the charge balance.

Compared with the structure of the Con. DT SJ LDMOS device, the problem of charge imbalance due to SIS capacitance can be solved. The P–N–P type SJ structure at the source can modulate the internal electric field of the device.

The BV of DC DT SJ LDMOS has increased by 28.9% to 705.5 V. In the on-state, the current path is widen at the drain, and the doping concentration of triangular-like SJ region at the drain and P–N–P structure source is higher than that of the Con. DT SJ LDMOS so the $R_{on,sp}$ can be reduced sig-

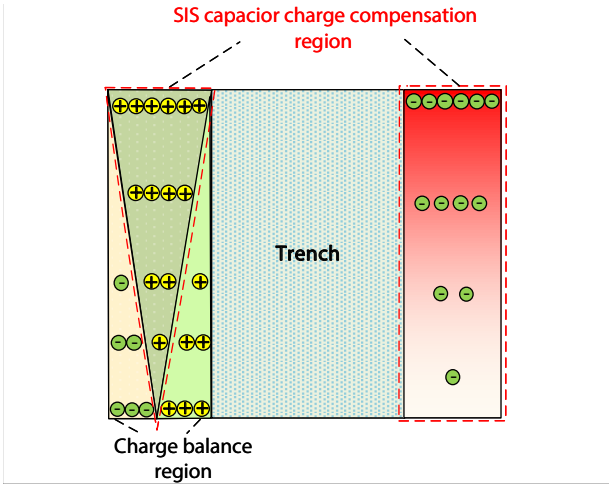


Fig. 2. (Color online) Structure and composition of the DC DT SJ LDMOS.

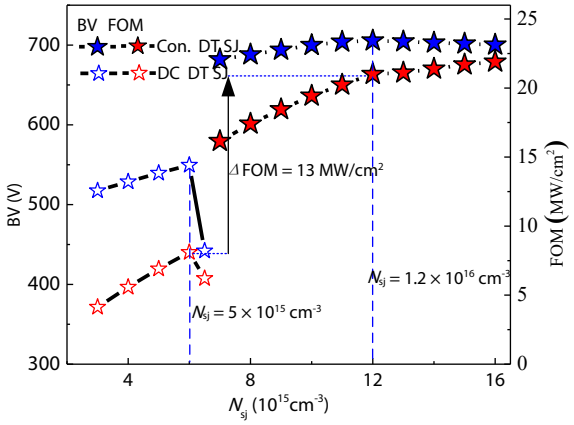


Fig. 3. (Color online) The influence of $N_{sj}$ at source on BV of Con. DT SJ LDMOS and DC DT SJ LDMOS.

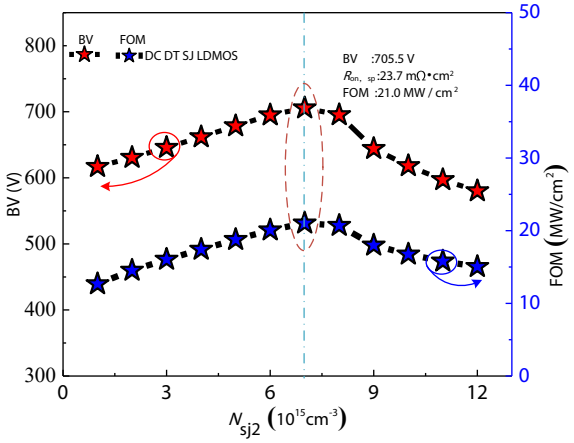


Fig. 4. (Color online) The influence of $N_{sj2}$ at the drain on BV of DC DT SJ LDMOS.

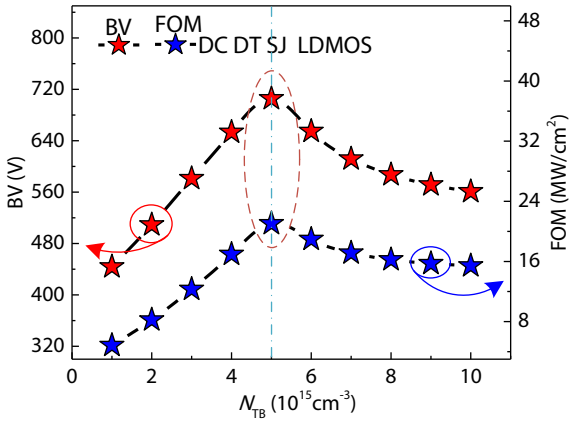


Fig. 5. (Color online) The influence of $N_{TB}$ at the drain on BV of DC DT SJ LDMOS.

nificantly.

The vertical variable-doped P-type charge compensation layer provides more uniform and sufficient charge compensation for the charge imbalance in the SJ region caused by the SIS capacitors on both sides of the $SiO_2$ dielectric trench. The change gradient of the vertical concentration of the P-type charge compensation layer is optimized by simulation.

The doping concentration of the P-type charge compensation layer on the right-hand side of the $SiO_2$ dielectric trench changes linearly. The position of the charge compensation layer is 3 to 20 $\mu$m in the $y$ direction, and the thickness is 17 $\mu$m. The doping concentration gradually decreased from $2 \times 10^{15}$ to $1 \times 10^{15}$ cm$^{-3}$. The concentration change gradient formula is:

$$N_{VB} = \frac{20 - y}{17} N_{VB,max} + N_{VB,min}. \quad (1)$$

## 3. Optimization of the parameters

This section discusses the effects of $N_{D1}$, $N_{A1}$, $N_{D2}$, $N_{A2}$, $N_{drift}$, $N_{TB}$ and $N_{VB}$ on the BV, $R_{on,sp}$ and FOM of the DC DT SJ LDMOS device. The above structure parameters were optimized by simulation.

Fig. 3 depicts the variation of the BV of the Con. DT SJ LDMOS and DC DT SJ LDMOS device with the $N_{sj}$ at the source. It can be seen from the figure that the optimal value of the BV of the Con. DT SJ LDMOS is just 549.5 when the $N_{sj}$ is $5 \times 10^{15}$ cm$^{-3}$ while the BV of the DC DT SJ LDMOS reaches a maximum of 705.5 V when the $N_{sj}$ is $1.2 \times 10^{16}$ cm$^{-3}$. For the DC DT SJ LDMOS, when the $N_{sj} \leqslant 1.2 \times 10^{16}$ cm$^{-3}$, the BV increases with the $N_{sj}$. This happens because the electron-hole pairs in the device were not fully depleted and the space charge region formed by the PN junction will form an electric field spike, leading to premature breakdown of the device. After the $N_{sj}$ exceeds the optimal value, the BV decreases with the increase of $N_{sj}$, because the excess electrons or holes cannot be completely depleted, the BV begins to drop again.

Fig. 4 shows the BV and FOM of the DC DT SJ LDMOS device with the change of the triangle-like SJ doping concentration $N_{sj2}$ at the drain side. The two curves of the device show a trend of first rising and then falling. When the concentration of $N_{sj2}$ is $7 \times 10^{15}$ cm$^{-3}$, the BV and FOM reach the maximum. The reason of this trend is similar to Fig. 3, which is related to the depletion of electron-hole pairs.

Fig. 5 shows the influence of $N_{TB}$ at the drain side on BV and FOM for the DC DT SJ LDMOS. The N-type region in the triangular SJ will not only deplete part of the charge through the SIS capacitance effect but also deplete with the P-type region. To achieve charge balance, a triangular charge compensation layer under the drain is added to compensate for holes that are not depleted in the P-type SJ region due to the SIS capacitance effect. The optimization of the doping concentration $N_{TB}$ in the triangular charge compensation layer can better solve the charge imbalance issue caused by the SIS capacitance effect. The compensation layer is an inverted triangle, which is uniformly doped, and the amount of compensation charge gradually decreases from the top to the bottom. Since the SJ region is in charge unbalanced state, which is affected by the SIS capacitance and will result in a decrease in BV.

It is very sensitive for BV that the changes in concentration of the charge compensation layer may cause a decay in its value.

It can be seen from Fig. 5 that when the triangular charge compensation layer $N_{TB} = 5 \times 10^{15}$ cm$^{-3}$, the BV and FOM reached the maximum. Both curves show a trend of increasing first and then decreasing, when the doping concentration increases from $1 \times 10^{15}$ to $5 \times 10^{15}$ cm$^{-3}$.

Fig. 6 shows how the change of vertical variable charge compensation layer doping concentration $N_{VB}$ influences BV and FOM. The doping concentration of the vertical variable

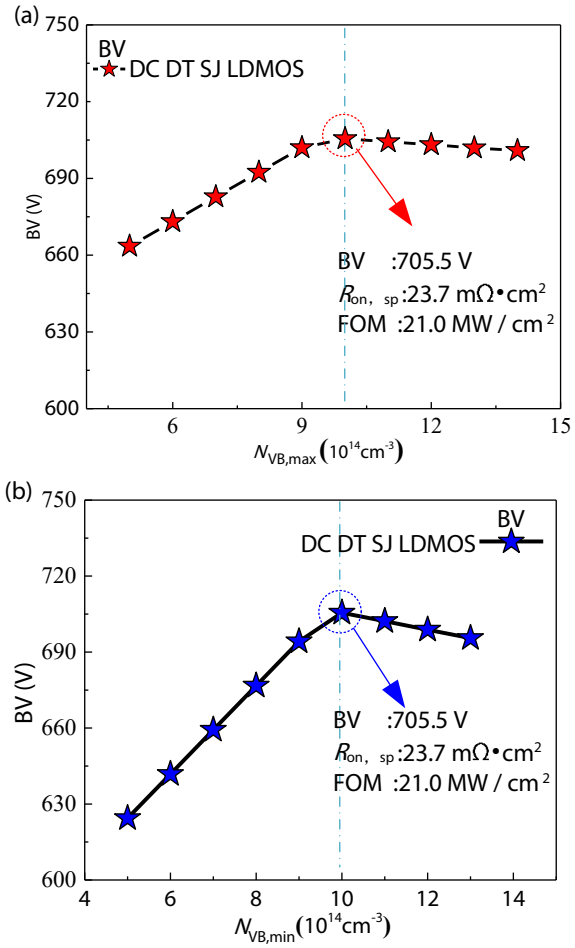


Fig. 6. (Color online) The influence of $N_{VB}$ on BV of DC DT SJ LDMOS. (a) Influence of $N_{VB,\ max}$ on BV of DC DT SJ LDMOS. (b) Influence of $N_{VB,min}$ on BV of DC DT SJ LDMOS.

doped charge compensation layer decreases with the increase of *Y*, and the doping concentration change is shown as Eq. (1). As shown in Fig. 6, when $N_{VB,min} = 1 \times 10^{15}$ cm$^{-3}$ and $N_{VB,max} = 1 \times 10^{15}$ cm$^{-3}$, the BV reaches the maximum. When the BV reaches the optimal value, the maximum concentration of the linear variable doping is $2 \times 10^{15}$ cm$^{-3}$. When the concentration of the vertical variable doping region is optimized to the optimum, the problem caused by the SIS capacitance effect in the SJ region is solved, and the SJ region returns to the charge balance state. The BV of DC DT SJ LDMOS device rises. The $R_{on,sp}$ is not affected by doping concentration. This happens because the current does not flow through the vertical variable doping P pillar. Consequently, when the BV achieves the optimal value, the FOM also achieves the optimal value.

Fig. 7 shows the influence of $N_{drift}$ on the BV and FOM of Con. DT SJ LDMOS and DC DT SJ LDMOS. From the figure it can be seen when the BV reaches the optimal value, the $N_{drift}$ are $5 \times 10^{15}$ and $7 \times 10^{15}$ cm$^{-3}$. The $N_{drift}$ of DC DT SJ LDMOS is higher than that of Con. DT SJ LDMOS. The N-type drift region at the bottom of the trench is mainly depleted with the P-type substrate to form a vertical P–N junction, which improves the device BV. It also serves as the necessary current path when the device is in the on state. $N_{drift}$ also has great influence on the $R_{on,sp}$. It can be seen from the figure that when the $N_{drift} = 7 \times 10^{15}$ cm$^{-3}$, the BV and FOM of the

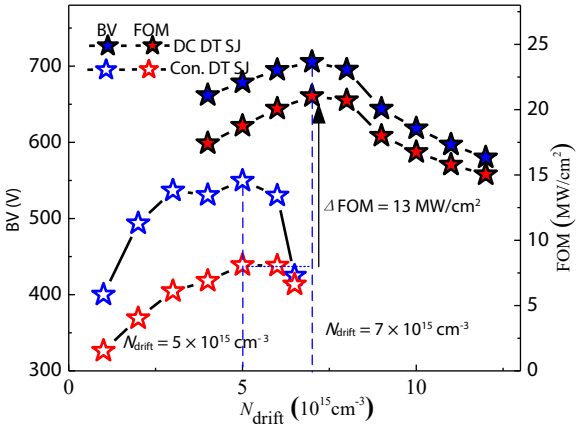


Fig. 7. (Color online) The influence of $N_{drift}$ on BV and FOM of Con. DT SJ LDMOS and DC DT SJ LDMOS.

DC DT SJ LDMOS reached the maximum. After the drift $N_{drift}$ reaches the optimal value, the P-type substrate is completely depleted, the BV of the DC DT SJ LDMOS device reaches the maximum value of 705.5 V.

In this part, the optimization process of key parameters that affects the performance of the device we proposed are shown as figures. In addition, the optimal value of each parameter is obtained. Compared with Con. DT SJ LDMOS, the charge imbalance problem of the Con. DT SJ LDMOS is solved by the double charge compensation layer. The electric field is modulated, and a higher BV is obtained. Compared with the Con. DT SJ LDMOS, the concentration of the drift region and SJ region of the new structure has been improved, and the conduction path is widened, which reduces the $R_{on,sp}$ and achieves a much higher FOM.

## 4. Results of the simulation

The DC DT SJ LDMOS structure device with a double charge compensation layer is proposed for the problem of trench type SJ SIS capacitor in this paper. This section conducts a targeted study on the BV when the DC DT SJ LDMOS is in the off state and the $R_{on,sp}$ in the on state, and compares the results of simulation to verify the principle of the device structure.

Fig. 8 shows the distribution of equipotential lines when the DC DT SJ LDMOS and Con. DT SJ LDMOS device are in the off state. Compared with the Con DT SJ LDMOS, the equipotential distribution of the new structure is denser, especially at the drain.

Fig. 9 shows the surface electric field ($Y = 0.01$ $\mu$m) and the electric field ($Y = 10$ $\mu$m) of the body of the DC DT SJ LDMOS device and Con. DT SJ LDMOS device in the off state. From this figure, it can be seen that the surface electric and both the surface electric field and the bulk electric field of the proposed structure are higher than those of the Con. DT SJ LDMOS. The BV of the proposed structure is also higher than that of the Con. DT SJ LDMOS.

Fig. 10 shows the breakdown characteristic curve of DC DT SJ LDMOS and Con. DT SJ LDMOS in the off state and the output characteristic curve in the on state. It can be seen from the figure that the BV of DC DT SJ LDMOS is 705.5 V, which is higer than 549.5 V of Con. DT SJ LDMOS. The illustration in the Fig. 10 shows the output characteristic curves corresponding to the gate voltage 15 V of DC DT SJ LDMOS and

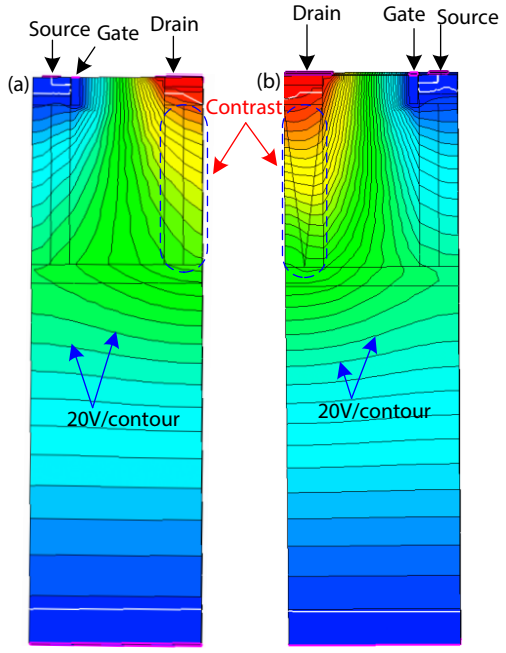


Fig. 8. (Color online) The distribution of equipotential lines in the off state of (a) Con. DT SJ LDMOS, (b) DC DT SJ LDMOS.

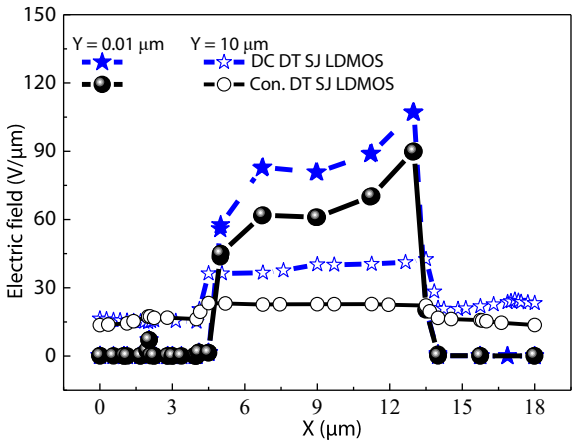


Fig. 9. (Color online) The surface electric field ($Y$ = 0.01 $\mu$m) and the electric field ($Y$ = 10 $\mu$m) of the SJ region of the DC DT SJ LDMOS device and Con. DT SJ LDMOS device in the off state.

the Con. DT SJ LDMOS respectively. It can be seen from this figure that both the on-state and off-state characteristics of the proposed structure are better than those of the Con. DT SJ LDMOS.

Fig. 11 shows the relationships between BV and $R_{on,sp}$ for Con. DT SJ LDMOS, some other reported structures[12–18] and DC DT SJ LDMOS proposed in this paper. From the figure it can be seen that the electrical performance of the device breaks through the "silicon limit"[11].

## 5. Conclusion

The SIS capacitor of deep trench SJ devices leads to charge imbalance in the SJ region. The DC DT SJ LDMOS is proposed in this paper to solve this problem, which adds a vertical variable doping compensation layer on the source side and an inverted triangular charge compensation layer on the drain based on the Con. DT SJ LDMOS. Moreover, the P–N–P dual voltage-resistant junction technology is used to improve the BV of the device. The double charge compensation layer solves the problem of the charge imbalance of the SJ region caused by the SIS capacitance. The P–N–P dual voltage-resistant junction technology adjusts the internal electric field, so that the BV of the device is improved. In addition, the current path is widen by the triangular-like SJ at the drain.

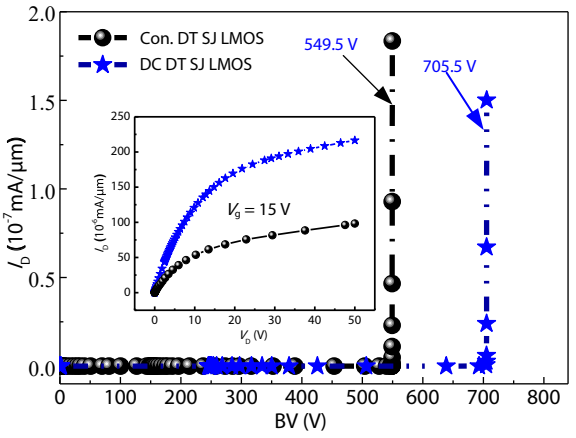


Fig. 10. (Color online) Measured off-state breakdown curve and on-state $I_d$–$V_d$ curves with $V_g$ = 15 V in the illustration of the TCCL DT SJ LDMOS and Con. DT SJ LDMOS.

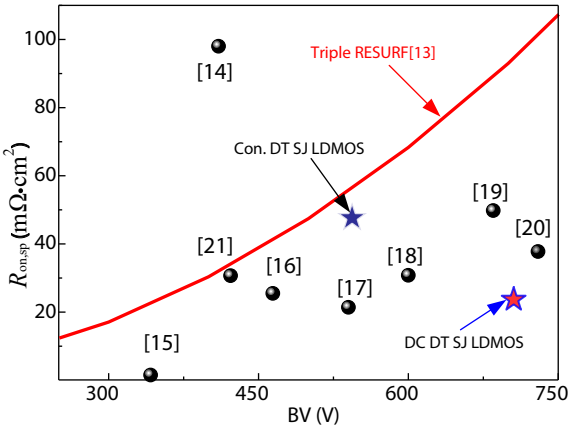


Fig. 11. (Color online) The $R_{on,sp}$ versus BV for different SJ LDMOSTs.

The simulation results show that compared with the Con. DT SJ LDMOS, the BV increases by 28.9% to 705.5 V, and the $R_{on,sp}$ of the device is reduced by 50.2% to 23.7 mΩ·cm$^2$ , and the FOM reached 21.0 MW/cm $^2$.

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**Lijuan Wu** received her B.S. from Sichuan University (SCU) in 2005 and Ph. D. Degree from the University of Electronic Science and Technology of China (UESTC) in 2012, respectively. Her graduate research work was focused on the high voltage drive structure and model. She is currently working on novel power device, process, and layout.