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ARTICLES

Multilayer doped-GeSe OTS selector for improved endurance and threshold voltage stability

Shiqing Zhang[1, ‡], Bing Song[1, ‡], Shujing Jia[2], Rongrong Cao[1], Sen Liu[1], Hui Xu[1], and Qingjiang Li[1, †]

[1]College of Electronic Science and Technology, National University of Defense Technology, Changsha 410073, China
[2]Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, Shanghai 200050 , China

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Abstract: Selector devices are indispensable components of large-scale memristor array systems. The thereinto, ovonic threshold switching (OTS) selector is one of the most suitable candidates for selector devices, owing to its high selectivity and scalability. However, OTS selectors suffer from poor endurance and stability which are persistent tricky problems for application. Here, we report on a multilayer OTS selector based on simple GeSe and doped-GeSe. The experimental results show improving selector performed extraordinary endurance up to 10^{10} and the fluctuation of threshold voltage is 2.5%. The reason for the improvement may lie in more interface states which strengthen the interaction among individual layers. These developments pave the way towards tuning a new class of OTS materials engineering, ensuring improvement of electrical performance.

Key words: ovonic threshold switch; selector; GeSe; multilayer structure; endurance; stability

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1. Introduction

Memristor study is rapidly developing and can be applied in multiple applications of storage or computing, while the array is suffering from errors caused by a sneak current flowing through the unselected cell blocks[1]. Therefore, access devices such as transistor, diode or selector are becoming indispensable for large passive crossbar arrays to ensure high resistance when the device is at low voltages[2]. In the selector domain, ovonic threshold switching (OTS) selectors, based on chalcogenide materials, exhibit high selectivity and fast response time, which makes it one of the most promising candidate selectors[3–7].

As for the ovonic threshold devices, the threshold switching phenomenon was demonstrated in 1968 for the first time[8]. A large number of reports have since been reported. A part of researchers focused on doping different chemical elements into material system in order to optimize the characteristics[9–12]. This will bring about an increased material complexity, even with more than five elements in the same alloy[13–15]. Furthermore, a common doping with arsenic element is able to improve the endurance significantly[16, 17]. However, arsenic is a highly toxic element which has negative impact on environmental protection and industrialization. Therefore, other scholars have turned their attention to two-terminal OTS materials, such as GeTe, ZnTe, SiTe[18] and GeSe[9, 10], which are more and more attractive due to their simple composition and competitive performance. Nevertheless, poor endurance and stability troubled these material systems, which is unable to match memristor operation. Hence, it is worthy to enhance device performance by changing the structure. It is expected that the heterostructures of different chalcogenide can be tried to improve the performance of OTS devices, referring to the phase change heterojunction of phase change devices[19–21]. Furthermore, some reported multilayer OTS selectors were recently put forward with too much layers, which make it difficult to manufacture[21, 22]. Therefore, a novel structure with simple multilayer is a new idea of device optimization and is quite necessary to be proposed.

In this article, we investigated a novel multilayer OTS selector with GeSe/doped-GeSe stacked structure. The experimental results demonstrated that the device had improved characteristics such as endurance and stability.

2. Experiments and methods

The multilayer devices were prepared with the cell size from 2 × 2 to 50 × 50 μm^2 on a p-type Si wafer with 200 nm-thick thermal oxide layers. TiN electrodes and GeSe material were deposited using the DC/RF sputtering method respectively. Doped GeSe were RF co-sputtered using the Ge_2Se_3 and Sb_2Te targets at room temperature (25 °C).

A cross-sectional TEM image of the multilayer stacked structure of GeSe/GeSeSbTe (GS/GSST sample) is given in Fig. 1(a). The stack consisted of five interlaced layers, including three layers of 7.9-nm-thick GeSe and two layers of 6-nm-thick GeSeSbTe. Total thickness was 35.7 nm and the composition was $Ge_xSe_y/Ge_xSe_ySb_zTe$, as determined via conventional TEM-energy dispersive X-ray spectroscopy (EDS) analysis shown in Figs. 1(b) and 1(c).

To compare the performance of the device, two types of other devices were prepared, namely a GeSe (GS sample) and a GeSe/GeSeSb (GS/GSS sample). The electrical characteristics of the devices with 10 × 10 μm^2 area were measured us-

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Shiqing Zhang and Bing Song contributed equally to this work.

Correspondence to: Q J Li, qingjiangli@nudt.edu.cn

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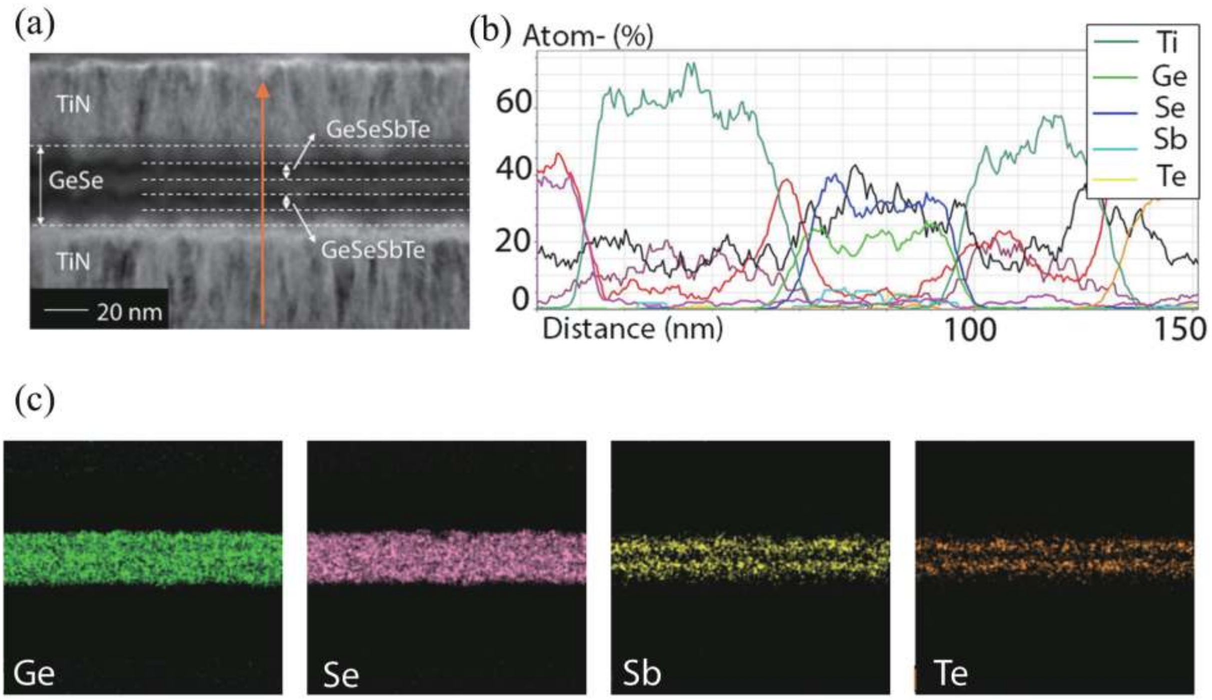

Fig. 1. (Color online) (a) TEM image of the multilayer selector device. (b) EDS line scanning spectrum along the direction marked by the line in (a). (c) EDS mapping of multilayer selector device.

ing a standard semiconductor parameter analyzer (Keithley 4200 SCS).

3. Results and discussion

The electrical characterization was mainly tested by quasi-static analysis, dynamic AC response and endurance analysis. The characteristics were tested under pulsed mode including triangular and trapezoidal voltage pulses. For chalcogenide glass, the electrical characteristics of the sample are mainly characterized by pulse testing to avoid enormous thermal and electrical stresses resulting from time lag in the DC voltage test[5, 23].

Fig. 2 presents cycle curves of triangle pulse test under the same triangular pulse with rising/falling edge of 500 ns/ 1 μs and a plateau length of 50 ns. As illustrated, all three samples show obvious threshold switching behavior. Figs. 2(a)–2(c) are the test results of monolayer GS sample, multilayer GSS sample and multilayer GSST sample, respectively. In Fig. 2(a), the ON current of GS sample degrades greatly and the OTS characteristic becomes inconspicuous with the increasing number of cycles. This is probably due to the unstable chemical bonds within GeSe material without doping other elements. The threshold voltage (V_{th}) of GSS sample is gradually degenerated and the OTS characteristic becomes inconspicuous, which is the same as the GS sample shown in Fig. 2(b). Owing to the increase of layers, a higher V_{th} with rapid decline exists. In Fig. 2(c), we report stable OTS characteristic of GS/GSST sample retaining with merely performance degradation after at least 20 cycles. By way of improving the structure and composition of the device, GS/GSST sample exhibits low V_{th} at 3.3 V and large selectivity at 10^4. The cumulative probability of V_{th} and V_h (holding voltage) is shown in Fig. 2(d). As demonstrated, the V_{th} coefficient of variation (C_v) of GSST sample is 2.5% calculated by $C_v = \sigma/\mu$, which means stable V_{th} and V_h. According to our analysis, Sb and Te doping contribute to the final result. Sb and Te are adopted to counteract the V_{th} rise and contribute to larger selectivity at the same time[11, 24]. Te concentration reduces the band gap and concentrates defects[24], while Sb is able to bring about lower threshold voltage[11]. The multilayer structure also leads to stronger interaction among individual layers[19], which helps to improve device stability. The increasing of layers acting as effective diffusion barriers against electron transport during extensive cycling.

Fig. 3 demonstrates the results of multiple trapezoidal pulse test with the rising and falling edge of trapezoidal pulse of 100 ns/100 ns and a plateau length of 200 ns. Figs. 3(a)–3(c) are the test results of monolayer GS sample, multilayer GSS sample and multilayer GSST sample, respectively. In Fig. 3(a), the GS sample loses OTS characteristic after several cycles of trapezoidal pulse. The GSS sample is able to present performance repeatability after at least 20 cycles, illustrated in Fig. 3(b). However, it is noted that the continuous curves demonstrate the randomness of delay time, indicating poor stability. We cycle GS/GSST sample for over 50 cycles as observed in Fig. 3(c). The curves of cycles pulse test are nearly superposed and the cumulative probability of delay time is presented in Fig. 3(d), which exhibits the lowest delay time and variance compared with GS sample and GS/GSS sample, indicating high stability and merely performance degradation.

The endurances of GS and GS/GSS sample are shown in Figs. 4(a) and 4(b), respectively. GS sample performs poor endurance with a degradation of high resistance after 10^4 pulses. Meanwhile, it is found that GS/GSS device presents an improvement of device endurance, after which it still presents a degradation of high resistance, indicating that multilayer structure has benefit effects on endurance improvement. However, it is still not up to expectations. In this case, Fig. 4(c) presents the endurance testing result of GS/GSST sample that is acquired using 7 V/200 ns programming pulses and

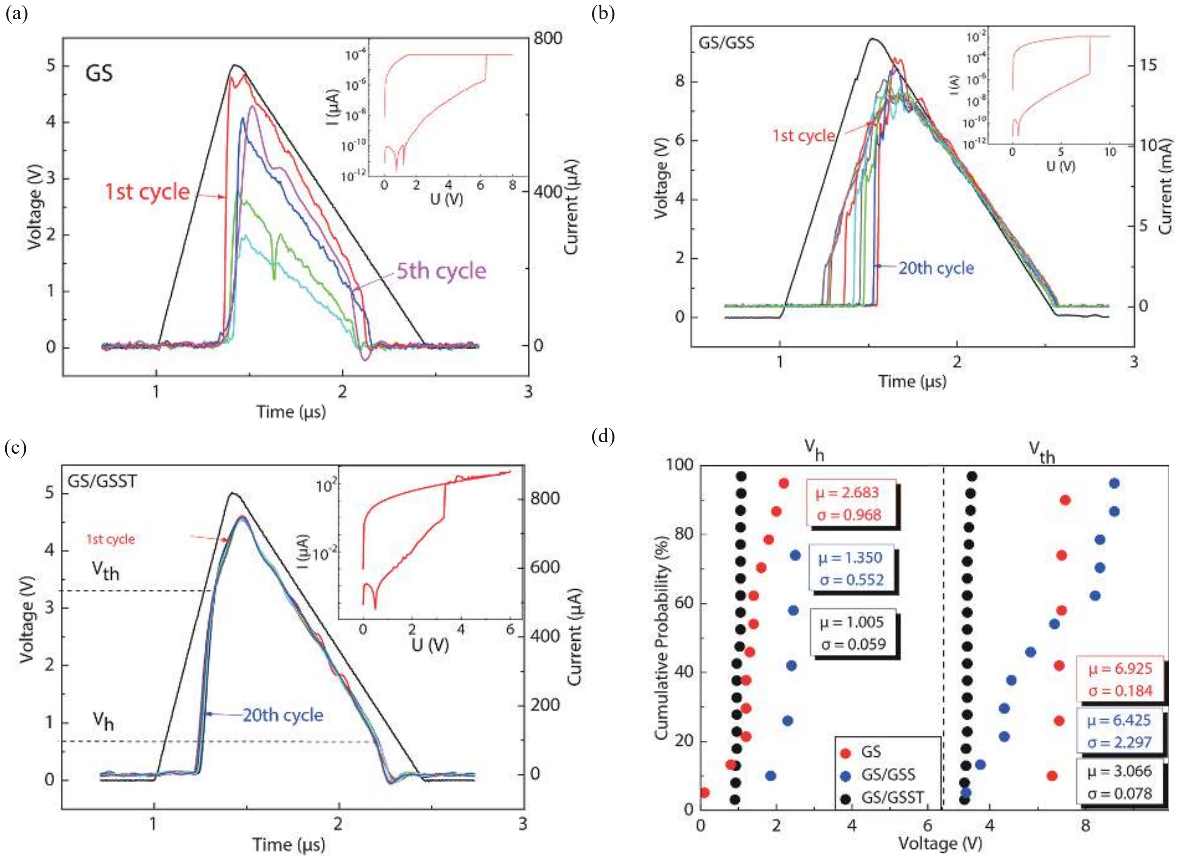

Fig. 2. (Color online) Cycle curves of triangle pulse test. (a) Monolayer GS sample. (b) Multilayer GSS sample. (c) Multilayer GSST sample. (d) Cumulative probability of V_{th} and V_h. The insets are the DC tests of each type of selector.

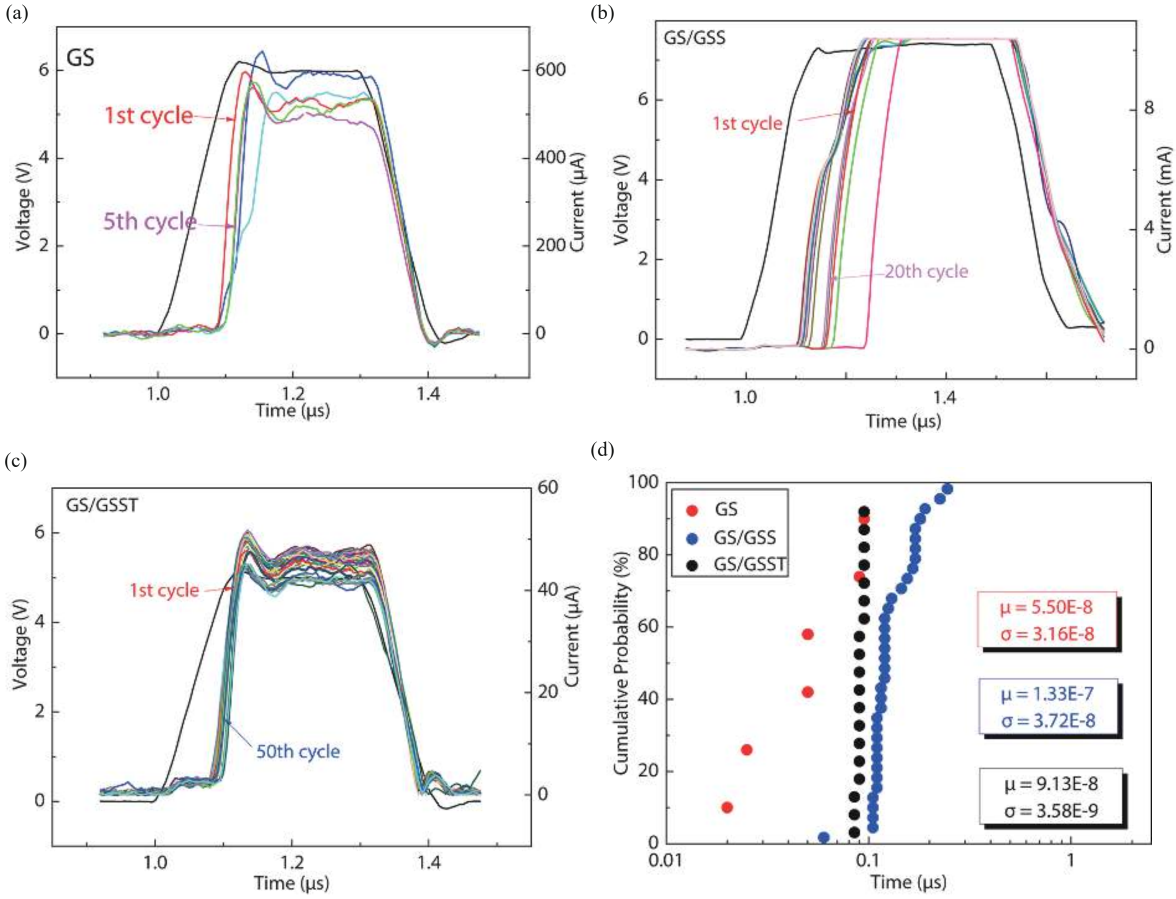

Fig. 3. (Color online) Cycle curves of trapezoidal pulses test. (a) Monolayer GS sample. (b) Multilayer GSS sample. (c) Multilayer GSST sample. (d) Cumulative probability of delay time.

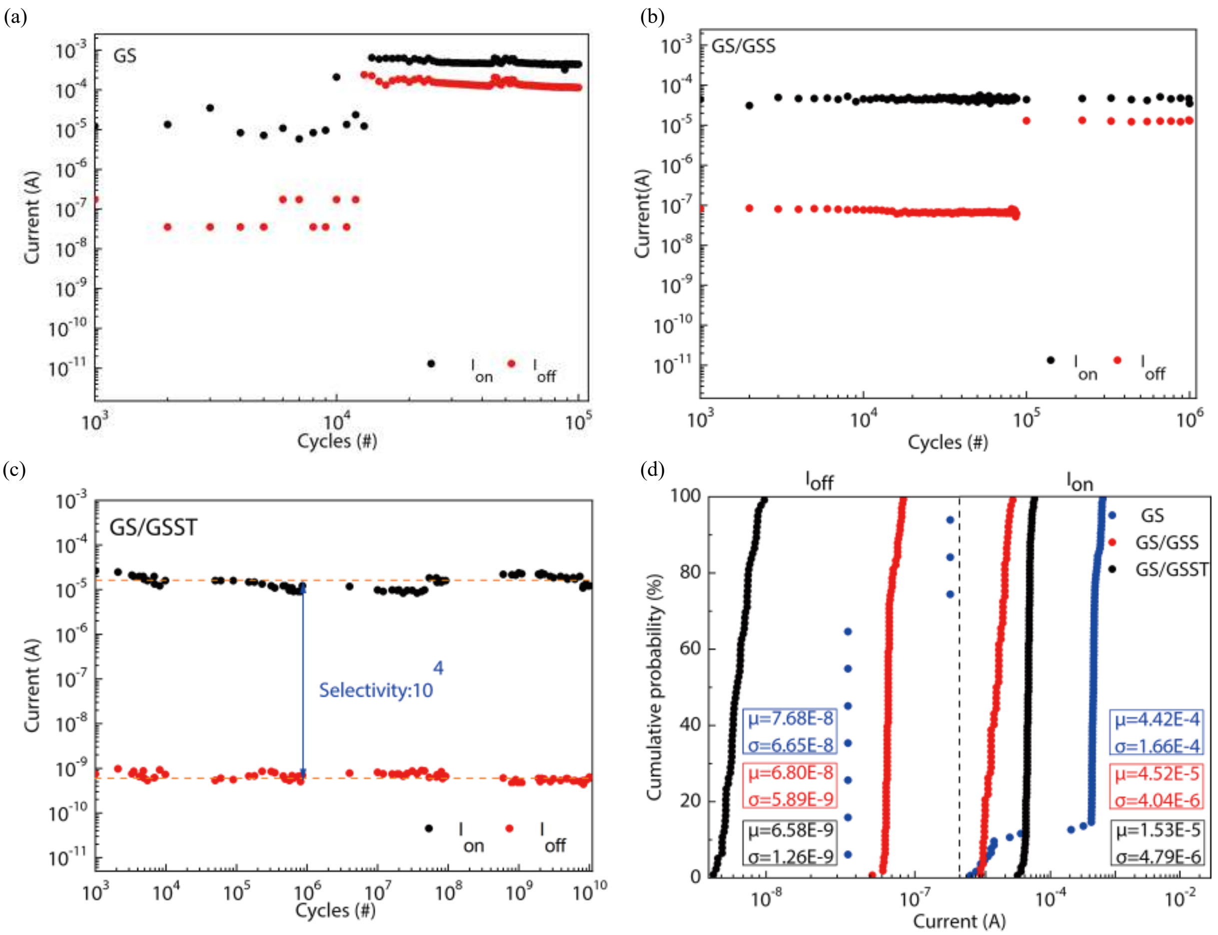

Fig. 4. (Color online) Results of endurance test. (a) Monolayer GS sample. (b) Multilayer GSS sample. (c) Multilayer GSST sample. (d) Cumulative probability of ON and OFF resistance.

Table 1. Comparison with other published selectors.

Material	Structure	Thinkness (nm)	I_{off} (A)	C_v (V_{th})	I_{on}/I_{off}	Endurance
SeSbN/GeSeSbN [21]	Multilayer	20	10^{-9}	–	10^6	2×10^9
AsTeGeSiN [27]	Monolayer	30	10^{-7}	–	10^3	10^8
SiTe [28]	Monolayer	13	10^{-8}	–	10^4	5×10^5
GeSe (this work)	Monolayer	30	10^{-8}	2.7%	10^3	10^4
GeSe/GeSeSb (this work)	Multilayer	30	10^{-7}	35.7%	10^3	10^5
GeSe/GeSeSbTe (this work)	Multilayer	35.7	10^{-9}	2.5%	10^4	$>10^{10}$

3.5 V/100 μs reading pulses with rising/falling edge is 100 ns/100 ns. The endurance result of the sample does not show any degradation up to more than 10^{10} switching cycles as illustrated. It is worthy that the phenomenon, multilayer sample electronically switches between off and on states repeatedly, which also indicate the material's stability. However, owing to the dependence of pulse test accuracy on pulse width and range, high current can be measured within a shorter time while low current can only be tested accurately in much longer time. Therefore, although it is limited by the test conditions, we suppose that the sample has potential to achieve a higher endurance over than 10^{10}. In addition, Fig. 4(d) illustrates the cumulative probability of on-state and off-state current. Compared with GS sample and GS/GSS sample, it performs the most stable current, which confirmed reliable switching on and off.

As-deposited materials and multilayer structure probably contribute to the improved endurance and stability. The increase of the layers indicates more interfaces, which bring strong interaction among individual layers. Take Ge–Se bonds as an example. The presence of Ge–Se bonds even in multilayers contributes to the strong inter-layers interaction and the high probability of Ge–Se formation[25]. Ge-Se bonds are important to avoid the OTS mechanism degradation. Besides, the doping of Te and Sb plays the same role. Sb–Se bonds and Sb–Sb bonds make the same contributions[11]. The increased concentration of Te and Sb is reported to decrease band-gap and concentrate traps[21, 26]. Therefore, GS/GSST sample performs a superior endurance and stability.

The characteristics of the devices proposed in this paper are compared with those of various reported bidirectional threshold switching devices as shown in Table 1. It can be seen that the multilayer structure can bring up improvement of endurance, but at the same time bring about a decline in stability. Therefore, by doping other elements to optimize the device, we can finally get a device with improved endurance and stability. As illustrated, the device we proposed demonstrates the endurance at over 10^{10} with simple multilayer structure, indicating greater potential for integration with memristors. The coefficient of variation (C_v) of V_{th} is 2.5 % and the C_v of delay time is 3.9 %, which indicate the improved stability. Furthermore, it can be seen that off-state current (I_{off}) and selectivity are able to achieve a pretty good level. Other multilayer device with the best reported performance is shown in Table 1[21]. In comparison, the multilayer device performs a better endurance and stability with a simpler structure. Further optimization can be achieved in selectivity and on state current. Therefore, it can be seen that the OTS selector can be optimized in the future for memristor integration and other applications.

4. Conclusion

Endurance and stability are crucial characteristics for OTS devices in a variety of applications. In this article, a reliability optimization method for OTS devices is investigated. We propose a symmetric multilayer OTS selector with improved endurance and stability. Compared with the characteristics of two other devices in the same material system, we provided a five interlaced multilayer structure based on GeSe/doped-GeSe stacked structure. It is observed that multilayer structure performs endurance more than 10^{10} cycles and 2.5% fluctuation of V_{th}. Therefore, an optimization of selector device is given by improving structure and doping. The device structure can provide a direction of device optimization based on improved structure of selector cells to manufacture high-performance selector and to be utilized to memristor integration with promising outlook.

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References

[1] Laudato M, Adinolfi V, Clarke R, et al. ALD GeAsSeTe ovonic threshold switch for 3D stackable crosspoint memory. 2020 IEEE Int Mem Work IMW, 2020, 1

[2] Kim T, Lee D, Kim J, et al. Firing voltage reduction in thermally annealed Ge-As-Te thin film with ovonic threshold switching. J Vac Sci Technol B, 2020, 38, 032213

[3] Czubatyj W, Hudgens S J. Thin-film Ovonic threshold switch: Its operation and application in modern integrated circuits. Electron Mater Lett, 2012, 8, 157

[4] Jeong D S, Lim H, Park G H, et al. Threshold resistive and capacitive switching behavior in binary amorphous GeSe. J Appl Phys, 2012, 111, 102807

[5] Ahn H W, Jeong D S, Cheong B K, et al. A study on the scalability of a selector device using threshold switching in Pt/GeSe/Pt. ECS Solid State Lett, 2013, 2, N31

[6] Kim S, Kim Y B, Kim K M, et al. Performance of threshold switching in chalcogenide glass for 3D stackable selector. 2013 Symp VLSI Technol, 2013, T240

[7] Zhu M, Ren K, Song Z T. Ovonic threshold switching selectors for three-dimensional stackable phase-change memory. MRS Bull, 2019, 44, 715

[8] Ovshinsky S R. Reversible electrical switching phenomena in disordered structures. Phys Rev Lett, 1968, 21, 1450

[9] Seo J, Ahn H W, Shin S Y, et al. Anomalous reduction of the switching voltage of Bi-doped $Ge_{0.5}Se_{0.5}$ ovonic threshold switching devices. Appl Phys Lett, 2014, 104, 153503

[10] Song B, Xu H, Liu S, et al. An ovonic threshold switching selector based on Se-rich GeSe chalcogenide. Appl Phys A, 2019, 125, 772

[11] Verdy A, Navarro G, Sousa V, et al. Improved electrical performance thanks to Sb and N doping in Se-rich GeSe-based OTS selector devices. 2017 IEEE Int Mem Work IMW, 2017, 1

[12] Noé P, Verdy A, d'Acapito F, et al. Toward ultimate nonvolatile resistive memories: The mechanism behind ovonic threshold switching revealed. Sci Adv, 2020, 6, eaay2830

[13] Cheng H Y, Chien W C, Kuo I T, et al. An ultra high endurance and thermally stable selector based on TeAsGeSiSe chalcogenides compatible with BEOL IC Integration for cross-point PCM. 2017 IEEE Int Electron Devices Meet IEDM, 2017, 2.2.1

[14] Kau D, Tang S, Karpov I V, et al. A stackable cross point Phase Change Memory. 2009 IEEE Int Electron Devices Meet IEDM, 2009, 1

[15] Lee M J, Lee D, Cho S H, et al. A plasma-treated chalcogenide switch device for stackable scalable 3D nanoscale memory. Nat Commun, 2013, 4, 2629

[16] Cheng H Y, Chien W C, Kuo I T, et al. Ultra-high endurance and low IOFF selector based on AsSeGe chalcogenides for wide memory window 3D stackable crosspoint memory. 2018 IEEE International Electron Devices Meeting, 2018, 37.3.1

[17] Navarro G, Verdy A, Castellani N, et al. Innovative PCM+OTS device with high sub-threshold non-linearity for non-switching reading operations and higher endurance performance. 2017 Symposium on VLSI Technology, 2017, T94

[18] Velea A, Opsomer K, Devulder W, et al. Te-based chalcogenide materials for selector applications. Sci Rep, 2017, 7, 8103

[19] Ding K Y, Wang J J, Zhou Y X, et al. Phase-change heterostructure enables ultralow noise and drift for memory operation. Science, 2019, 366, 210

[20] Adinolfi V, Laudato M, Clarke R, et al. ALD heterojunction ovonic threshold switches. ACS Appl Electron Mater, 2020, 2, 3818

[21] Laguna C, Castellani N, Bernard M, et al. Innovative multilayer OTS selectors for performance tuning and improved reliability. 2020 IEEE Int Mem Work IMW, 2020, 1

[22] Laguna C, Bernard M, Bernier N, et al. Multilayer OTS selectors engineering for high temperature stability, scalability and high endurance. 2021 IEEE Int Mem Work IMW, 2021, 1

[23] Govoreanu B, Donadio G L, Opsomer K, et al. Thermally stable integrated Se-based OTS selectors with >20 MA/cm^2 current drive, >3.103 half-bias nonlinearity, tunable threshold voltage and excellent endurance. 2017 Symp VLSI Technol, 2017, T92

[24] Koo Y, Baek K, Hwang H. Te-based amorphous binary OTS device with excellent selector characteristics for x-point memory applications. 2016 IEEE Symp VLSI Technol, 2016, 1

[25] Goyal D R, Maan A S. Far-infrared absorption in amorphous $Sb_{15}Ge_xSe_{85-x}$ glasses. J Non Cryst Solids, 1995, 183, 182

[26] Ho Lee J, Hwan Kim G, Bae Ahn Y, et al. Threshold switching in Si-As-Te thin film for the selector device of crossbar resistive memory. Appl Phys Lett, 2012, 100, 123505

[27] Lee M J, Lee D, Kim H, et al. Highly-scalable threshold switching select device based on chaclogenide glasses for 3D nanoscaled memory arrays. 2012 Int Electron Devices Meet, 2012, 2.6.1

[28] Koo Y, Lee S M, Park S, et al. Simple binary ovonic threshold switching material SiTe and its excellent selector performance for high-density memory array application. IEEE Electron Device Lett, 2017, 38, 568

Shiqing Zhang got her BS from Anhui University in 2019. Now she is a MS student at National University of Defense Technology under the supervision of Prof. Hui Xu. Her research focuses on ovonic threshold switching device and memristor.

Bing Song got his BS in 2011 at Beijing Institute of Technology and PhD degree in 2018 at National University of Defense Technology. He joined National University of Defense Technology as an associate professor in 2018. His research interests include intelligent device, circuit and system.

Qingjiang Li got his BS in 2008 and PhD degree in 2014 at National University of Defense Technology. He joined National University of Defense Technology as an associate professor in 2014. His research interests include intelligent device, circuit and system.