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Integration of high-performance spin-orbit torque MRAM devices by 200-mm-wafer manufacturing platform

Hongchao Zhang[1], Xiangyue Ma[1], Chuanpeng Jiang[1], Jialiang Yin[1], Shuqin Lyu[2], Shiyang Lu[2], Xiantao Shang[2], Bowen Man[2], Cong Zhang[2], Dandan Li[2], Shuhui Li[2], Wenjing Chen[3], Hongxi Liu[2, †], Gefei Wang[2, †], Kaihua Cao[1, 3, †], Zhaohao Wang[1], and Weisheng Zhao[1, 3]

[1]Fert Beijing Institute, School of Integrated Science and Engineering, Beihang University, Beijing 100191, China

[2]Truth Memory Tech. Corporation, Beijing 100088, China

[3]Beihang-Goertek Joint Microelectronics Institute, Qingdao Research Institute, Beihang University, Qingdao 266000, China

Abstract: We demonstrate in-plane field-free-switching spin-orbit torque (SOT) magnetic tunnel junction (MTJ) devices that are capable of low switching current density, fast speed, high reliability, and, most importantly, manufactured uniformly by the 200-mm-wafer platform. The performance of the devices is systematically studied, including their magnetic properties, switching behaviors, endurance and data retention. The successful integration of SOT devices within the 200-mm-wafer manufacturing platform provides a feasible way to industrialize SOT MRAMs. It is expected to obtain excellent performance of the devices by further optimizing the MTJ film stacks and the corresponding fabrication processes in the future.

Key words: SOT MTJ; low switching current densities; 200-mm-wafer platform; endurance; data retention

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1. Introduction

Magnetic random access memory (MRAM), as an emerging non-volatile memory, features high read and write speed, high endurance, long storage time and low-power dissipation, and has captured considerable interest in large semiconductor foundries, such as TSMC, Samsung and GlobalFoundries a few years ago[1–5]. On the one hand, MRAM's high performance characteristics help it to become an important solution to replace the embedded flash (e-flash) memory below 28 nm CMOS technology node, whereas e-flash has severe economic barriers that hampers its further scaling[6]. On the other hand, MRAM is aimed as an alternative to become working memories, such as static random-access memory (SRAM) to solve severe potential leakage in the advanced CMOS node[7, 8]. However, it is difficult to replace L1 or L2 cache SRAM due to the speed limitations and endurance problems, especially for two-terminal spin-transfer torque (STT) MRAMs[9–11]. Thus, the further exploration of next-generation MRAM devices is needed.

Based on the writing mode[12], MRAMs can be classified into three main categories: toggle MRAM, STT MRAM and spin-orbit torque (SOT) MRAM. Toggle MRAM is the first generation of commercial MRAM, which utilize the Oster field generated by the current to reverse the free layer magnetization[13]. However, difficulties such as, scaling-down and high-power consumption limit its development. Two-terminal STT MRAM devices use the current-induced spin-transfer torque to switch the free layer magnetization[14–17]. The high write current density stresses the tunnel barrier during the write operation, then degrades its reliability[18–21]. To solve the reliability issues of the STT MRAM, SOT MRAM is proposed because read and write paths are separated in three-terminal devices which intrinsically solves the read error issue and tunnel barrier aging issues due to high write current[22–26].

Nevertheless, SOT MRAM is still in the research and development phase because there are several challenges in the wafer-level manufacturing process. These challenges stem mainly from two aspects. First, the commercialized STT MRAM usually consists of bottom-pinned perpendicular magnetic tunnel junctions (p-MTJ) stack structure. For this kind of film stack, the free layer is on the top of the structure, which is not sensitive to the roughness of the substrate because of the thicker bottom seed layer and synthetic antiferromagnetism (SAF)/reference layer (RL). Unlike STT MRAM, SOT MRAM currently uses a top-pinned film structure. The heavy metal and free layer are adjacent to the substrate, and the substrate roughness plays a key role in the film quality of the upper film, thus affecting the electrical and magnetics performance of the MTJs. Therefore, it is challenging to integrate MTJ in commonly used back-end-of-line (BEOL) process because of the severe influence of the surface roughness on MTJ film performance[27]. Second, the SOT channel is ultra-thin to obtain as large as possible charge-to-spin conversion efficiency due to relatively small spin diffusion length. This ultra-thin SOT channel would give more challenges on how to etch stop exactly on the channels across the wafer. This issue needs to be solved for wafer level manufacturing[28]. In view

Correspondence to: H X Liu, hongxi_liu@tmc-bj.cn; G F Wang, gefei_wang@tmc-bj.cn; K H Cao, kaihua.cao@buaa.edu.cn
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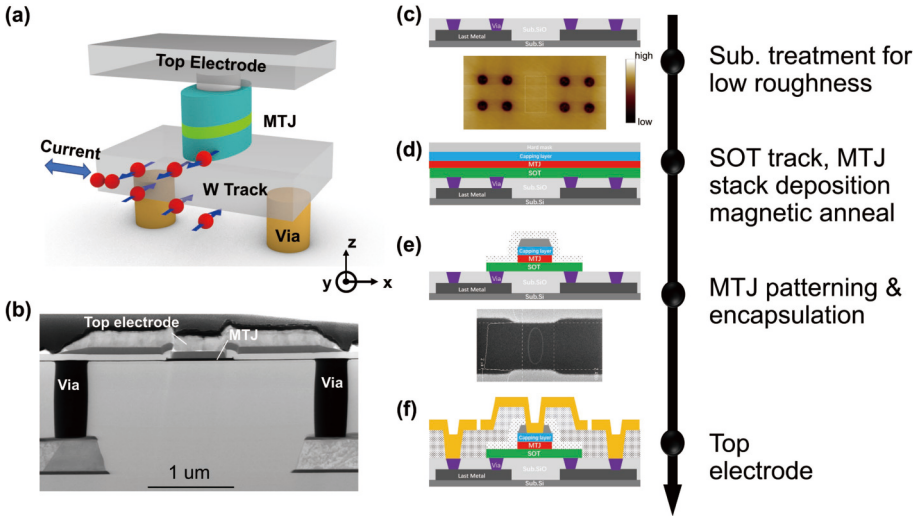

Fig. 1. (Color online) SOT device structure and the SOT-MTJs process flow. (a) Three-dimensional schematic pictures of SOT device. (b) Cross-section TEM images cutting along the SOT track (*x*-direction). (c) Substrate treatment for low roughness. (d) SOT track, MTJ film stack deposition and magnetic anneal. (e) MTJ patterning and encapsulation. (f) Top electrode process.

of these challenges, several research groups have focused their efforts on developing wafer-level SOT MRAM devices. For example, Singapore IME successfully prepared a 200-mm-wafer-level in-plane SOT MTJs using thick Pt as a heavy metal (HM) layer. The tunnel magnetoresistance ratios (TMR) of these devices are 80%–100%[29]. However, the prepared device was not integrated by the BEOL process. Moreover, the resistance of SOT track is too large, which cannot match with the CMOS integrations. In 2019, Tohoku University demonstrated the canted field-free SOT MRAM with excellent device performance on 300 mm wafer. They systematically tested various parameters of the devices and showed that the in-plane SOT MRAM has a favorable development prospect. However, the data they presented are based on the performance of single devices, there is no description about the wafer-level uniformity[26]. Taiwan's Industrial Research Institute also designed an 8 kb in-plane SOT MRAM chip based on 200 mm wafer for the first time. However, the most important endurance results are not clarified clearly and there are no data shown to support the uniformity performance at wafer level[30].

In view of these problems, the purpose of our present study is to demonstrate the manufacturing capability of wafer-level SOT MTJ devices. We integrated in-plane SOT MTJ devices by the 200-mm-wafer platform, using a two-metal-layers BEOL process. Film structural information, electrical properties, and reliability performance are systematically studied for the SOT devices that we have fabricated.

2. Results and discussion

SOT MTJs were integrated by the 200-mm-wafer manufacturing platform. Figs. 1(a) and 1(b) show the three-dimensional schematic pictures of the MTJ device and the corresponding cross-section transmission electron microscopy (TEM) image cutting along the SOT track (*x*-direction), respectively. The substrate, consisting of one metal layer and one via, was prepared by the foundry through the so called "short loop" process flow. The process and design rules of the metal line and the via are the same as that of "Metal5" and "Via5" widely used in the common 0.18 μm CMOS technology node. As can be seen in Figs. 1(a) and 1(b), the isolated SOT MTJs are designed using Kelvin structure located between the vias and on top of the dielectric materials. Following the arrow sequence, the SOT MTJs process cartoon flow is illustrated in Figs. 1(c)–1(f). The substrate was first treated under a chemical mechanical polishing process to obtain sufficiently low roughness (< 0.2 nm) required for MTJ stacks[26]. The bottom image of Fig. 1(c) is scanned by atomic force microscope (AFM) in the SOT MTJ area. The R_a value in the marked white box area is 0.155 nm, which is perfect for the following MTJ stack deposition. Second, the SOT track and the MTJ stack were deposited in a 200 mm capable PVD tool with thickness nonuniformity of 1.6% across the wafer confirmed through the 49 points resistivity measurements. The stacks featuring in-plane magnetic anisotropy are composed of (from the bottom to the top) W (5)/CoFeB (1.3)/MgO (1.5)/CoFeB (1.9)/CoFe (0.8)/Ru (0.8)/CoFe (2.5)/IrMn (7.5)/Ta (3)/Ru (2)/Ta (2). The numbers in parentheses signify every layer thickness in nanometers. Here, we use W as the SOT HM layer. As well known, W has a relatively large charge-to-spin conversion efficiency, i.e., spin Hall angle (SHA) ~ –0.3 for the β-W phase[31]. The first CoFeB next to W is the free layer (FL), the magnetization direction of which can be switched effectively due to the spin current generated by the spin-Hall effect (SHE) or/and Rashba effects at the interface of HM/FL once the current pass through the SOT HM layer. The CoFeB/CoFe/Ru/CoFe/IrMn multilayers are used as a synthetic antiferromagnetic (SAF) layer for pinning the second CoFeB reference layer, which can also effectively reduce the stray field. Top Ta/Ru/Ta layers are used as a protective cap and top electrode, which can simultaneously avoid oxidation. The MTJ resistance area products (RA) are 4863 $\Omega{\cdot}\mu m^2$ obtained by the CIPT method, with 7.2% nonuniformity across the wafer. The whole wafer was subsequently annealed at 300 °C under a magnetic field of 1 T. Next, the SOT MTJs were patterned through i-line photolithograph and combination of reactive ion etching (RIE) and ion beam etching (IBE). The optimized IBE can stop the etching exactly on the SOT track determined by signals of the second ion mass spectrometer. 700 × 2100 nm^2 MTJs are successfully patterned with just etch stop

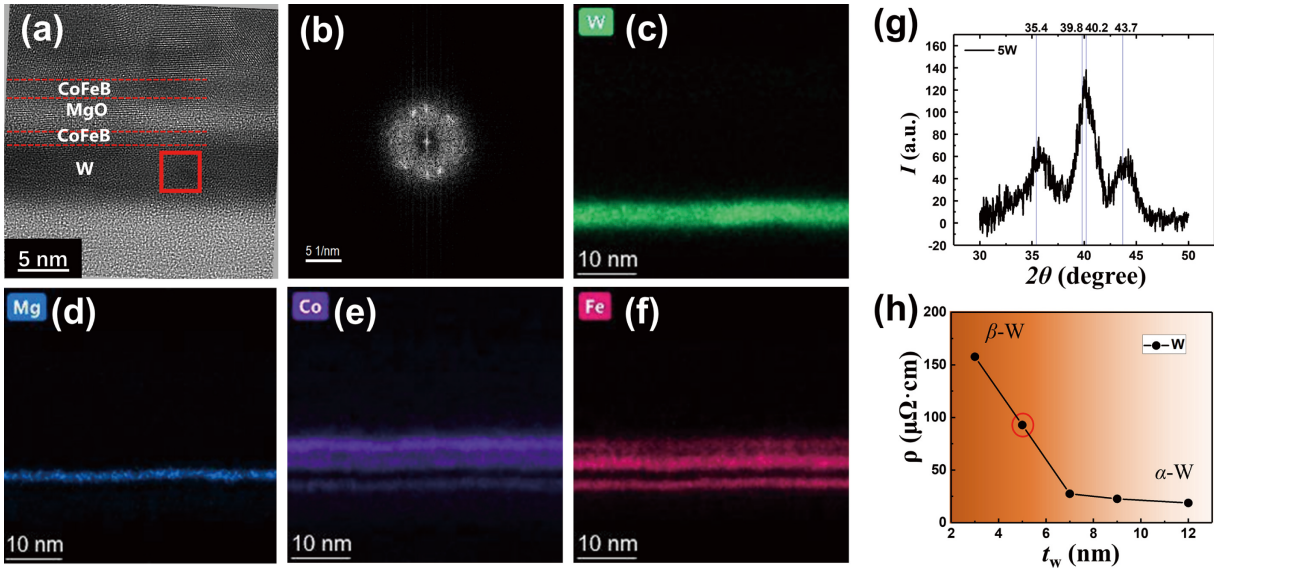

Fig. 2. (Color online) Detailed microstructure of the MTJ film stack and the resistivity of W. (a) TEM diagram of the MTJ film stack. (b) Nano-beam diffraction analysis of W captured from the red box in (a). EDS mappings of (c) W, (d) Mg, (e) Co and (f) Fe. (g) The XRD curve for a simplified film structure of W/CoFeB/MgO/Ta. (h) The resistivities of W with various thicknesses. The resistivity of 5 nm W is highlighted by red circle. The orange color gradient indicate the W phase transition.

at the SOT track layer surface, non-residual at the side wall of the MTJ, and low damage at the same time (Fig. 1(b)). In subsequent devices tests, the open rate and short rate of the full wafer are less than 5%. The baseline devices are designed as so-called "Type-Y" MTJs[25] with an ellipse of a short axis a = 700 nm along the SOT track direction, i.e., x-axis. The long axis has a width with a 3 : 1 aspect ratio to the short axis, i.e., b = 2100 nm, pointing to the direction perpendicular to the SOT track (y-axis). Meanwhile, few other MTJs with smaller critical dimensions (CD), such as a = 300 nm and 500 nm, are also patterned with various aspect ratios for the size dependence study purpose. After *in-situ* encapsulations, the SOT track is patterned to a dumbbell shape having 2500 nm width as shown in the bottom of Fig. 1(e). The width of the SOT track is larger than that of the MTJ long axis width b and has enough overlay margins that take account of our process limitations. Finally, top electrodes are fabricated using a common Al pad process. After fabrications, the electrical tests, e.g., R–H, R–V and so on were carried out. These tests allow us to systematically investigate the performance of devices, which include short pulse width switching probability, reliability performance, such as endurances, and data retentions. The R–H loop was performed by applying an in-plane magnetic field of –100 – +100 Oe along the long axis while the MTJ junction resistance was read. The R–V loop was tested using a 200-mm probe station with Keysight 2912b to read the MTJ junction resistance while applying a –2 – +2 V voltage to the SOT channel. Keithley 4200 was used to provide the short pulse for switching probability and endurance measurements. We defined the TMR ratio as $(R_{AP} - R_P)/R_P$, where R_{AP} and R_P are the resistances for the antiparallel and parallel magnetization configurations between the free layer and the reference layer.

We first describe the structural properties of the prepared SOT MTJs. Detailed structural information of the MTJ film stack was analyzed by the TEM. The high-resolution TEM (HRTEM) images are shown in Fig. 2(a) which are captured from the Fig. 1(b) sample. The images show flat and clear interfaces between W/CoFeB/MgO/CoFeB layers. Simultaneously with the HRTEM, energy dispersive X-ray spectroscopy (EDS) mapping analysis was performed for the same sample. Figs. 2(c)–2(f) are the corresponding EDS mappings of each element; that is, W, Mg, Co, and Fe, respectively. These images suggest that each layer is uniformly deposited, indicating no clear interdiffusion at the 300 °C annealing temperature. We also performed nano-beam diffraction analysis through fast Fourier transforms (FFT) from HRTEM images to further characterize the film quality, especially focused on the W layer. Fig. 2(b) is the FFT analysis image of the W layer from the selected red box region in Fig. 2(a). As can be seen, Fig. 2(b) shows a vague halo combining with a few weak diffraction spots, which suggests our 5 nm W is a more amorphous-like film with some lattice fringes coexisting. The spots likely correspond to α-W {110}[32]. However, it is hard to distinguish between the α-W {110} and the β-W {210} since the inter-planes' distances are close to each other. From the FFT results, we could not identify the presence of the β-W. The simplified film structure, which is the bottom part of the SOT MTJ stacks and consisting of W/CoFe/MgO/Ta, was carried out for the X-Ray Diffraction (XRD) measurements. From Fig. 2(g), the XRD clearly shows β-W {200} and {211} peaks besides β-W {210} and/or α-W {110} peaks. The resistivities of W with various thicknesses (Fig. 2(h)) were also measured in this kind of short stack structure. The resistivity of 5 nm W is around 100 μΩ·cm, which is just at the median point between the β-W and α-W resistivities. This resistivity result indicates that our prepared 5 nm W is at the β to α phase transition boundary and it is consistent with the observations from the previously discussed structural properties analysis. In conclusion, we observed the co-existence of α-W, β-W and amorphous W for our 5 nm W SOT track that may provide reasonable SHA.

Furthermore, we describe the electrical characteristics of the fabricated SOT MTJs across the 200-mm-wafer through R–H and R–V measurements at room temperatures. Fig. 3(a) shows typical R–H hysteresis loops of the SOT MTJs. The mag-

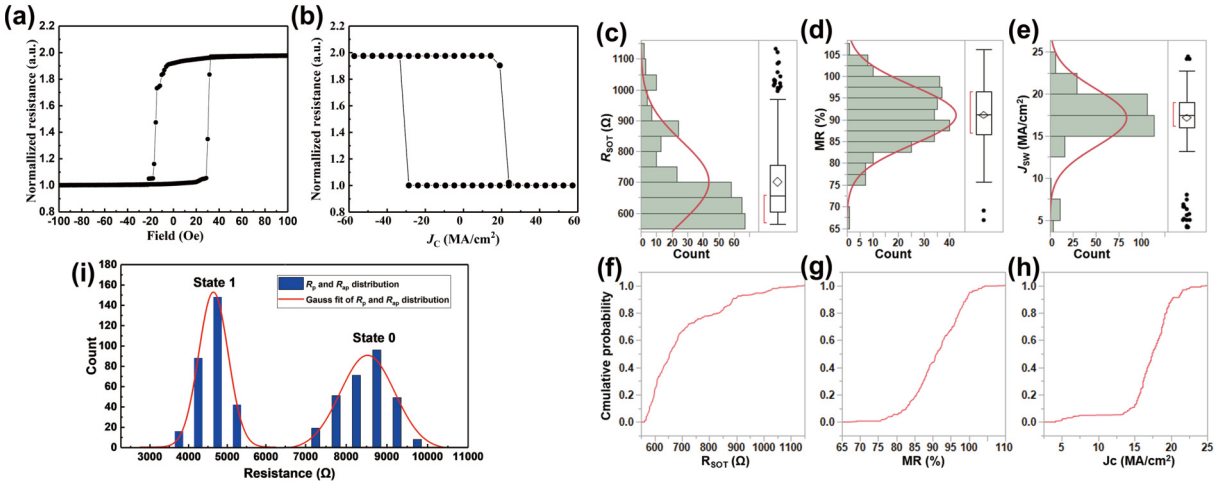

Fig. 3. (Color online) The typical electrical and magnetic properties of the SOT device. The wafer level distribution of the R_{SOT}, MR, J_{SW}, R_{AP} and R_P. (a) Typical R–H hysteresis loops of the SOT-MTJs. (b) Typical R–J hysteresis loops of the SOT MTJs obtained from the same sample in (a). The wafer-level electrical distribution of (c) R_{SOT}, (d) MR, (e) J_{SW}. (f–h) The corresponding CDF plots. (i) The bit-cell resistance distributions of SOT MTJs for both P and AP states.

netic fields were applied along the in-plane magnetic easy axis during the R–H measurements. The SOT MTJs show a high TMR ratio of 102% as seen in Fig. 3(a), which is close to that of 114% obtained from the CIPT measurements at the film stack level. This result indicates a low damage during the MTJ fabrication process and low series resistances. Fig. 3(b) shows the corresponding R–J curves obtained from the same junction in Fig. 3(a). The TMR ratio of 107% obtained from the R–V curves is comparable to that of the value from the R–H curves. The switching current density is –25 MA/cm^2 for P to AP direction and +29 MA/cm^2 for the AP to P direction. The unbalanced switching current density in two directions is probably due to the non-zero magnetic stray field from the SAF layers. The average current density of 20 MA/cm^2 is comparable to the commercialized STT MRAM[33]. However, with smaller channel resistances than those of STT MTJ, our results indicate a possibly lower write power consumptions in SOT MTJ devices.

Next, the wafer-level distributions of the previously-mentioned electrical parameters were examined. Figs. 3(c)–3(e) show the distributions of electrical parameters such as R_{SOT}, TMR ratio, and the J_{SW} (switching current densities) of over 286 measured normal SOT MTJs across the 200-mm wafer. As references, the box plots are also shown on the right-hand side of the distribution pictures. Figs. 3(f)–3(h) are corresponding cumulative distribution function (CDF) plots as an alternative view of the distributions besides the box plots. As can be seen, R_{SOT} is screwed to one side with a median value of 650 Ω, matching with the designed resistance value. The outscrewed data (sigma% = 18%), especially on higher resistance side, probably happens because of the etch depth non-uniformity due to the ultra-thin W layer we used. Nevertheless, the range and sigma of the R_{SOT} are still acceptable, well within the CMOS transistor driving capability (this will not be discussed here as it is beyond the scope of this paper). Meanwhile, TMR ratios and J_{SW} both follow the normal distributions, with sigma% of 7% and 20%, respectively. The relatively high sigma% of J_{SW} is probably linked to the non-uniformity of R_{SOT} that we observed. To improve R_{SOT} and associated J_{SW}, uniformity robust etch process and thicker SOT track materials might be necessary. Fig. 3(i) shows the bit-cell resistance distributions of 286 SOT MTJs for both P and AP states. A wide separation between R_P and R_{AP}, about ~5 R_P sigma, indicates that there is enough read margin to use differential sensing[34] or self-reference sensing methods[35]. This might provide a possibility for utilization of the middle point sensing method[36] but some efforts still needed for the process integration improvement. Overall, wafer level electrical characterizations suggest a relatively good uniform process capability of our 200-mm SOT MRAM manufacturing platform.

The CD dependence of the switching current in our SOT MTJs was also investigated. R–V measurements were carried out for the SOT MTJs with various short axis a and long axis b. It should be noted that the width of the bottom electrode is the same for different MTJ CDs. Fig. 4(a) shows the normalized switching current as a function of long axis b. The I_{SW} is normalized by the average value of the current for MTJs with baseline size b = 2100 nm. Surprisingly, the current decreases strongly and monotonically with the scaling of the MTJ long axis b. The I_{SW} of MTJs with b = 500 nm is almost 50% of that baseline MTJ with b = 2100 nm. Even though the current drop is suitable for CMOS integration, this behavior is still different from the well-known SOT critical switching current equation, as follows[37]:

$$I_{SW} = \frac{2e}{\hbar}\frac{\alpha\mu M_S t_{FL}}{\xi}(H_{ani} + H_{eff})wd, \quad (1)$$

because there are no MTJ CD related parameters can be found in the equation.

In Eq. (1), e is the electron charge, $\hbar$ is the reduced Planck constant, α is the damping constant, μ is the permeability of vacuum, M_S is the saturation magnetization, t_{FL} is the free layer thickness, ξ is the spin polarization of spin current, H_{ani} is the magnetic shape anisotropy field, H_{eff} is related to the demagnetization field, w and d are the SOT HM channel width and thickness, respectively.

We note that the equation is an ideal case, which does not consider the current shunting effect. Severe current shunting would have happened in SOT MTJ devices when the cur-

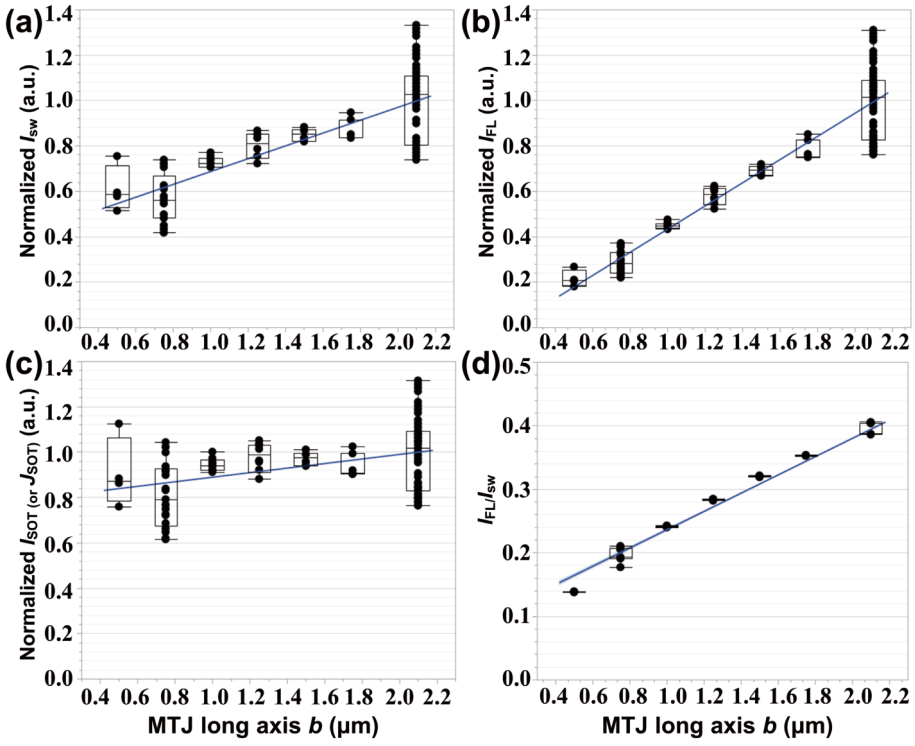

Fig. 4. Normalized (a) I_{SW}, (b) I_{FL}, (c) I_{SOT}, and (d) I_{FL}/I_{SW} as functions of MTJ long axis b. The data are normalized by the average value of MTJ with $b = 2100$ nm.

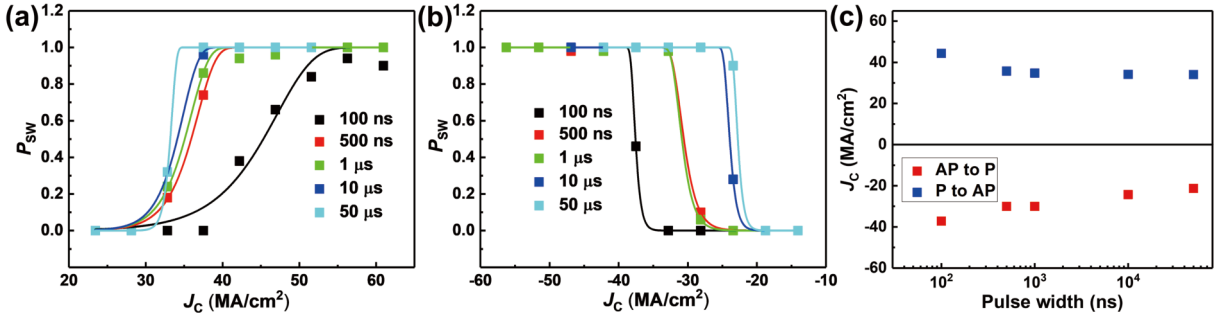

Fig. 5. (Color online) The switching probability (P_{SW}) as a function of applied voltage when pulse widths were varied from 50 μs down to 100 ns for both (a) P-to-AP and (b) AP-to-P directions. (c) The extracted J_C at different pulse width for both P-to-AP and AP-to-P directions when P_{SW} = 50%.

rent is applied on the SOT track because the free layer resistance, i.e., CoFeB, is lower than that of SOT HM, i.e., W in our case. We then use a simplified parallel circuit model[38] to extract the current passing through the W contributing to the switching and another portion of current passing through the free layer, accordingly.

$$I_{SW} = I_{SOT} + I_{FL}, \tag{2}$$

$$I_{SOT}/I_{FL} = \rho_{CFB} wd/\rho_W bt, \tag{3}$$

where w is the SOT channel width 2500 nm, d is the SOT W channel thickness 5 nm, b is the MTJ long axis varied from 500 to 2100 nm, t is the free layer thickness 1.3 nm, ρ_{CFB} is the resistivity of free layer 127 $\mu\Omega$·cm, and ρ_W is the resistivity of W 90 $\mu\Omega$·cm. After calculations, the normalized I_{FL} and I_{SOT} are illustrated in Figs. 4(b) and 4(c). It is clear that the normalized I_{FL} declines 80% from the baseline values. However, I_{SOT} shows only a minor change of ~10%, suggesting that charge-to-spin conversion efficiencies are similar with different CDs and the equation (1) is still valid when CD changes. We also checked the ratios of I_{FL}/I_{SW} as shown in Fig. 4(d), which follows the trends of CD dependence of I_{FL} as the I_{FL} reduction plays a dominant role in the results of Figs. 4(b) and 4(c). Based on the results, the CD dependence of I_{SW} could be explained by minimizing the current shunting effect as CD shrinks. Therefore, beyond enhancing charge-to-spin conversion efficiency, eliminating the current shunting effect would be important for the switching current reduction of SOT MTJ devices to match with the CMOS scaling.

The switching current for the SOT MTJ devices was further investigated with various pulse widths (from 100 ns to 50 μs) applied on the W track. Figs. 5(a) and 5(b) show the switching probability (P_{SW}) as a function of applied voltage when pulse widths were varied from 50 μs down to 100 ns for both P-to-AP and AP-to-P directions. As can be seen, the P_{SW} changes sharply from 0 to 1 with only about 10% of switching current densities increasing, indicating a reliable switching occurred for our SOT MTJ devices. We also note that the current densities obviously increase with the decreasing of pulse widths, which is like the STT switching

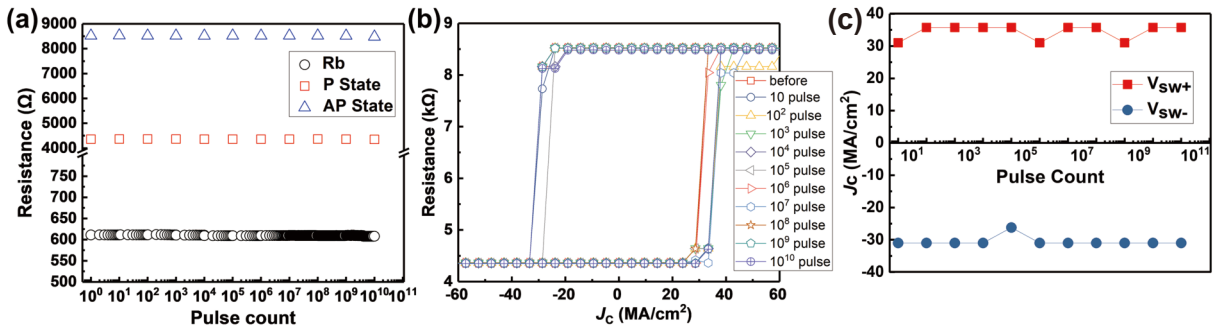

Fig. 6. (Color online) (a) R_{SOT}, R_P, R_{AP} measured after the corresponding cycling current pulses for a typical SOT-MTJ device. (b) The MR loops were recorded multiple times at each power of 10 pulses up to 10^{10}. (c) The extracted J_{SW} from (b) multiple times at each power of 10 pulses.

behavior[39]. Similarly, we evaluated the dependence of the switching current on the pulse widths. Fig. 5(c) shows switching current density at P_{sw} = 50% of various pulse widths for both P-to-AP and AP-to-P directions, extracted from Figs. 5(a) and 5(b). At 100 ns pulse width, the switching current density is around –37 MA/cm^2 for AP-to-P and +44 MA/cm^2 for P-to-AP, respectively. The values are twice as compared with the DC measurement described before. The switching write current density of SOT MTJ can be expressed as[40]

$$J_C = J_{C0}\left[1 - \frac{1}{\Delta}\ln\left(\frac{t}{t_0}\right)\right], \tag{4}$$

where J_{C0} is the zero-thermal critical switching current, Δ is the thermal stability factor ($\Delta = E_b/k_BT$), E_b is the energy barrier, and t_0 is the initial time for thermally-activated switching, normally 1 ns. From Fig. 5(c), we extract the J_{C0} is around ±38.6 MA/cm^2 by fitting the data using Eq. (4). Despite the large size of the MTJ in our work, the estimated J_{C0} is smaller than that reported in Ref. [41]. Based on the data, our SOT MTJ devices are capable of low power consumption and could match the conventional CMOS operating voltages.

Let us now describe the reliability properties of fabricated SOT MTJ devices. First, we checked the endurance performance, which is theoretically one of the merit points compared with STT MTJ devices[42]. The endurance test was carried out on the device-level by applying current pulse cycles with 200 ns width and constant 58 MA/cm^2 current density. The current density used in the endurance test is 1.5 times large of J_{SW}, taking into account of the wafer-level variations. Fig. 6(a) shows R_{SOT}, R_P, and R_{AP} measured after the corresponding cycling current pulses for a typical SOT MTJ device. As illustrated, there were no apparent changes of R_{SOT}, R_P, and R_{AP} during the test, even after 10^{10} write cycles. The test was stopped just after 10^{10} cycles because of time limitations. Even though we only have data at 10^{10} cycles level, it would be better than those of commercialized embedded STT MRAM devices[43] and would be possible to achieve higher cycles as claimed by the first-generation field-driven toggle MRAM[13]. We also note that the R_{SOT} of W channel remains nearly the same, which satisfies the electromigration (EM) requirement even if it is not a stringent EM qualification method[44]. During the endurance test, the MR loops were recorded multiple times at each power of 10 pulses up to 10^{10} (Fig. 6(b)). The normal *R*–*V* tests were also measured at the same time besides the *R*–*H* tests (Fig. 6(c)). As can be seen, the variations in the TMR ratios and the switching current density of the tested device are less than 1%, respectively. These results show the outstanding endurance and high-reliability of our fabricated SOT MTJ devices.

The data retention performance, which is another reliability metric of the non-volatile memory[45], was also examined. The thermal stability factor (Δ) is the critical parameter that determining data retention. To evaluate Δ, we conducted two kinds of data retention tests, one for the device-level and another for the chip-level. For the device-level measurements, *R*–*H* loops were measured for the same device by 500 times. Then, H_C dependence of switching probabilities is extracted from the *R*–*H* loops. Finally, Δ could be fitted by the following equation[46]:

$$P_{SW} = 1 - \exp\left\{-\frac{\tau}{\tau_0}\exp\left[-\Delta\left(1 - \frac{H - H_S}{H_k^{eff}}\right)^2\right]\right\}, \tag{5}$$

where τ and τ_0 are the relaxation time and attempt time, typically 1 ns. H is the external magnetic field, H_S is the coupling field due to the magnetic stray field, and H_k^{eff} is the anisotropy field. Fig. 7(a) shows the extracted switching probabilities as a function of the external magnetic field and the corresponding fitting curve in red. The fitting Δ is around 100 k_BT, which is large enough for Gb-size memory array maintaining the data over 10 years. We also checked the Δ for the MTJs with various CDs which are described before based on 7 devices for every CD by the same method as shown in Fig. 7(b). The diamond plots of Δ are comparable for the MTJs even if *b* scales down to 1000 nm. This probably happens because our MTJs' CD is still large. However, please note that Eq. (5) is assumed to be valid for the single magnetic domain[47]. Then, the fitted Δ would be overestimated as our junction size is much larger than the typical single domain (<100 nm). To accurately obtain the Δ values, the chip-level retention test was conducted generally using the thermal acceleration test, which has been preferred in the industry. We estimate 200-mm-wafer level data retention performance by checking the failure-bit rate of the array through baking the wafer at 200 °C with several baking time. Fig. 7(c) shows the failure-bit rates of different bake time; that is, 12, 24, and 48 h at 200 °C, respectively. We then, used the Eq. (6) as follows to fit the chip-level Δ[48]:

$$\ln(F) = \ln(t) + \ln(F_0) - \left(\Delta - \frac{\Delta_{sigma}^2}{2}\right), \tag{6}$$

where F is the failure-bit rate, t is the bake time, Δ_{sigma} is the deviation of Δ. Here, we roughly use 10% to estimate the

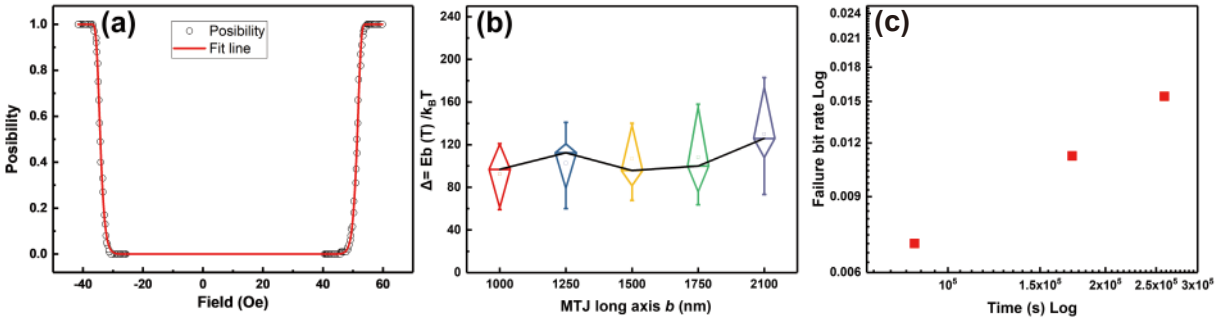

Fig. 7. (Color online) (a) The extracted switching probabilities as a function of the external magnetic field and the corresponding fitting curve. (b) Diamond plots of Δ for the MTJs with various MTJ long axis b. (c) The failure-bit rates of different bake time, i.e., 12, 24, 48 h at 200 °C, respectively.

Δ_{sigma}% for the fitting, which is from the wafer-level R_P distribution mentioned earlier. The transmitted of the data retention is according to the fitting between different temperature vs Δ in the literature. From the fitting, the thermal stability factor Δ is 55 transmitting to our working temperature 85 °C[49], which satisfies the 10-years device storage requirements for 1 kb SOT MTJ array. There are two possible reasons for the relatively low chip-level Δ. The first is the process variations mentioned above, and the process can be improved by further optimizing the lithography and etch process to minimize the damage to the free layers[50]. The second is that we use a single 1.3 nm-thick CoFeB free layer in the current stack, which probably cannot provide a sufficient energy barrier if we peruse the Mb-level chip. Further stack engineering is required, such as changing the single CoFeB free layer to a double ferromagnetic or synthetic antiferromagnetic free layer design[22].

3. Conclusion

In summary, we successfully demonstrated the capability of manufacturing in-plane field-free-switching SOT MTJ devices in the 200-mm-wafer platform. The devices exhibit low critical switching current density J_C ~ 40 MA/cm^2 at 100 ns, high TMR exceeding 100%, excellent thermal stability E_b > 50 k_BT satisfying the 10-years device storage requirements and ultra-high endurance over 10^{10} cycles under 200-ns-pulses with current density of 58 MA/cm^2, which is 1.5 times large of J_C. Most importantly, decent variations of 18%, 7%, and 20% were achieved for the SOT channel resistance R_{SOT}, MTJ resistance, and TMR ratios, respectively in 200-mm-wafer. The results encourage us to explore large size SOT MRAM arrays further. The large size SOT MRAM chips are suitable not only for the memory but also for hybrid CMOS/SOT MRAM logic applications, such as the in-memory computing field.

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References

[1] Dieny B, Prejbeanu I L, Garello K, et al. Opportunities and challenges for spintronics in the microelectronics industry. Nat Electron, 2020, 3, 446

[2] Apalkov D, Dieny B, Slaughter J M. Magnetoresistive random access memory. Proc IEEE, 2016, 104, 1796

[3] Zhang Y, Zhao W S, Klein J O, et al. Spintronics for low-power computing. 2014 Design, Automation & Test in Europe Conference & Exhibition, 2014, 1

[4] Chiang H L, Wang J F, Chen T C, et al. Cold MRAM as a density booster for embedded NVM in advanced technology. 2021 Symposium on VLSI Technology, 2021, 1

[5] Antonyan A, Pyo S, Jung H, et al. Embedded MRAM macro for eFlash replacement. 2018 IEEE International Symposium on Circuits and Systems, 2018, 1

[6] Naik V B, Lee K, Yamane K, et al. Manufacturable 22nm FD-SOI embedded MRAM technology for industrial-grade MCU and IOT applications. 2019 IEEE International Electron Devices Meeting, 2019, 2.3.1

[7] Chang L, Fried D M, Hergenrother J, et al. Stable SRAM cell design for the 32 nm node and beyond. 2005 Symposium on VLSI Technology, 2005, 128

[8] Chen Y H, Chan W M, Wu W C, et al. A 16nm 128Mb SRAM in high-κ metal-gate FinFET technology with write-assist circuitry for low-VMIN applications. IEEE J Solid-State Circuits, 2015, 50, 170

[9] Thomas L, Jan G, Serrano-Guisan S, et al. STT-MRAM devices with low damping and moment optimized for LLC applications at Ox nodes. 2018 IEEE Int Electron Devices Meet IEDM, 2018, 27.3.1

[10] Wang K L, Alzate J G, Amiri P K. Low-power non-volatile spintronic memory: STT-RAM and beyond. J Phys D, 2013, 46, 074003

[11] Wang S D, Lee H, Ebrahimi F, et al. Comparative evaluation of spin-transfer-torque and magnetoelectric random access memory. IEEE J Emerg Sel Top Circuits Syst, 2016, 6, 134

[12] Endoh T. Nonvolatile logic and memory devices based on spintronics. 2015 IEEE International Symposium on Circuits and Systems, 2015, 13

[13] Engel B N, Akerman J, Butcher B, et al. A 4-Mb toggle MRAM based on a novel bit and switching method. IEEE Trans Magn, 2005, 41, 132

[14] Slonczewski J C. Current-driven excitation of magnetic multilayers. J Magn Magn Mater, 1996, 159, L1

[15] Huai Y M, Albert F, Nguyen P, et al. Observation of spin-transfer switching in deep submicron-sized and low-resistance magnetic tunnel junctions. Appl Phys Lett, 2004, 84, 3118

[16] Stiles M D, Zangwill A. Anatomy of spin-transfer torque. Phys Rev B, 2002, 66, 014407

[17] Stiles M D, Miltat J. Spin-transfer torque and dynamics. In: Spin Dynamics in Confined Magnetic Structures III. Springer, 2006, 225

[18] Carboni R, Ambrogio S, Chen W, et al. Understanding cycling endurance in perpendicular spin-transfer torque (p-STT) magnetic

memory. 2016 IEEE International Electron Devices Meeting, 2016, 21.6.1
[19] Li J, Augustine C, Salahuddin S, et al. Modeling of failure probability and statistical design of spin-torque transfer magnetic random access memory (STT MRAM) array for yield enhancement. 2008 45th ACM/IEEE Design Automation Conference, 2008, 278
[20] Mukhopadhyay S, Mahmoodi H, Roy K. Modeling of failure probability and statistical design of SRAM array for yield enhancement in nanoscaled CMOS. IEEE Trans Comput Aided Des Integr Circuits Syst, 2005, 24, 1859
[21] Zhao W S, Zhang Y, Devolder T, et al. Failure and reliability analysis of STT-MRAM. Microelectron Reliab, 2012, 52, 1848
[22] Shao Q M, Li P, Liu L Q, et al. Roadmap of spin–orbit torques. IEEE Trans Magn, 2021, 57, 800439
[23] Guo Z X, Yin J L, Bai Y, et al. Spintronics for energy-efficient computing: An overview and outlook. Proc IEEE, 2021, 109, 1398
[24] Zhu D Q, Guo Z X, Du A, et al. First demonstration of three terminal MRAM devices with immunity to magnetic fields and 10 ns field free switching by electrical manipulation of exchange bias. 2021 IEEE International Electron Devices Meeting, 2021, 17.5.1
[25] Fukami S, Anekawa T, Zhang C, et al. A spin–orbit torque switching scheme with collinear magnetic easy axis and current configuration. Nat Nanotechnol, 2016, 11, 621
[26] Honjo H, Nguyen T V A, Watanabe T, et al. First demonstration of field-free SOT-MRAM with 0.35 ns write speed and 70 thermal stability under 400°C thermal tolerance by canted SOT structure and its advanced patterning/SOT channel technology. 2019 IEEE International Electron Devices Meeting, 2019, 28.5.1
[27] Couet S, Rao S, Van Beek S, et al. BEOL compatible high retention perpendicular SOT-MRAM device for SRAM replacement and machine learning. 2021 Symposium on VLSI Technology, 2021, 1
[28] Rahaman S Z, Wang I J, Wang D Y, et al. Size-dependent switching properties of spin-orbit torque MRAM with manufacturing-friendly 8-inch wafer-level uniformity. IEEE J Electron Devices Soc, 2020, 8, 163
[29] Lourembam J, Huang L S, Chen B J, et al. Multi-state magnetic tunnel junction programmable by nanosecond spin-orbit torque pulse sequence. Adv Electron Mater, 2021, 7, 2001133
[30] Chen G L, Wang I J, Yeh P S, et al. An 8kb spin-orbit-torque magnetic random-access memory. 2021 International Symposium on VLSI Technology, Systems and Applications, 2021, 1
[31] Pai C F, Liu L Q, Li Y, et al. Spin transfer torque devices utilizing the giant spin Hall effect of tungsten. Appl Phys Lett, 2012, 101, 122404
[32] Liu J, Ohkubo T, Mitani S, et al. Correlation between the spin Hall angle and the structural phases of early 5*d* transition metals. Appl Phys Lett, 2015, 107, 232408
[33] Embedded Memories Technology scaling & STT-MRAM for IoT & Automotive. IEEE International Electron Devices Meeting Archive, 2017
[34] Das J, Alam S M, Bhanja S. Non-destructive variability tolerant differential read for non-volatile logic. 2012 IEEE 55th International Midwest Symposium on Circuits and Systems, 2012, 178
[35] Li Z, Yan B N, Yang L, et al. A new self-reference sensing scheme for TLC MRAM. 2015 IEEE International Symposium on Circuits and Systems, 2015, 593
[36] Yun J, Nadeau-Dostie B, Keim M, et al. MBIST supported multi step trim for reliable eMRAM sensing. 2020 IEEE International Test Conference, 2020, 1
[37] Sun J Z. Spin-current interaction with a monodomain magnetic body: A model study. Phys Rev B, 2000, 62, 570
[38] Zhu L J, Zhu L J, Shi S J, et al. Enhancing spin-orbit torque by strong interfacial scattering from ultrathin insertion layers. Phys Rev Appl, 2019, 11, 061004
[39] Lee K, Kang S H. Design consideration of magnetic tunnel junctions for reliable high-temperature operation of STT-MRAM. IEEE Trans Magn, 2010, 46, 1537
[40] Rahaman S Z, Wang I J, Chen T Y, et al. Pulse-width and temperature effect on the switching behavior of an etch-stop-on-MgO-barrier spin-orbit torque MRAM cell. IEEE Electron Device Lett, 2018, 39, 1306
[41] Liu L Q, Pai C F, Li Y, et al. Spin-torque switching with the giant spin Hall effect of tantalum. Science, 2012, 336, 555
[42] Sura A, Nehra V. Performance comparison of single level STT and SOT MRAM cells for cache applications. 2021 25th International Symposium on VLSI Design and Test, 2021, 1
[43] Song Y J, Lee J H, Han S H, et al. Demonstration of highly manufacturable STT-MRAM embedded in 28nm logic. 2018 IEEE Int Electron Devices Meet IEDM, 2018, 18.2.1
[44] JC-14 Quality and reliability of solid state products. Avilable from: https://www. jedec. org/committees/jc-14
[45] Tsunoda K, Aoki M, Noshiro H, et al. Area dependence of thermal stability factor in perpendicular STT-MRAM analyzed by bi-directional data flipping model. 2014 IEEE International Electron Devices Meeting, 2014, 19.3.1
[46] Sato H, Yamanouchi M, Ikeda S, et al. Perpendicular-anisotropy CoFeB-MgO magnetic tunnel junctions with a MgO/CoFeB/Ta/CoFeB/MgO recording structure. Appl Phys Lett, 2012, 101, 022414
[47] Kim W, Jeong J H, Kim Y, et al. Extended scalability of perpendicular STT-MRAM towards sub-20nm MTJ node. 2011 Int Electron Devices Meet, 2011, 24.1.1
[48] Thomas L, Jan G, Zhu J, et al. Perpendicular spin transfer torque magnetic random access memories with high spin torque efficiency and thermal stability for embedded applications. J Appl Phys, 2014, 115, 172615
[49] Thomas L, Jan G, Le S, et al. Quantifying data retention of perpendicular spin-transfer-torque magnetic random access memory chips using an effective thermal stability factor method. Appl Phys Lett, 2015, 106, 162402
[50] Endoh T, Honjo H, Nishioka K, et al. Recent progresses in STT-MRAM and SOT-MRAM for next generation MRAM. IEEE Symposium on VLSI Technology, 2020, 1

Hongchao Zhang received the M.S. degree in the school of physics from Qingdao University, Shandong, China, in 2018. He is currently working toward a Ph.D. degree in microelectronics and solid-state electronics at Beihang University, Beijing, China. His current research interests include nanofabrication of magnetic tunnel junctions and the development of SOT MRAM device characteristic techniques.

Hongxi Liu received the Ph.D. degree in Electronics for Informatics from Hokkaido University, Japan, in 2012. He has worked in academia and industry for over 10 years, mainly focusing on the research and development of MRAM technology. He is currently in charge of the activities of SOT MRAM R&D in Truth Memory tech. Corporation, Beijing, China.

Gefei Wang (M'90) received a B.S. degree in electronics and information engineering in 2012 and a M.S. degree in microelectronics and solid-state electronics in 2015 from Beihang University, Beijing, China. From 2015 to 2019, he received Ph.D. degree in physics from Paris-Saclay University, Paris, France. His research interest includes the development of spin-based nano device modeling and spin-based circuit design, especially in memory design.

Kaihua Cao (M'92) received the B.S. degree in microelectronics from Qingdao University, Shandong, China, in 2014 and the Ph.D. degree in microelectronics and solid-state electronics from Beihang University, Beijing, China, in 2019. From 2015 to 2019, he was a joint Ph.D. student with Institute of Microelectronics of The Chinese Academy of Sciences, Beijing, China. His research interest includes the development of STT-MRAM/SOT-MRAM basic cell nanofabrication and characteristic techniques, and fundamental study of processing in memory device.