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Low-thermal-budget Au-free ohmic contact to an ultrathin barrier AlGaN/GaN heterostructure utilizing a micro-patterned ohmic recess

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Abstract: A pre-ohmic micro-patterned recess process, is utilized to fabricate Ti/Al/Ti/TiN ohmic contact to an ultrathin-barrier (UTB) AlGaN/GaN heterostructure, featuring a significantly reduced ohmic contact resistivity of 0.56 Ω·mm at an alloy temperature of 550 °C. The sheet resistances increase with the temperature following a power law with the index of +2.58, while the specific contact resistivity decreases with the temperature. The contact mechanism can be well described by thermionic field emission (TFE). The extracted Schottky barrier height and electron concentration are 0.31 eV and 5.52×10^{18} cm^{-3}, which suggests an intimate contact between ohmic metal and the UTB-AlGaN as well as GaN buffer. A good correlation between ohmic transfer length and the micro-pattern size is revealed, though in-depth investigation is needed. A preliminary CMOS-process-compatible metal–insulator–semiconductor high-mobility transistor (MIS-HEMT) was fabricated with the proposed Au-free ohmic contact technique.

Key words: ultrathin-barrier AlGaN/GaN heterostructure; low thermal budget; Au-free ohmic contact; micro-patterned ohmic recess; MIS-HEMTs; transfer length

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1. Introduction

The good potential of the ultrathin barrier (UTB) AlGaN/GaN heterostructure has been demonstrated in the fabrication of high uniformity GaN-on-Si power devices and integration of peripheral controlling circuits[1–4]. To integrate GaN power devices with GaN- or even Si-based ICs on the UTB-AlGaN/GaN platform[5, 6], it is highly desirable to develop a CMOS-compatible process[7], in which a low contact resistivity Au-free ohmic contact is critical to both GaN power and RF devices[8–16].

Regrowth of n-type GaN on source–drain region is an effective way to reduce R_c to 0.05–0.15 Ω·mm[17, 18]. However, the procedure adds complexity and a high maintenance cost. N-doped in the ohmic region by ion implantation is also useful while extremely high annealing temperature is needed[19]. Utilizing the Ti_xAl_y alloy instead of multilayers as contact metal schemes has been demonstrated as being efficient but the required annealing temperature is also high (880 °C)[14]. A low annealing temperature of less than 650 °C is preferred for the Au-free ohmic contact, in order to mitigate high-temperature annealing-induced degradation of the III-nitride surface and dielectric/III-nitride interface[15, 16]. Previous study has optimized the over-etching condition of a low-pressure chemical vapor deposited SiN_x (LPCVD-SiN_x) passivation layer on the UTB-AlGaN/GaN heterostructure[16], while the obtained ohmic contact resistivity R_C of 1.57 Ω·mm remains too high.

To break the R_C limit of the uniform-ohmic-recess process, a patterned AlGaN layer structure was proposed on Ti/Al/Ni/Au ohmic contact to a conventional AlGaN/GaN heterostructure[17, 18]. However, further research is needed to investigate the effect of such patterning processes on the Au-free ohmic contact to ultrathin-barrier heterostructures. In this work, to lower down the Ti/Al/Ti/TiN-based Au-free ohmic contact to the UTB-AlGaN/GaN heterostructure, a grid-patterned ohmic-recess process with good over-etching tolerance was developed. A significantly reduced R_C of 0.56 Ω·mm was realized at a relative low annealing temperature of 550 °C. CMOS-compatible GaN MIS-HEMTs was also fabricated on the UTB-AlGaN/GaN on the Si platform.

2. Device fabrication

The schematic cross section of the fabricated CMOS-compatible LPCVD-SiN_x/AlGaN/GaN MIS-HEMTs is depicted in Fig. 1(a). The UTB-AlGaN/GaN heterostructure wafer used in this work was grown by metal organic chemical vapor deposition (MOCVD) on a 3-inch Si substrate.

The AlGaN barrier consists of a ~1 nm GaN cap, a ~4 nm $Al_{0.25}Ga_{0.75}N$ layer and a ~1 nm AlN interface enhancement lay-

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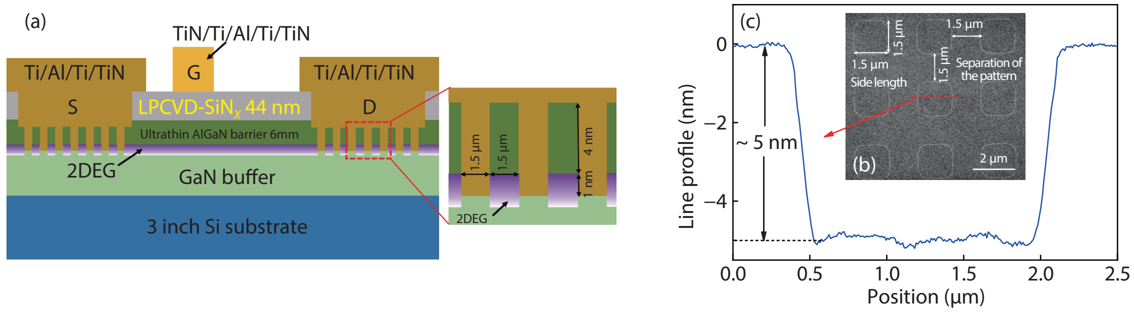

Fig. 1. (Color online) (a) Schematic cross section of the fabricated Si-CMOS-compatible GaN MIS-HEMTs utilizing a micro-patterned ohmic recess. (b) SEM image. (c) Line profile of the micro-patterned AlGaN/GaN heterostructure measured by atomic force microscopy (AFM).

er. The fresh wafers were first cleaned by standard Radio Corporation of America (RCA) treatment, followed by a ~44 nm LPCVD-SiN_x deposited immediately at 780 °C. The high deposition temperature ensures compact film quality and good thermal stability of the SiN_x film, and moreover provides sufficient thermal budget for the subsequent process[4]. The LPCVD-SiN_x layer in the ohmic region was then etched away by low power SF_6/CHF_3 hybrid plasmas with 20% over-etching time[16], yielding a squared ohmic contact region of 100 × 100 μm^2. The 20% over etching resulted in about 2 nm AlGaN barrier removal. Another photolithography was conducted to form uniformly distributed square patterns with separation equal to the side length in the ohmic contact area, as shown in Fig. 1(a). Chlorine-based plasmas were adopted to etching through the AlGaN barrier to expose the GaN buffer. The sides and adjacent spacing of square holes are both 1.5 μm, as measured by a scanning electron microscope (SEM) shown in Fig. 1(b). The recess depth is determined to be ~5 nm (corresponding to ~1 nm over recess of GaN buffer) by an atomic force microscope (AFM), as shown in Fig. 1(c). Then, device isolation was realized by multi-energy argon ion implantation.

The Ti/Al/Ti/TiN ohmic metal stack was then sputtered to cover the ohmic contact region by another photolithography with a proper wet treatment of the etched surface. The source-drain ohmic contact was then annealed at 550 °C for 90 s in N_2 ambient. Subsequently, a TiN/Ti/Al/Ti/TiN metal stack was sputtered over the LPCVD-SiN_x layer to form a MIS-gated structure. The fabricated MIS-HEMTs were finally annealed at 280 °C for 4 min in N_2 ambient to further improve the thermal stability of the gate. The gate length L_G, gate-to-source L_{GS}, and gate-to-drain distance L_{GS} of the MIS-HEMTs are 2.25, 1.25, and 1.75 μm, respectively.

3. Results and discussion

The transmission line method (TLM) was used for the determination of R_C and R_{SH} for the Au-free ohmic contact utilizing a pre-ohmic micro-patterned recess process, as shown in Fig. 2(a). The typical R_C of the Au-free ohmic contact is determined to be 0.56 Ω·mm, about one-third of our previous reported value (1.57 Ω·mm) without the micro-patterned ohmic recess[16]. The corresponding sheet resistance R_{SH} is extracted to be 385 Ω/sq, indicating that the charge-modulated LPCVD-SiN_x layer has recovered the 2DEG effectively. To verify the process window of such a micro-patterned ohmic recess, another ohmic-patterned sample with about a 10-nm over-recess of the GaN channel was also fabricated, only resulting in a slight increase of R_C, from 0.56 to 0.58 Ω·mm, while with comparable R_{SH} (399 versus 385 Ω/sq), as shown in Fig. 2(a).

Temperature-dependent four-probe measurement was conducted from −50 to 200 °C, in an N_2 protecting environment, to explore the contact mechanism of the fabricated Au-free ohmic contact (Fig. 2(b)). R_C is observed to vary slightly over the temperature range, while R_{SH} increases with the temperature. The latter is due to optical phonon scattering induced by degradation of 2-D electron gas (2DEG) mobility at high temperature ($T >\sim 200$ K)[19–21]. In this case, the mobility follows a power law against temperature, since R_{SH}, which is inversely proportional to the mobility, has a power-law relation with a negative power factor[20–22]. Fig. 2(b) shows the fitting curve of R_{SH} and the extracted power index of +2.58 is consistent with reported values[21]. The corresponding specific contact resistivity ρ_C shown in Fig. 2(c) decreases from 1.95 × 10^{-5} to 2.01 × 10^{-6} Ω·cm² when the temperature increases from −50 to 200 °C[16]. Both ohmic contact mechanisms of the patterned and un-patterned ohmic contacts can be well fitted by the thermionic field emission (TFE) mechanism shown below [16, 20, 23],

$$\rho_C = \frac{1}{qA^*}\frac{k_B^2}{\sqrt{\pi(\phi_B+E_n)E_{00}}}\cosh\left(\frac{E_{00}}{k_BT}\right)\cdot\sqrt{\coth\left(\frac{E_{00}}{k_BT}\right)} \times\exp\left(\frac{\phi_B+E_n}{E_0}-\frac{E_n}{k_BT}\right), \tag{1}$$

where

$$E_0 = E_{00}\coth\left(\frac{E_{00}}{k_BT}\right), \tag{2}$$

and

$$E_{00} = \frac{qh}{4\pi}\sqrt{\frac{N_D}{m^*\varepsilon}}, \tag{3}$$

where $A^* = 4\pi m^* k_B^2/h^3$ is the effective Richardson constant, m^* is the effective mass of the tunneling electrons in (Al)GaN, ε is the dielectric constant of (Al)GaN, Φ_B is Schottky barrier height between (Al)GaN and the ohmic metals, N_D is electron carrier concentration, and E_n is the energy difference between the conduction-band edge and the Fermi level at the AlGaN/GaN interface.

As for the patterned ohmic contact, the TFE fitting yields a Schottky barrier height Φ_B of 0.31 eV and a N_D of 5.5 ×

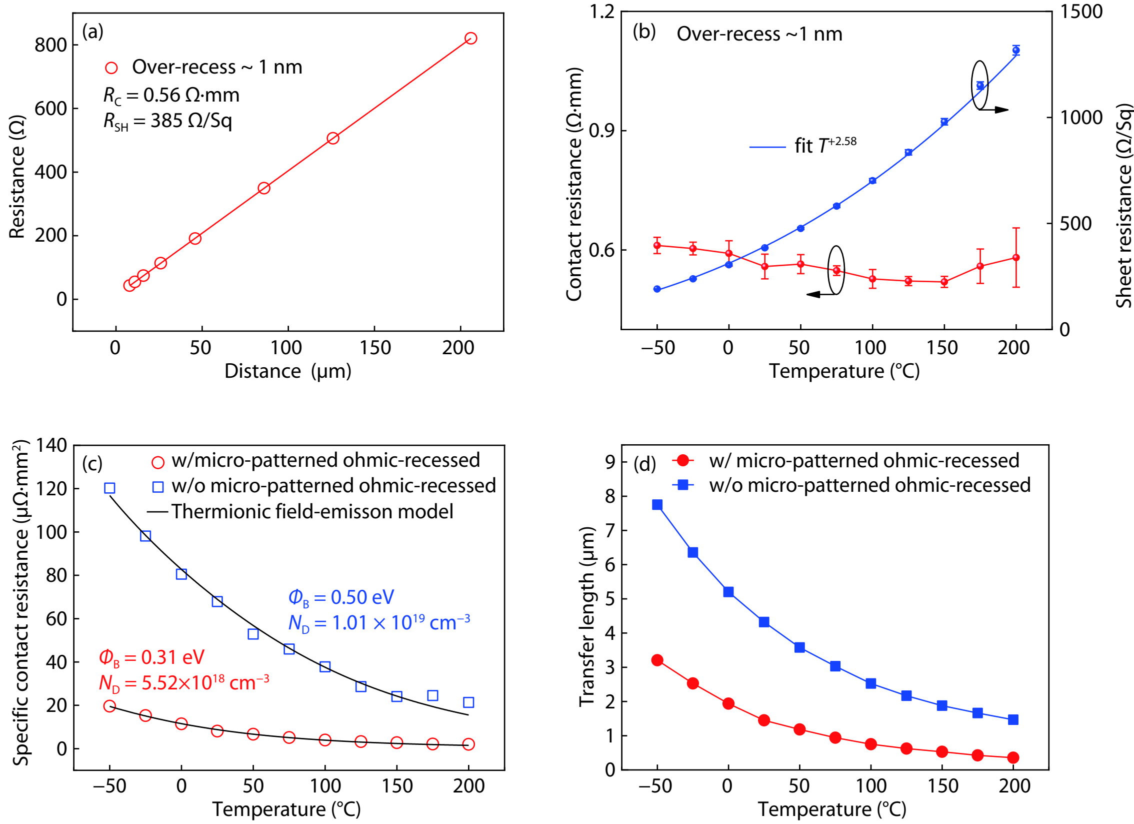

Fig. 2. (a) Linear fit of the fabricated Ti/Al/Ti/TiN ohmic contact resistances versus TLM spacing. (b) Temperature-dependent characteristics: R_C and R_{SH}. (c) ρ_C as fitted by thermionic field emission model. (d) Temperature-dependent transfer length L_T.

Table 1. The summary of micro-patterned ohmic contacts to various AlGaN/GaN heterostructures.

AlGaN/GaN heterostructure	Ohmic metal stack	Annealing temperature (°C)	Recessed-AlGaN barrier thickness in the patterned region (nm)	Side length / Separation of pattern (μm)	L_T (μm)	R_C (Ω·mm)	R_{SH} (Ω/sq)
30 nm $Al_{0.25}Ga_{0.75}N$/GaN[24]	$TiSi_2$/TiN	non-alloy	5	5.00/10.00	13.41	5.86	437
24 nm $Al_{0.3}Ga_{0.7}N$/GaN[17]	Ti/Al/Ni/Au	850	15	0.50/0.50	0.35	0.12	341
2 nm GaN(cap)/18 nm $Al_{0.26}Ga_{0.74}N$/GaN[18]	Ti/Al/Ni/Au	790	12	1.00/1.00	1.10	0.52	475
	Ti/Al/Ni/Au	810	12	1.00/1.00	1.00	0.48	475
	Ti/Al/Ni/Au	790	over-recess 30	1.00/1.00	1.06	0.51	475
	Ti/Al/Ni/Au	810	over-recess 30	1.00/1.00	1.06	0.50	475
(UTB) 1 nm GaN(cap)/ 3 nm $Al_{0.25}Ga_{0.75}N$/ 1 nm AlN/GaN[16]	Ti/Al/Ti/TiN	600	5	/	4.33	1.57	363
(UTB) 1 nm GaN(cap)/ 4 nm $Al_{0.25}Ga_{0.75}N$/ 1 nm AlN/GaN (This work)	Ti/Al/Ti/TiN	550	over-recess ~1	1.50/1.50	1.45	0.56	385
			over-recess ~10	1.50/1.50	1.45	0.58	399

10^{18} cm^{-3}, in contrast to the value of 0.50 eV and 1.01 × 10^{19} cm^{-3} obtained in the un-patterned sample. The lower Φ_B is due to partial transition of metal/AlGaN to metal/GaN contact because of over-etching of the AlGaN barrier. However, over-etching also results in 2DEG depletion in the micro-patterned region, giving rise to a reduced N_D. Further investigation is ongoing to verify the trade-off between Φ_B and N_D and their effects on ρ_c. Transfer length L_T of the fabricated ohmic contacts have also been plotted in Fig. 2(d) with the temperature. The micro-pattern ohmic recess leads to a remarkable reduction of L_T in the measured range. And the shorter current flow distance from the metal (semiconductor) to the semiconductor (metal) can be attributed to the larger lateral contact area to collect current.

To shed light on the effect of pattern size on the contact resistance, a survey of state-of-the-art ohmic contacts that adopts a similar pre-ohmic pattern process is summarized in Table 1. It can be observed that whether the AlGaN barrier in the patterned region is partially or fully recessed, the change of L_T follows closely with the pattern separation. For instance, L_T decreases from 1.45 to 0.35 μm as the separation is reduced from 1.50 (this work) to 0.50 μm[17]. However, there is little correlation between transfer length value and the over-recess depth, since the L_T of ohmic-patterned sample with a

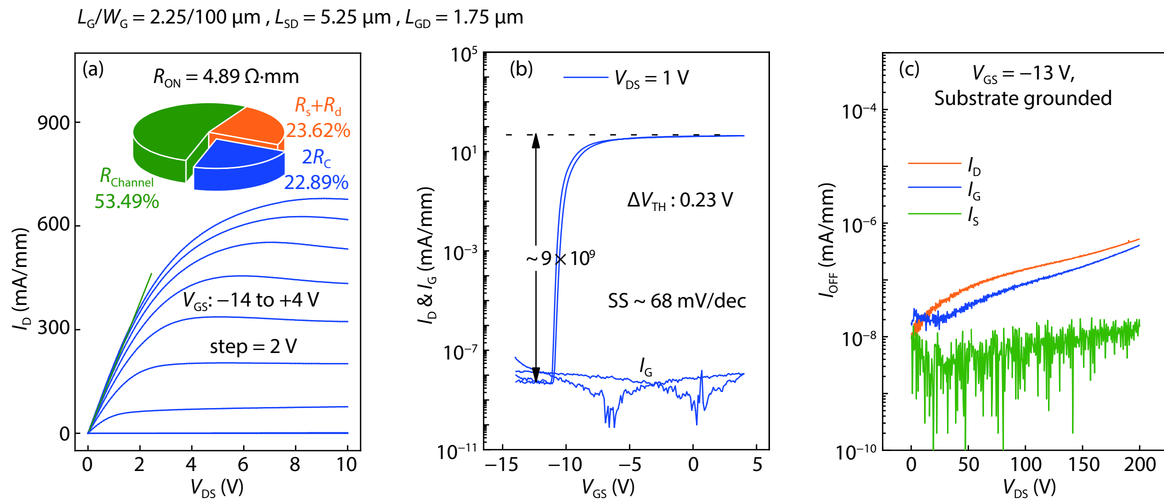

Fig. 3. (Color online) (a) DC output, (b) transfer, and (c) off-state leakage characteristics of the fabricated CMOS-process compatible LPCVD-SiN_x/AlGaN/GaN MIS-HEMTs.

~1 nm and ~10 nm over-recess are the same. Further study is needed to investigate the mechanism behind the correlation between L_T and the separation of the micro-pattern. Anyway, the micro-patterned ohmic recess could be an efficient method to reduce R_C and L_T in Au-free ohmic contacts to the UTB-AlGaN/GaN heterostructure, and the shrinking of L_T will also do good to the scaling down of the active chip area of GaN-based electronic devices.

The pre-ohmic micro-pattered recess process was then implemented in a fabrication of CMOS-compatible LPCVD-SiN_x/AlGaN/GaN MIS-HEMTs, with LPCVD-SiN_x serving as the gate dielectric. The MIS-HEMTs' output characteristics are shown in Fig. 3(a). The on-state resistance (R_{ON}), as extracted from the linear region of the output curve, composed of ohmic contact resistance 2R_C (22.89%), access region resistance R_s + R_d (23.62%) and gate channel resistance $R_{Channel}$ (53.49%), is substantially low owing to the ohmic pattern process. High ON/OFF current ratios (I_{ON}/I_{OFF}) are more than 9 × 10^{10} while low gate leakage (~10^{-7} mA/mm) is also obtained in transfer measurements (Fig. 3(b)), thanks to the high insulating behavior of the LPCVD-SiN_x gate dielectric. Due to the trapping behavior of deep states located at the LPCVD-SiN_x/GaN interface, a clockwise threshold voltage (V_{TH}) hysteresis of 0.23 V is observed at a drain bias of 1 V (Fig. 3(b)). A smaller V_{TH} hysteresis, while a relative lower extrinsic transconductance, can be further realized with proper surface treatments[1]. Moreover, the OFF-state drain and gate current of the MIS-HEMTs with L_{GD} of 1.75 μm, are well suppressed towards V_{DS} of 200 V (Fig. 3(c)). Further work on the implementation of the micro-patterned ohmic recess in enhancement-mode AlGaN/GaN (MIS)HEMTs is ongoing.

4. Conclusion

A pre-ohmic micro-patterned recess process was developed to facilitate low-thermal-budget Au-free ohmic contact to a UTB-AlGaN/GaN heterostructure. The contact mechanism of ohmic-patterned technology on a UTB AlGaN/GaN heterostructure and the relationship between L_T and pattern size were revealed. CMOS-process-compatible SiN_x/AlGaN/GaN MIS-HEMTs were fabricated with the proposed Au-free ohmic contact and LPCVD-SiN_x gate dielectric.

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