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The investigation of DARC etch back in DRAM capacitor oxide mask opening

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Abstract: Opening the silicon oxide mask of a capacitor in dynamic random access memory is a critical process on a capacitive coupled plasma (CCP) etch tool. Three steps, dielectric anti-reflective coating (DARC) etch back, silicon oxide etch and strip, are contained. To acquire good performance, such as low leakage current and high capacitance, for further fabricating capacitors, we should firstly optimize DARC etch back. We developed some experiments, focusing on etch time and chemistry, to evaluate the profile of a silicon oxide mask, DARC remain and critical dimension. The result shows that etch back time should be controlled in the range from 50 to 60 s, based on the current equipment and condition. It will make B/T ratio higher than 70% meanwhile resolve the DARC remain issue. We also found that CH_2F_2 flow should be ~15 sccm to avoid reversed CD trend and keep in-line CD.

Key words: dynamic random access memory (DRAM); oxide mask open of capacitor; capacitive coupled plasma (CCP) etch; dielectric anti-reflective coating (DARC); etch back (EB)

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1. Introduction

The dynamic random access memory (DRAM) industry has addressed an ongoing challenge to shrink the size of the device[1]. It renders the fabrication more and more exact and difficult. Etching capacitor is a critical process in fabricating the DRAM device[2]. We have to balance the dilemma, the trade-off effect between capacitance and leakage current, during the process[3]. Many performances, for instance critical dimension (CD), the ratio of bottom CD to top CD (B/T ratio) and bowing, can affect it. The technological parameters in various steps, such as chemistry, etch time, power and pressure, decide the performances. Therefore, how to control parameters in the capacitor-etching process is very challenging and valuable for shrinking the size of the DRAM device.

To form high-performance capacitors in the DRAM device, most research prefers to develop novel materials for high-dielectric layers[4]. It is effective, however, the cost limits the application. Compared with using novel materials, structure design and process promotion are more practical.

Therefore, we focus on studying and improving the oxide-mask-open process of the DRAM capacitor. The CD and profile of SiO_x will influence the properties of the HM-Si mask (HM hard mask), further influencing the main etch of capacitor. The oxide mask process are consisting of three steps, DARC etch back (EB), SiO_x main etch(ME), and stripping remained carbon.

The strategy and profile of SiO_x mask open are shown in Fig. 1. The DARC layer is generally composed of Si O N for reducing the surface reflection, thus maximizing light collection efficiency in lithography. The carbon layer is set as a mask for following SiO_x ME. DARC and carbon mask here have been already opened by "double-patterning" strategy. The purpose of etch back is to remove DARC on the top of the feature. Typically, due to the similar component of DARC and SiO_x, the SiO_x layer can also been etched to a taper profile in the EB step. Then we use ME step to full open the oxide layer and stop at the HM-Si layer. To obtain more straight holes i.e. high B/T ratio and baseline CD, we usually extend the time for over etch (OE). Finally, we should strip the remaining carbon to avoid some defect issues.

Here, we study DARC etch back due to the importance of beginning. Firstly, we found that DARC etch time can decide the profile of the oxide mask. It can be ascribed to the low selectivity of etching DARC and SiO_2, based on traditional $CF_4/CH_xF_y/O_2$ chemistry. The profile of oxide mask thus become taper in DARC etch back step, which is reversed to our expectation. We would like to obtain a relative straight profile to the end. Thereby, we have to reduce the etch time and extend ME or OE time to obtain more straight holes i.e. high B/T ratio. However, not enough etch back time will result in DRAC remaining. It can lead to defect issues in the integration flow. According to the results, 50–60 s etch time is reasonable and appropriate. To evaluate the effect of DARC etch back on capacitor final CD, we also optimized the CH_2F_2 flow. We found that final CD is increased by 2.4% when CH_2F_2 increases from 15 to 25 sccm. It is an abnormal phenomenon because CH_2F_2 can produce amounts of a sticky C_xF_y polymer based on a free radical coupling mechanism. The polymer will be absorbed on hole side-wall and protect it from the physical bombarment as well as chemical reaction, indicating that higher flow of CH_2F_2 will usually result in smaller CD.

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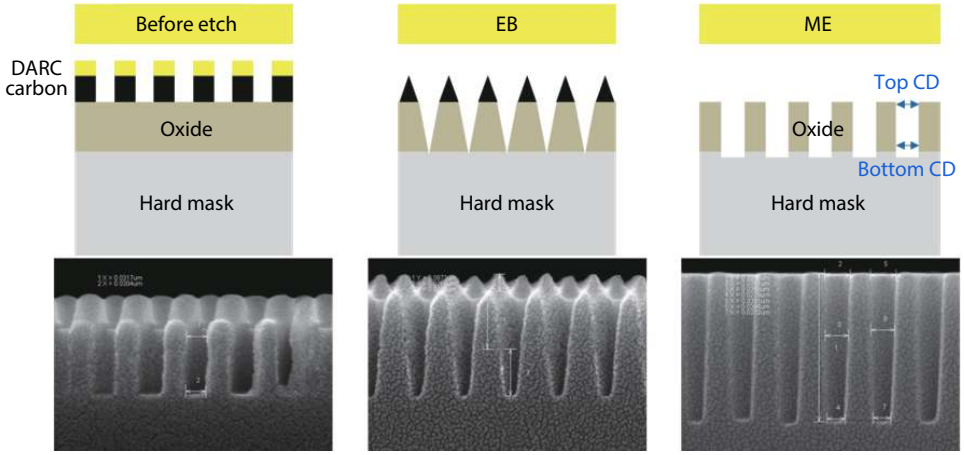

Fig. 1. The strategy of etching oxide mask in the DRAM capacitor.

However, in our case, too much CH_2F_2 will remain in some carbon polymers in the following HM-Si mask open process. It will consume some O_2, which is a protective gas in Si etch, thereby leading to the larger final CD. The results indicate that we can control CH_2F_2 flow in DARC etch back step to change the final CD trend. Compared with the baseline process, our optimized process shows better profile, no DARC remaining and controlled final CD trend. All the results are from the co-work of equipment company and wafer fabrication company, suggesting the necessity and importance of further coporation in developing DRAM capacitors.

2. Experiment

All etching experiments were conducted in 300 mm capacitive coupled plasma (CCP) etch tool with two radio frequency (RF) frequency generator (50–60 MHz source and 2–3 MHz bias power). The etch tool is AMEC HD RIE. Typically, three steps were used to etch oxide masks in a DRAM capacitor: DARC etching back, silicon oxide (SiO_x) main etch and remained carbon mask ashing. $CF_4/CHF_3/CH_2F_2$ chemistry were used to etch DARC (SiON) at etch back (EB) step. $C_4F_6/C_4F_8/Ar/O_2$ chemistry were used to etch oxide (SiO_2) at the main etch (ME) step. O_2 chemistry were used to strip carbon at the strip step.

To avoid wasting resources, here we use "coupon", a small chip sample cut from whole wafer, for experiment. The coupon has already been pre-coated with designed film stack and exposed for following etching process. We then paste the chip on a carrier wafer as a sample. To decrease the variation between the sample and whole wafer, we coat it with photoresist/SiO_2 film stacks. The open ratio of the sample is similar with that of the whole wafer.

A 2×3 cm^2 chip sample was pasted on a 300 mm carrier wafer to test in AMEC lab. The film stack of carrier wafer is photoresist/SiO_2 from top to bottom. The open ratio of photoresist is about 50% with chess board pattern. 300 mm-structure whole wafers were used as samples in CXMT fab.

AMEC lab XSEM and top view metrology tool is Hitachi 4800 SEM. CXMT inline CD track tool is AMAT CDSEM.

3. Result and discussion

3.1. AMEC Lab chip test: Taper profile vs long EB time

To evaluate the effect of etch time step by step, we did 30 s partial etch in EB and ME step respectively. Fig. 2(a) shows that the etch depth, indicating the in-hole etch rate (ER) is 2.36 nm/s. Fig. 2(b) shows that the etch depth after 30 s ME, implying the in-hole ER is 4.76 nm/s. The ratio of in-hole ER between EB and ME step is around 1 : 2. Besides, the post-etch profiles of the oxide layer are also different between two steps. The EB step can form the taper profile while straight profile will be observed in ME step. Those differences in two steps can be ascribed to their chemistry and power[5]. C_4F_y gases with high power will make ER faster and profile more straight due to the strong bombarment at the bottom and protective polymers at the side-wall. It is proved to be beneficial to the oxide-hole etching[6]. The strong ion bombarment can remove bottom polymer and make the surface more reactive. The long-chain polymer produced from C_4F_y gases in plasma, are sticky, thereby can be adsorbed at the side wall for protection, resulting in the anistropic etch i.e. the great capability of the CD and profile control. However, the EB step is designed to etch DARC. DARC is composed of SiO_xN_y. The etching of it is proved to be chemically dominated, suggesting less-polymer chemistry (CH_xF_y) and lower bias power[7]. Therefore, the profile is taper and ER is slower when using the EB step to open the oxide mask. By the way, it is difficult to control the EB step that only etch DARC and stop at OX layer due to the low selectivity based on current condition.

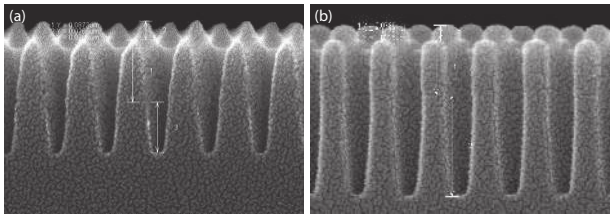

Fig. 2. The XSEM of (a) 30 s partial etch in EB step, (b) 30 s partial etch in ME step.

After partial etch, we start to study full-etch profile and ER. Considering the total thickness of etch layer, we use "60 s EB + 36 s ME" as a starting point to achieve 40% over etch amount (OE), the percentage of OE time. According to our previous experience, enough OE time will make SiO_x holes more straight. The etch time is calculated by the previous ER. Then we split the step time "30 s EB + 51 s ME" and "90 s EB + 21 s

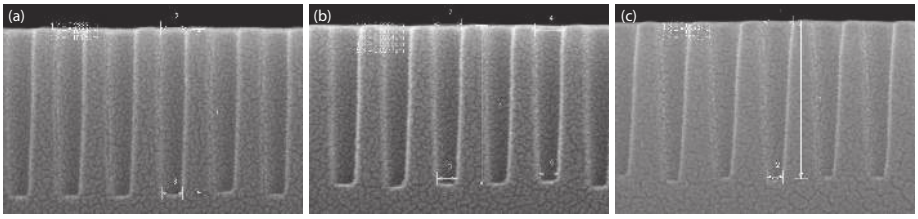

Fig. 3. The XSEM of various profiles with the condition of (a) 30 s EB + 51 s ME, 77% B/T ratio, (b) 60 s EB + 36 s ME, 70% B/T ratio, (c) 90 s EB + 21 s ME, 52% B/T ratio.

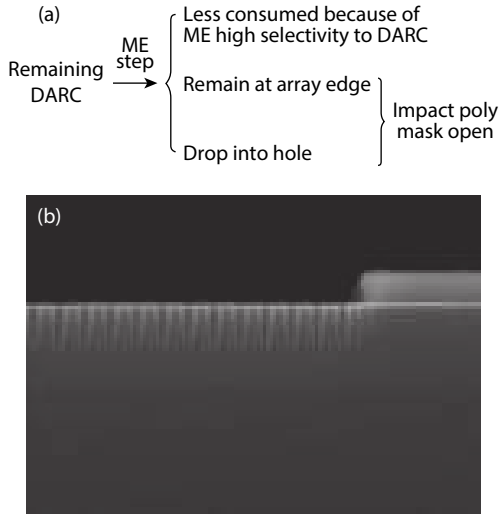

Fig. 4. (a) The DARC remaining issue. (b) The SEM cross section with the conditio of "40 s EB + 0 s ME + 100 s Strip".

ME" to study profile change. The time of two steps are calculated by ER, etch depth and 40% OE amount. We use B/T ratio (Bottom CD/Top CD) to evaluate the vertical index of profile. The CD is measured by SEM data manager software. Finally, we obtain three kinds of profiles with various B/T ratios, for instance 77%, 70% and 52% as shown in Fig. 3. The result indicates that longer EB time will make more of a taper profile and longer ME time will make holes more straight. It is corresponding to the previous analysis when we study partial etch. The proportion of DARC EB is more, the profile of oxide mask is taper. Generally, we prefer a straight profile for the mask open application, suggesting that the long EB time is not appropriate for the desired profile as well as throughput.

3.2. AMEC Lab chip test: DARC remaining issue vs short EB time

According to the feedback of the whole wafer test in Fab, we found that remained DARC after the EB step will lead to further under etch or even defect issue in the following integration flow. Fig. 4(a) shows the model of the remaining DARC issue. Whether the DARC remains at array edge or drops into the hole SiO_x holes will block the following etching. By the way, the DARC remaining at array edge will make remained carbon cannot be stripped in the following step, as shown in Fig. 4(b). It can also result in further defect.

To directly evaluate the remaining DARC, here we observe the top-view pictures of oxide mask by SEM, we provide schematic diagrams in the manuscript, as shown in Fig. 5. The dark areas maintained DARC, including circles between holes and bars at the edge of storage array. Deeper color refers to more severe DARC remaining. We first etch with "0 s EB + 30 s ME" (Fig. 5(a)). We can see plenty of DARC remaining due to the high ER selectivity between OX and DARC in ME step. When EB time increased from 30 to 40 s, DARC remaining at the center of storage array becomes less and even disappeared (Figs. 5(b) and 5(c)). However, 40 s is still not enough to remove the DARC at the edge of storage array (Fig. 5(d)). With 50 s EB, the DARC remaining in array edge obviously becomes less (Fig. 5(f)). And after 60 s EB, all the DARC is removed (Fig. 5(f)).

3.3. CXMT Fab whole wafer test: Inline CD performance vs EB chemistry

Checking inline CD is critical in etching. CD in the forward step will influence that in the next step. Therefore, we should control CD in the SiO_x mask opening well to acquire a good performance in the following process, including the HM-Si mask opening and the capacitor etch. We here name the CD in the oxide mask opening as current CD and the CD in capacitor etch as final CD. Chemistry, power and pressure, for instance, in DARC etch, will decide the current CD. For chemistry, the kinds and flow are both effective on controlling CD. We generally divide gases into two types. The one is "polymer gas", implying some chemistry that can produce protective polymer in plasma based on free radical polymerization, such as CHF_3, CH_2F_2, C_4F_8 and C_4F_6. Polymer gases generally has high C/F ratio and unsaturated bonds. The other one is "clean gas", such as CF_4, with all the saturated backbones. It works for etching but not polymer deposition[8]. Therefore, when we add "polymer gas" and increase the flow, the holes CD will be smaller and ER wil be lower. Actually, due to the complicated reaction in plasma, the experienced rule cannot always be right.

Considering the small CD SiO_x mask, we combine $CF_4/CHF_3/CH_2F_2$ as etching chemistry. Since CH_2F_2 prefers to produce heavy and sticking i.e. long-chain polymer, leading to the best capability of controlling CD, here we study how CH_2F_2 flow affects the current CD and the final CD. It is also a strategy to evaluate the capability of controlling CD on our equipment and process.

As shown in Fig. 6, the current CD decreased from 40.8 to 37.4 nm when CH_2F_2 increasing from 5 to 25 sccm. It is reasonable because more CH_2F_2 will produce more protective polymer, resulting in smaller CD. However, for final CD, the rule is not appropriate. We observed that the final CD decreased from 56.5 to 54.1 nm when CH_2F_2 increasing from 5 to 15 sccm while increased from 54.1 to 55.4 nm when CH_2F_2 increasing from 15 to 25 sccm.

To clarify the reversed CD trend, we firstly tested the etch rate (ER) of the blanket Si_3N_4 wafer, using DARC EB condition, in AMEC lab. In Fig. 7, ER is almost kept when CH_2F_2 in-

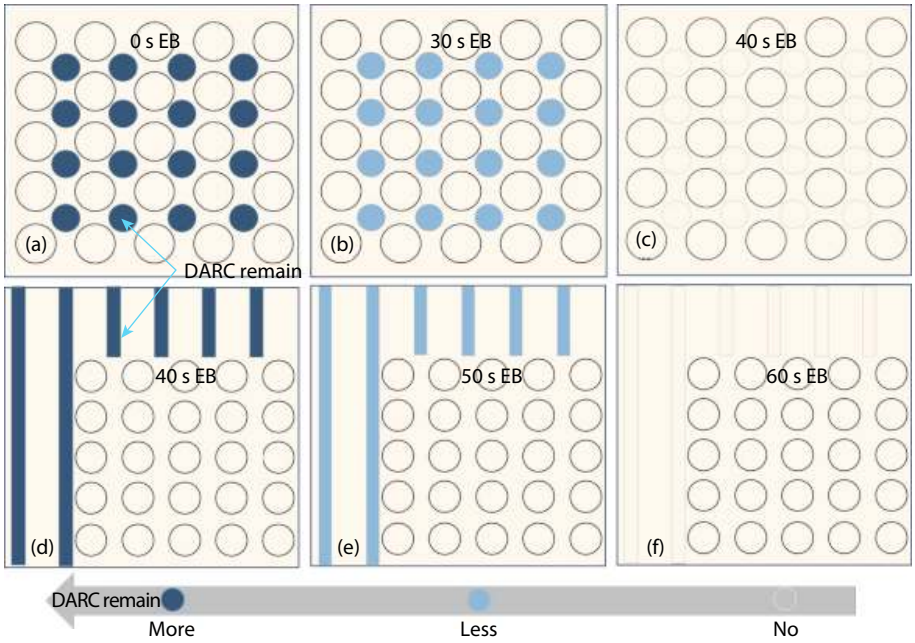

Fig. 5. The SEM top view of the SiO_x mask with the condition of (a) 0 s EB + 30 s ME, (b) 30 s EB + 0 s ME, (c, d) 40 s EB + 0 s ME, (e) 50 s EB + 0 s ME, (f) 60 s EB + 0 s ME.

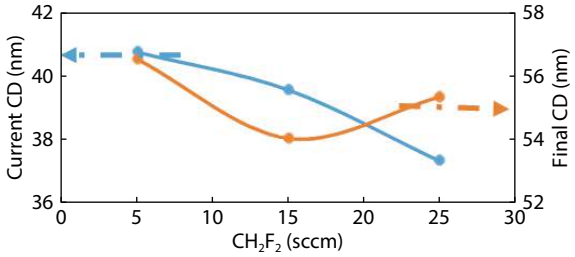

Fig. 6. The trend of SiO_x mask CD (current CD, blue one, left axis) and capacitor CD (final CD, red one, right axis) with CH_2F_2 flow.

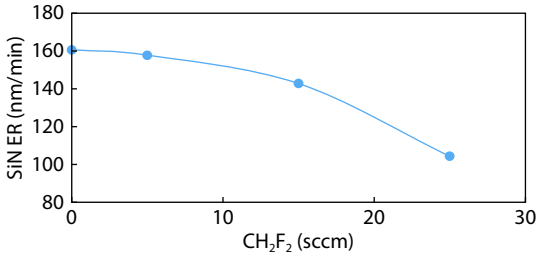

Fig. 7. The blanket Si_3N_4 ER of EB step.

creasing from 0 to 5 sccm. ER is then dropped by ~10% when CH_2F_2 increasing from 5 to 15 sccm. When CH_2F_2 increased from 15 to 25 sccm, ER is decreased by ~30%. According to the previous research on DARC remain issue, we suspect that some DARC will be remained at array edge when the range of CH_2F_2 flow is 15–25 sccm. It will then mean that carbon cannot be stripped.

As shown in Fig. 8, the remained carbon will consume O_2 during the following process of HM-Si mask open, resulting in less SiO_x passivation on the poly-Si side wall[9]. The profile of HM-Si mask will then become more vertical, leading to the bigger final CD. Therefore, we should control the flow of CH_2F_2 to keep the DARC etch amount andavoidd the reversed final CD trend.

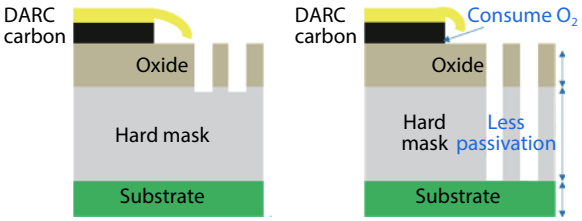

Fig. 8. (Color online) The mechanism of reversed CD trend.

4. Conclusion

To obtain a good performance in the oxide mask open, we have optimized the DARC EB step, including profile, DARC remaining and inline CD. Based on the current equipment and condition, EB time should be controlled under 60 s to make profile B/T ratio higher than 70%. We also suggest that EB time should be more than 50 s to avoid DARC remaining issue. Besides, CH_2F_2 flow is better around ~15 sccm to avoid the reversed CD trend and keep inline CD. Except for providing an appropriate process window, we also figure out the mechanism of three issues, including polymer formation and passivation in DARC EB. We believe that the results of our research will give some suggestions on further relative research. And we really would like to advocate the co-work between equipment company and wafer fabrication company in developing the process of the DRAM capacitor.

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