

# A 15 Gbps-NRZ, 30 Gbps-PAM4, 120 mA laser diode driver implemented in 0.15- $\mu\text{m}$ GaAs E-mode pHEMT technology

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**Abstract:** This paper presents the design and testing of a 15 Gbps non-return-to-zero (NRZ), 30 Gbps 4-level pulse amplitude modulation (PAM4) configurable laser diode driver (LDD) implemented in 0.15- $\mu\text{m}$  GaAs E-mode pHEMT technology. The driver bandwidth is enhanced by utilizing cross-coupled neutralization capacitors across the output stage. The output transmission-line back-termination, which absorbs signal reflections from the imperfectly matched load, is performed passively with on-chip 50- $\Omega$  resistors. The proposed 30 Gbps PAM4 LDD is implemented by combining two 15 Gbps-NRZ LDDs, as the high and low amplification paths, to generate PAM4 output current signal with levels of 0, 40, 80, and 120 mA when driving 25- $\Omega$  lasers. The high and low amplification paths can be used separately or simultaneously as a 15 Gbps-NRZ LDD. The measurement results show clear output eye diagrams at speeds of up to 15 and 30 Gbps for the NRZ and PAM4 drivers, respectively. At a maximum output current of 120 mA, the driver consumes 1.228 W from a single supply voltage of -5.2 V. The proposed driver shows a high current driving capability with a better output power to power dissipation ratio, which makes it suitable for driving high current distributed feedback (DFB) lasers. The chip occupies a total area of  $0.7 \times 1.3 \text{ mm}^2$ .

**Key words:** high current drivers; impedance matching; laser diode driver; optical transmitter; NRZ; PAM4; pHEMT technology.

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## 1. Introduction

There are many modulation schemes that have been studied for different applications in optical communication systems. Non-return-to-zero (NRZ) is widely used due to its simplicity and cost-effectiveness. However, the rapid growth of data traffic has motivated the utilization of other modulation formats with better spectral efficiency. Among them, 4-level pulse amplitude modulation (PAM4) has been adopted for high data rate standards because it doubles the transmission bit rate at the same bandwidth, compared to NRZ binary modulation. The spectral efficiency of the PAM4 modulation scheme comes at the cost of more than a 9 dB SNR penalty due to the reduction of the PAM4 eye height with respect to NRZ. Therefore, PAM4 transmitters are required to deliver a larger output voltage swing to satisfy the same bit error rate (BER) of NRZ. This work demonstrates a dual-mode NRZ/PAM4 driver circuit for high current directly modulated lasers with minimum hardware overhead.

The design of a laser diode driver (LDD) is considered to be one of the most challenging parts among the whole optical transceiver due to the following reasons: firstly, LDDs must deliver large output currents at high speeds, corresponding to small driving signals. For a large output current, a high driving signal and/or wider output transistors are necessary. The high input capacitance of the wide output transistors dramatically decreases the driver operating speed. Therefore, pre-driver stages must precede the output driver so as to deliver a large output current while displaying a small input ca-

pacitance<sup>[1]</sup>.

Secondly, the LDD circuit must employ an output back termination to absorb signal reflections from the laser side when driving commercial laser diodes (LDs)<sup>[2, 3]</sup>, due to the imperfect match between the laser impedance and the printed circuit board (PCB) transmission line (TL) impedance. The simplest way to achieve that is to use passive on-chip back termination resistors across the driver output terminals<sup>[4–8]</sup>, as shown in Fig. 1(a). If the value of this resistor exactly equals the TL impedance, the driver will completely absorb all reflected pulses without any further re-reflections to the laser side. However, the modulation current range is reduced by 50% as half of it is lost in the back-termination resistor. Another method, so-called active back termination (ABT)<sup>[2, 3, 9–12]</sup>, can absorb the loading reflections without compromising the modulation current range. In this method, shown in Fig. 1(b),  $R_T$  is connected between the driver output and the output of a scaled-down replica stage, used to generate an internal estimate of the driver output voltage. Due to the external dc offset of laser diodes, a dc offset cancellation loop circuit is needed to guarantee perfect matching between the dc output voltages of the ABT and the driver<sup>[9, 12]</sup>. Under normal operation, no power is wasted in  $R_T$ , and the modulation current exactly equals the driver tail current. However, this technique needs additional circuitry with extra power and area, and its functionality is degraded at high speeds. Therefore, it is not adopted in this design, and passive back termination resistors are mainly utilized to reduce the physical layout area.

Thirdly, LDDs are power-hungry circuits, especially at high output currents. Therefore, it is highly recommended to reduce the power dissipation of driver circuits to enable the realization of an air-cooled system and simplify the chip

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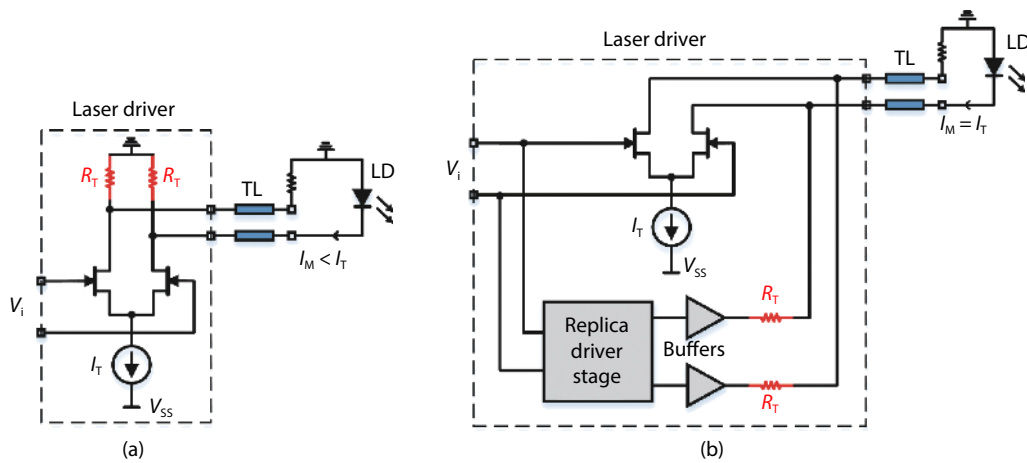


Fig. 1. LDD output stage: (a) with passive back termination, (b) with active back termination.

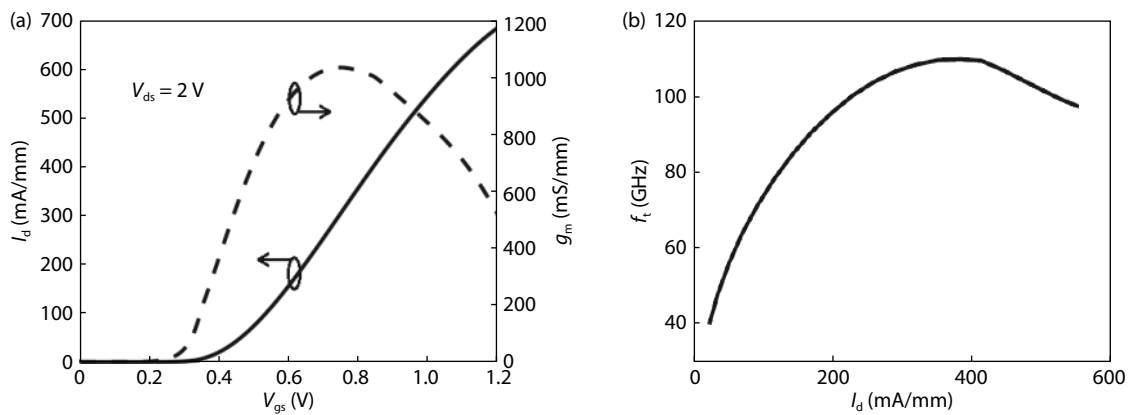


Fig. 2. (a)  $I_d$  and  $g_m$  versus  $V_{gs}$  of pHEMT transistor. (b)  $f_t$  in terms of  $I_d$ .

packaging<sup>[13]</sup>.

Recently, several attempts with excellent results were reported for high current NRZ driver ICs implemented in various high-speed technologies. Using SiGe BiCMOS technology, an 80 mA laser driver operating at 1.25 Gbps, an 80 mA variable data rate driver (155 Mb/s to 4.25 Gbps), and a 50 Gbps optical transmitter with 40 mA output current were reported in Refs. [14, 10, 6], respectively. In pHEMT technology, a 10 Gbps modulator driver with 1.8  $V_{pp}$  single-ended output voltage and a 100 mA 10 Gbps laser driver with active back termination were proposed in Refs. [15, 9], respectively. On the other hand, the CMOS process can still compete to implement such circuits using broadband techniques like inductive peaking<sup>[3, 5, 12, 16–18]</sup> and negative impedance converters<sup>[4, 12, 19]</sup>. These techniques improve the speed, especially when a high driving current capability is required. PAM4 driver ICs were also reported for low current vertical-cavity surface-emitting lasers (VCSELs), at 90 Gbps<sup>[20]</sup> and 56 Gbps<sup>[21]</sup> in SiGe BiCMOS technology and 25 Gbps in 90 nm CMOS<sup>[22]</sup>, and high current distributed feedback (DFB) laser, at 30 Gbps in the 65 nm CMOS process<sup>[11]</sup>.

This paper reports on the design, fabrication, and testing of a 15 Gbps-NRZ, 30 Gbps-PAM4 high current LDD implemented in a 0.15- $\mu\text{m}$  GaAs pHEMT technology. The proposed driver is experimentally verified using a wire-bonded chip-on-board assembly. It can deliver a maximum modulation current of 120 mA to 25- $\Omega$  load.

## 2. Technology

The proposed LDD is designed and fabricated using the 0.15- $\mu\text{m}$  GaAs E-mode pHEMT process. Besides the 0.15- $\mu\text{m}$  E-mode transistor, the process also includes the following elements: PN junction diodes; 50  $\Omega/\text{sq}$ . tantalum nitride (TaN) thin-film resistors; 150  $\Omega/\text{sq}$ . active layer resistors; MIM capacitors with a density of 400 pF/mm<sup>2</sup>; round and square inductors; and two metal layers for interconnecting.

In Fig. 2(a), the variations of the drain current ( $I_d$ ) and transconductance ( $g_m$ ) with gate-source voltage ( $V_{gs}$ ) of the pHEMT are shown. The maximum  $g_m$  is 1000 mS/mm. The drain current is about 430 mA/mm at  $V_{gs} = 0.9$  V. The typical threshold voltage ( $V_{th}$ ) is 0.3 V. The characteristics of unity gain cutoff frequency ( $f_t$ ) in terms of  $I_d$  is depicted in Fig. 2(b). It can be seen that the maximum  $f_t$  is about 110 GHz. These results are promising enough to produce high-speed drivers that can deliver large output currents.

## 3. Architecture and circuit design

The LDD architecture consists of two two-stage slices, as shown in Fig. 3. Each slice includes a pre-driver followed by an output driver, as schematically depicted in Fig. 4. The circuit is designed in a differential current mode logic (CML) topology due to its high speed and excellent immunity to switching noise, as the supply current is maintained relatively constant<sup>[1]</sup>. The circuit is powered using a single negative supply

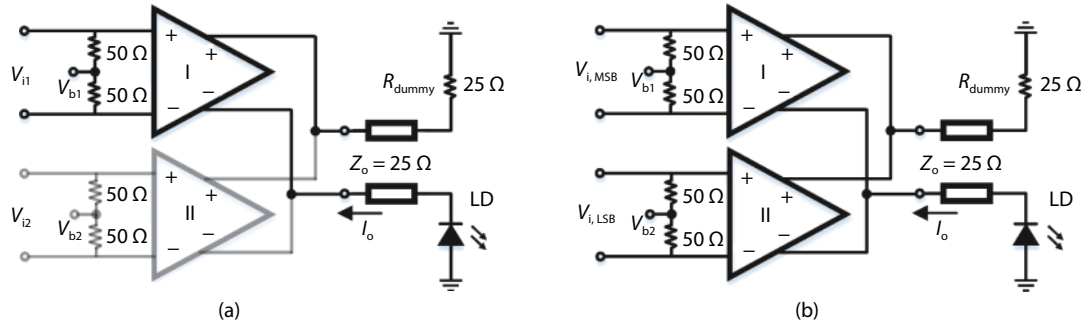


Fig. 3. Driver circuit architecture. (a) 15 Gbps-NRZ LDD with 80 mA output current (Slice I is enabled while slice II is disabled). (b) 30 Gbps (15 Gbaud/s) PAM4 LDD.

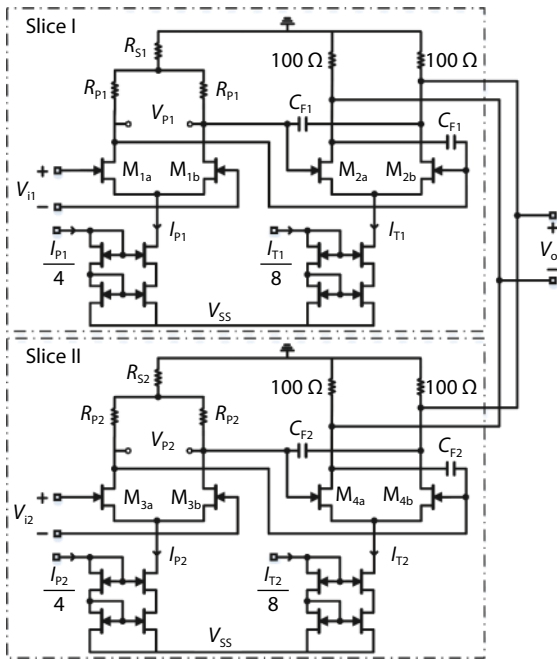


Fig. 4. Circuit diagram of the proposed driver.

voltage ( $V_{SS}$ ) as shown in Fig. 4. A 100- $\Omega$  on-chip resistor is used across the output of each slice, producing a 50- $\Omega$  output back-termination impedance. Each slice presents a 50- $\Omega$  single-ended input impedance using on-chip resistors. The maximum tail currents,  $I_{T1}$  and  $I_{T2}$ , are 120 and 60 mA, and the corresponding output currents of slice I and slice II, when driving 25- $\Omega$  loads, are 80 and 40 mA, respectively. In this design, the cascode current mirror circuits are used to accurately adjust the tail currents due to their low systematic gain-error<sup>[23]</sup>. They also introduce a small output conductance, which improves the common-mode rejection ratio, and consequently, the driver circuit becomes less sensitive to common-mode noise.

The proposed driver can be used in two different functions: firstly, as illustrated in Fig. 3(a), each slice can operate as a stand-alone 15 Gbps-NRZ LDD with a maximum output current of 80 and 40 mA for slice I and slice II, respectively, when driving 25- $\Omega$  lasers. In this case, the NRZ input data is connected to the enabled slice while the other slice is deactivated. The output current can be boosted to 120 mA by simultaneously enabling the two slices and driving them with identical input signals.

Secondly, the circuit can work as a 30 Gbps (15 Gbaud/s)

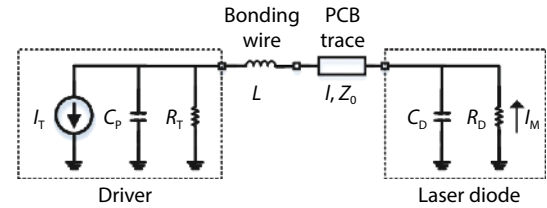


Fig. 5. Equivalent circuit of an LDD connected to an LD using wire-bonded chip-on-board assembly.

PAM4 LDD by combining the two 15 Gbps-NRZ drivers, as shown in Fig. 3(b). According to the possibilities of the most significant bit ( $V_{i,MSB}$ ) and the least significant bit ( $V_{i,LSB}$ ), 00, 01, 10, or 11, the output modulation current will be 0, 40, 80, or 120 mA, respectively. With the PAM4 modulation scheme, the transmission bit data rate is doubled at the same bandwidth compared to NRZ binary modulation.

### 3.1. Output impedance match

Fig. 5 illustrates a simple model of an LDD with passive back termination and the LD, where the LDD and the LD are connected using a wire-bonded chip-on-board assembly. Here,  $C_P$  is the parasitic output capacitance of the driver,  $R_T$  is the passive back termination resistor,  $L$  is the bonding wire inductance,  $C_D$  and  $R_D$  are the parasitic capacitance and the equivalent input resistance of the LD, respectively.  $I_T$  is the tail current of the driver and  $I_M$  is the modulation current of the LD.  $R_D$  equals 25  $\Omega$  and  $C_D$  is assumed to be as low as 0.2 pF. The PCB trace is a 25- $\Omega$  microstrip TL ( $l = 5$  mm), designed using Rogers material, which has a relative dielectric constant ( $\epsilon_r$ ) of 3.48. In this case, only  $C_D$  degrades the matching at the laser side, especially at high frequencies. Fig. 6 shows the 25- $\Omega$   $S_{22}$  curves, simulated at the LD side, at different  $R_T$  and  $L$  values. Without  $R_T$ ,  $I_M$  will exactly equal  $I_T$ , but the maximum  $S_{22}$  in the frequency range from 0 to 15 GHz ( $S_{22,max}$ ) is about -0.03 dB, which seriously degrades the waveform fidelity. At perfect matching ( $R_T = 25 \Omega$ ),  $I_M$  is reduced to  $0.5I_T$  while a better  $S_{22}$  performance is obtained especially at low  $L$  values. If  $R_T$  is somewhat chosen to be greater than 25  $\Omega$ ,  $I_M$  will be larger than  $0.5I_T$  ( $I_M$  equals  $0.667I_T$  and  $0.75I_T$  when  $R_T = 50$  and 75  $\Omega$ , respectively) on the cost of degrading  $S_{22}$  at low frequencies. However,  $S_{22}$  performance at high frequencies may not be significantly impacted (or even improved) where the driver output impedance, parasitic capacitances, and inductances play a significant role<sup>[24]</sup>. When  $L = 0, 0.5,$  and 1 nH,  $S_{22,max}$  values at  $R_T = 25, 50,$  and 75  $\Omega$  are (-12.9, -4, and -1.2 dB), (-7.4, -8.2, and -2.1 dB), and (-4.9, -6, -2.4 dB), re-

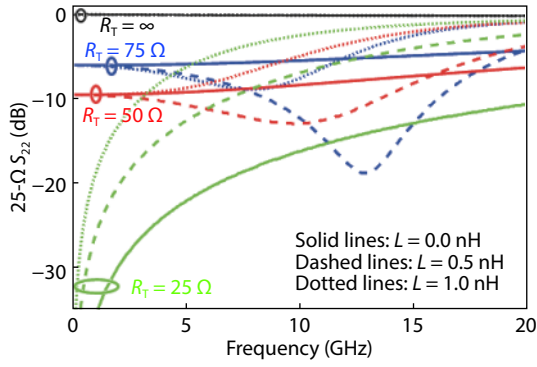


Fig. 6. (Color online) 25- $\Omega$   $S_{22}$  at different values of  $R_T$  and  $L$ . Line patterns: solid, dashed, and dotted represent the 25- $\Omega$   $S_{22}$  curves at  $L = 0$ , 0.5, and 1 nH, respectively. Line colors: black, blue, red, and green represent the 25- $\Omega$   $S_{22}$  curves when  $R_T = \infty$ , 75, 50, and 25  $\Omega$ , respectively. Simulation results are obtained when  $C_P = 0.2$  pF,  $C_D = 0.2$  pF, and  $R_D = 25$   $\Omega$ .

spectively. At  $L = 0$  nH,  $S_{22,max}$  at  $R_T = 25$   $\Omega$  is much lower than  $S_{22,max}$  at  $R_T = 50$  or 75  $\Omega$ . Whereas, when  $L = 0.5$  nH or 1.0 nH,  $S_{22,max}$  values at  $R_T = 50$  and 75  $\Omega$  are better than the values obtained at perfect matching ( $R_T = 25$   $\Omega$ ). These simulation results demonstrate that LDDs must employ output transmission line back-termination to absorb signal reflections from the laser side. A larger  $R_T$  values could be used to reduce the waste in  $I_M$ <sup>[8, 24]</sup>, especially when a good matching at the laser side is guaranteed. In the proposed design, a 50- $\Omega$  passive on-chip back termination resistor is utilized to balance between suppressing reflections and the loss in modulation current. It is worth mentioning that the TL is preferred to be as short as possible to reduce the insertion loss and propagation delay across it.

### 3.2. Driver circuit design

For any CML circuits in cascade, the single-ended output voltage swing is relatively small, less than  $V_{th}$  peak-to-peak<sup>[25]</sup>, to keep the transistors of the differential pairs in saturation, and consequently guarantee a high-speed operation. In the proposed circuit, the maximum single-ended output voltage of the output driver ( $V_o$ ) equals  $3 V_{pp}$  when the output current is 120 mA. Therefore, a series resistor ( $R_{Si}$ ) is utilized in the pre-driver stage as a level shifter that reduces the common-mode output voltage at  $V_{Pi}$  from  $(-I_{Pi}R_{Pi}/2)$  to  $(-I_{Pi}R_{Pi}/2 - I_{Pi}R_{Si})$ . Consequently, the output voltage swing of the output driver stage can be higher than  $V_{th}$ . An alternative solution to provide a high output voltage is to use level shifter stages, connecting between the pre-driver and the output driver<sup>[7, 13, 26]</sup>. Despite the buffering effect introduced by these stages, they significantly increase the power consumption of the driver circuit.

Focusing on slice I and considering the case at which the two slices are enabled to drive a 25- $\Omega$  load, the following formulas must be satisfied to keep  $(M_{1a}-M_{1b})$ ,  $(M_{2a}-M_{2b})$ , and the tail current sources  $I_{P1}$  and  $I_{T1}$  in saturation region:

$$V_{P1} + V_{i1}/2 < -I_{P1}R_{S1} - V_{i1,cm} + V_{th}, \quad (1)$$

$$V_o < I_{P1}R_{S1} + V_{th}, \quad (2)$$

$$V_{i1,cm} - V_{GS1} - V_{SS} > V_{knee,I_{P1}}, \quad (3)$$

$$-I_{P1}R_{S1} - V_{P1}/2 - V_{GS2} - V_{SS} > V_{knee,I_{T1}}, \quad (4)$$

where  $V_{i1}$ ,  $V_{i1,cm}$ ,  $V_{P1}$ , and  $V_o$  are the single-ended input voltage, the DC common-mode input voltage, the single-ended output voltage of the pre-driver, and the output driver, respectively.  $V_{knee,I_{P1}}$  and  $V_{knee,I_{T1}}$  are the minimum required voltage to maintain the cascode current mirrors in saturation.  $V_{GS1}$  and  $V_{GS2}$  are the required gate-source voltages to make  $I_{P1}$  and  $I_{T1}$  equally divided between  $(M_{1a}$  and  $M_{1b})$  and  $(M_{2a}$  and  $M_{2b})$ , respectively. The cascode current mirrors are sized such that  $V_{knee,I_{P1}}$  and  $V_{knee,I_{T1}}$  are less than 0.7 and 0.9 V, respectively. To operate near the maximum  $f_t$ ,  $V_{GS1}$  and  $V_{GS2}$  are assumed to be higher than or equal to 0.6 V, drain current density  $\geq 170$  mA/mm.

By substituting into Eq. (2) with the maximum possible  $V_o$ , which is  $3 V_{pp}$  when both slices are simultaneously enabled, and  $V_{th}$  of 0.3 V, we get that  $I_{P1}R_{S1}$  must be higher than 2.7 V. From Eq. (3),  $V_{i1,cm}$  must be 1.3 V above the  $V_{SS}$  level. If  $I_{P1}R_{S1}$ ,  $V_{i1,cm}$ , and  $V_{SS}$  are set to 2.8, -3.8, and -5.2 V, respectively,  $V_{P1} + V_{i1}/2$  must be less than 1.3 V, as derived from Eq. (1).  $V_{i1}$  at which complete current switching in both the pre-driver and the output driver stages is required to be as low as 300 mV<sub>pp</sub>, and thereby  $V_{P1}$  must be less than 1.15  $V_{pp}$ .

In order to achieve complete current switching in the output driver stage, a large input swing ( $V_{P1}$ ) and/or wide transistors ( $M_{2a}-M_{2b}$ ) are required. However, the circuit bandwidth is degraded as  $W_2$  increases due to the corresponding large input capacitance. On the other hand, increasing the output swing of the pre-driver ( $V_{P1}$ ), by increasing  $I_{P1}$  and/or  $R_{P1}$ , results in higher power dissipation and/or bandwidth degradation, respectively. Thus, the final choices of  $I_{P1}$ ,  $R_{P1}$ , and  $W_2$  are determined after a set of iterations to achieve complete switching at acceptable speed and power consumption.

The small-signal equivalent half-circuit of the proposed driver and a 25- $\Omega$  laser diode is shown in Fig. 7, when only slice I is enabled.  $C_{gs1}$ ,  $C_{gd1}$ , and  $C_{db1}$  are the gate-source, gate-drain, and drain-bulk capacitances of  $M_i$ .  $g_{mi}$  is the transconductance of  $M_i$ .  $R_i$  and  $C_i$  are the single-ended input resistance and capacitance of the pre-driver stage.  $R_{P1}$  and  $R_m$  are the resistive loads of the pre-driver and output driver, respectively.  $R_D$  and  $C_D$  represent the equivalent input resistance and the parasitic capacitance of the laser diode, and they account for 25  $\Omega$  and 0.5 pF, respectively. As the frequency response of the circuit is dominated by the output driver capacitances, the miller approximation capacitance of  $C_{gd1}$  is considered for simplicity, thereby  $C_1 = C_{gs1} + (1 + |A_{V,P}|)C_{gd1}$  and  $C_2 = C_{gs2} + C_{db1} + C_{gd1}$ , where  $A_{V,P}$  is the pre-driver voltage gain. The small-signal transfer function of the circuit can be expressed as;

$$\left| \frac{V_o}{V_{id}} \right| = \frac{g_{m1}g_{m2}R_{P1}R_o \left( 1 - S \frac{C_{gd2} - C_{F1}}{g_{m2}} \right)}{\left( 1 + S \frac{R_i C_1}{2} \right) (aS^2 + bS + 1)}, \quad (5)$$

where

$$a = R_{P1}R_o [C_2 (C_{gd2} + C_{F1}) + C_o (C_2 + C_{gd2} + C_{F1}) + 4C_{gd2}C_{F1}], \quad (6)$$

$$b = R_{P1} (C_2 + C_{gd2} + C_{F1}) + R_o (C_o + C_{gd2} + C_{F1}) + g_{m2}R_{P1}R_o (C_{gd2} - C_{F1}). \quad (7)$$

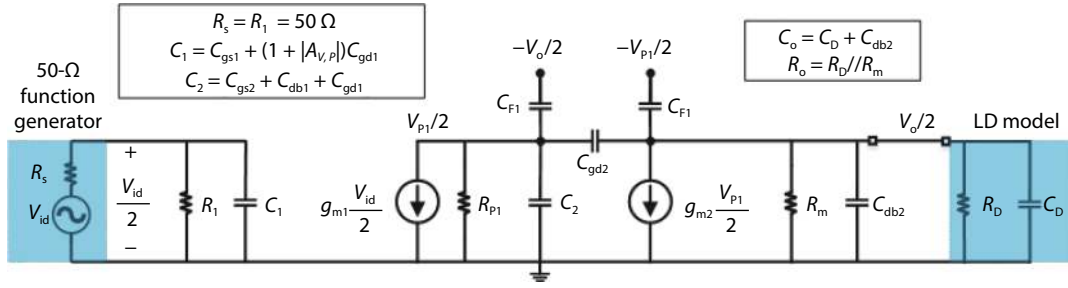


Fig. 7. The small-signal equivalent half-circuit for the proposed driver when only slice I is enabled.

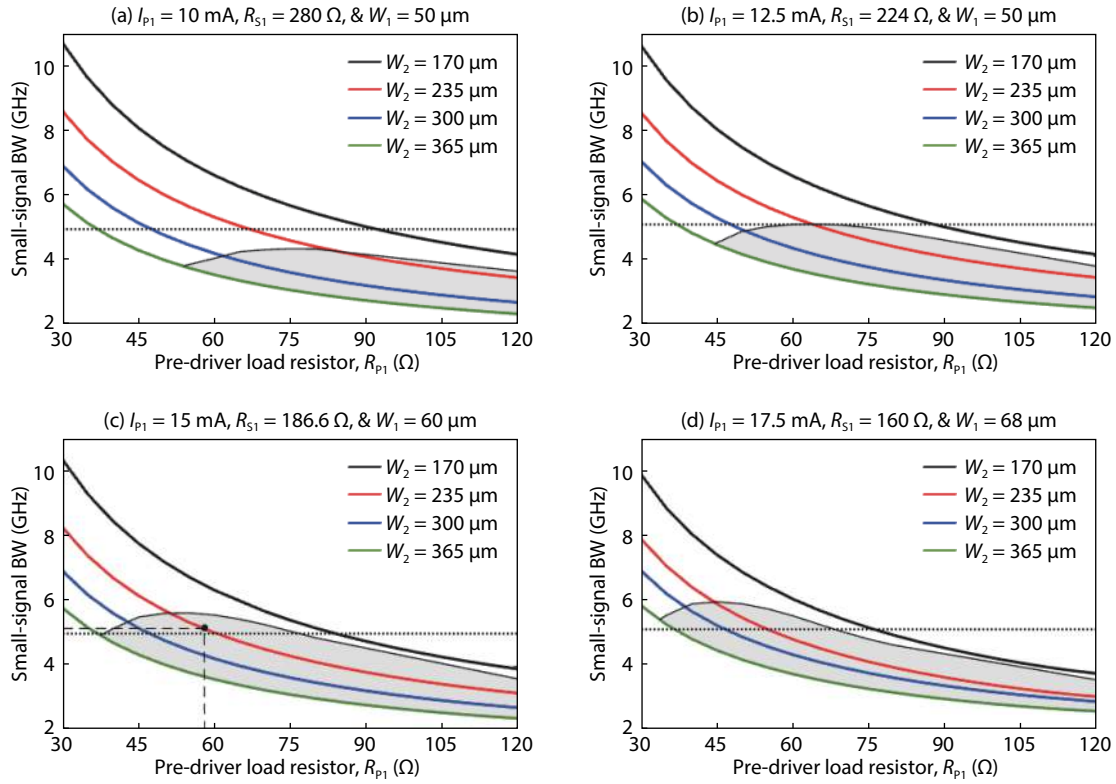


Fig. 8. Small-signal bandwidth dependence on  $R_{p1}$  and  $W_2$  at different  $I_{p1}$ . Shaded areas represent the accepted values of  $R_{p1}$  and  $W_2$  at which  $V_o$  exceeds  $1.96 V_{pp}$ .

$R_o$  and  $C_o$  represent the parallel combination of ( $R_m$  and  $R_D$ ) and ( $C_D$  and  $C_{db2}$ ), respectively. For  $b^2 \gg 4a$ , which is generally achieved for small values of  $C_{F1}$ , the transfer function shows an overdamped behavior with three real left half-plane (LHP) poles;

$$|P_1| = \frac{1}{\pi R_1 C_1}, \quad (8)$$

$$|P_2| \approx \frac{1}{2\pi R_{p1} [C_2 + C_{gd2} (1 + g_{m2} R_o) - C_{F1} (g_{m2} R_o - 1)]}, \quad (9)$$

$$|P_3| \approx \frac{C_2 + C_{gd2} (1 + g_{m2} R_o) - C_{F1} (g_{m2} R_o - 1)}{2\pi R_o C_2 C_o}. \quad (10)$$

The numerator of Eq. (5) shows only one zero located at  $g_{m2}/2\pi (C_{gd2} - C_{F1})$ , which is substantially larger than the system poles. Generally,  $W_2$  is larger than  $W_1$ , and therefore  $|P_2| \ll |P_1|$ . Moreover, at  $C_{F1} = 0$ ,  $|P_2|$  is much lower than  $|P_3|$ , and the small-signal bandwidth (BW) approximately equals

$|P_2|$ . Initially,  $C_{F1}$  is assumed to be zero, and the values of  $I_{p1}$ ,  $R_{p1}$ , and  $W_2$  are chosen such that the small-signal BW is higher than 5 GHz, while complete current switching is achieved. Then, the BW will be boosted by adjusting  $C_{F1}$ . Fig. 8 shows the BW dependence on  $R_{p1}$  and  $W_2$  at different  $I_{p1}$ . The size of the pre-driver differential pair ( $W_1$ ) is chosen to guarantee complete switching of  $I_{p1}$  corresponding to the 300 mV<sub>pp</sub> single-ended input signal. The value of  $R_{S1}$  is adjusted such that the voltage drop across it is about 2.8 V, as derived from Eq. (2). The shaded areas in Fig. 8 represent the accepted values of  $R_{p1}$  and  $W_2$  at which the output voltage of the output driver ( $V_o$ ) exceeds  $1.96 V_{pp}$  (98% of  $I_{T1}$  passes through the ON transistor) when the input voltage equals 300 mV<sub>pp</sub> (single-ended). At  $I_{p1} = 15$  mA, the highest BW in the shaded area, where  $V_o > 1.96 V_{pp}$ , exceeds 5 GHz (about 5.6 GHz), and this occurs at  $W_2 = 235 \mu\text{m}$  and  $R_{p1} = 52.2 \Omega$ . The parameters  $I_{p1}$ ,  $R_{p1}$ , and  $W_2$  are chosen to be 15 mA, 58  $\Omega$  (a little bit higher than 52.2  $\Omega$  to ensure that  $V_o > 1.96 V_{pp}$  at different processes and temperature corners), and 235  $\mu\text{m}$ , respectively, as shown in Fig. 8(c). At this point,  $V_{p1}$  and  $V_o$  equal 0.87 and 2  $V_{pp}$ , respect-

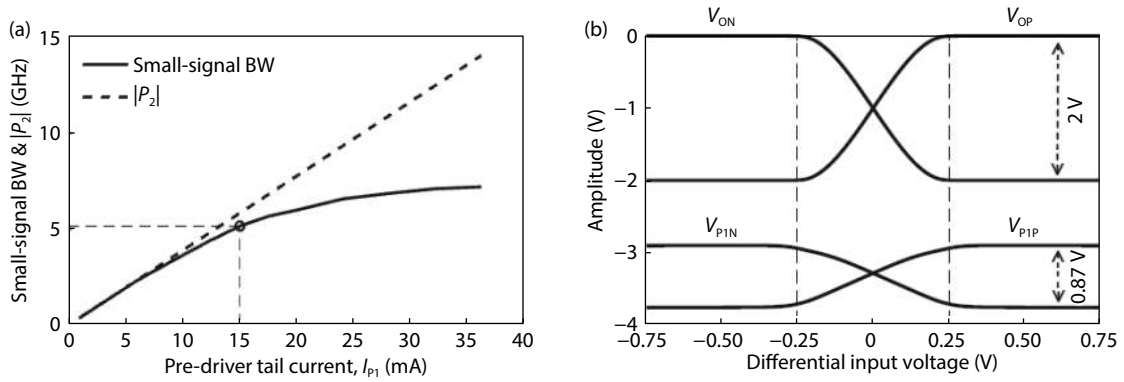


Fig. 9. (a) Small-signal BW and  $|P_2|$  dependence on  $I_{P1}$ , where  $V_{P1}$  is maintained constant at  $0.87 V_{pp}$ . (b) DC transfer characteristics of the pre-driver and output driver.

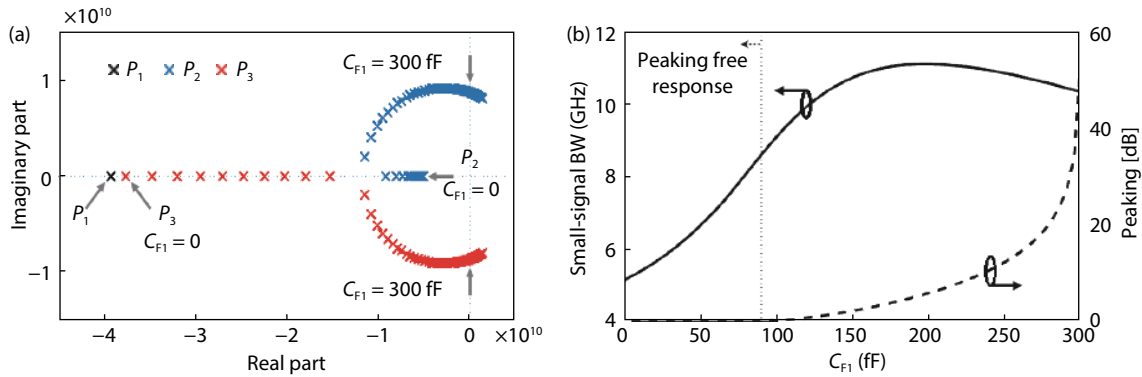


Fig. 10. (Color online) (a) Poles locus as  $C_{F1}$  varied from 0 to 350 fF. (b) Small-signal BW and peaking dependence on  $C_{F1}$ .

ively, and the small-signal BW is about 5.16 GHz.

Fig. 9(a) illustrates the dependence of BW and  $|P_2|$  on  $I_{P1}$ , where  $V_{P1}$  is maintained constant at  $0.87 V_{pp}$  ( $R_{P1} = 0.87/I_{P1}$ ) and  $W_1$  is chosen to achieve complete switching of  $I_{P1}$  through ( $M_{1a}$ – $M_{1b}$ ). At lower values of  $I_{P1}$ ,  $W_1$  is much lower than  $W_2$ , and consequently, the BW is dominated by  $|P_2|$ . However, as  $I_{P1}$  increases,  $W_1$  and thereby  $C_1$  increase accordingly. In this case, the pole introduced at the input of the pre-driver ( $P_1$ ) can no longer be ignored as it significantly degrades the circuit BW. So, at higher  $I_{P1}$  values, a little improvement in the BW is achieved on the cost of higher power dissipation and area for the pre-driver circuit.

The dc transfer characteristic curves that show the voltage variations of the pre-driver and output driver output nodes in terms of the fully differential input voltage are shown in Fig. 9(b). It is clear that complete current switching, in the output driver stage, occurs at a differential input voltage of about  $500 mV_{ppd}$  ( $250 mV_{pp}$  single-ended).

In the proposed design, the input capacitance effect of the output driver is reduced by using cross-coupled neutralization capacitors. The impact of these capacitors on the poles locus is illustrated in Fig. 10(a), where  $C_{F1}$  is varied from 0 to 350 fF. The first pole ( $P_1$ ) is not altered by changing  $C_{F1}$  as given in Eq. (8). As  $C_{F1}$  increases, the dominant pole ( $P_2$ ) moves away from the origin, resulting in a higher bandwidth. Meanwhile  $P_3$  moves towards the origin until reaching the break-out point, and then the two poles split out, producing an underdamped response. If  $C_{F1}$  is further increased above 300 fF,  $P_2$  and  $P_3$  become positive, and an unstable system is ob-

tained. Fig. 10(b) shows the small-signal BW and the peaking in the magnitude response dependences on  $C_{F1}$ . For peaking-free frequency response,  $C_{F1}$  must be below 90 fF. Fig. 11 shows the magnitude and group delay (GD) responses of slice I at different  $C_{F1}$  values. The highest BW, without peaking, and the optimum GD response occurred exactly at  $C_{F1} = 90$  fF. However, the chosen value of  $C_{F1}$  must be below this bound to avoid any peaking in the magnitude response and large variances in GD when bonding wire inductance is accounted. In this design, a  $C_{F1}$  value of 65 fF satisfies this condition. At this point,  $C_{F1}$  equals approximately 126 % of  $C_{gd2}$ , and the input capacitance of the main driver is reduced by about 30%. Consequently, the small-signal BW of slice I is increased by 42.8% to reach 7.3 GHz.

Actually, the small-signal transfer function will be impacted in the existence of bonding wire inductance ( $L$ ), which connects between the driver output and the LD. In this case, the system order is raised to five, and hence two additional complex conjugate poles are introduced. Fig. 12 shows the poles locus and the small-signal BW dependence on  $L$ , when  $C_{F1} = 65$  fF and  $L$  is swept from 0.1 to 3 nH. Whereas, the magnitude and group delay responses at different values of  $L$  is illustrated in Fig. 13. However, the dominant pole ( $P_2$ ) moves towards origin as  $L$  increases, the BW slightly increases, as  $L$  varies from 0 to 0.5 nH, due to the high-quality factor of the complex conjugate poles ( $P_4$  and  $P_5$ ) which introduces a peaking at their undamped natural frequency. If  $L$  is further increased above 0.5 nH, the BW decreases as the quality factor of ( $P_4$  and  $P_5$ ) decreases such that it is no longer able to com-

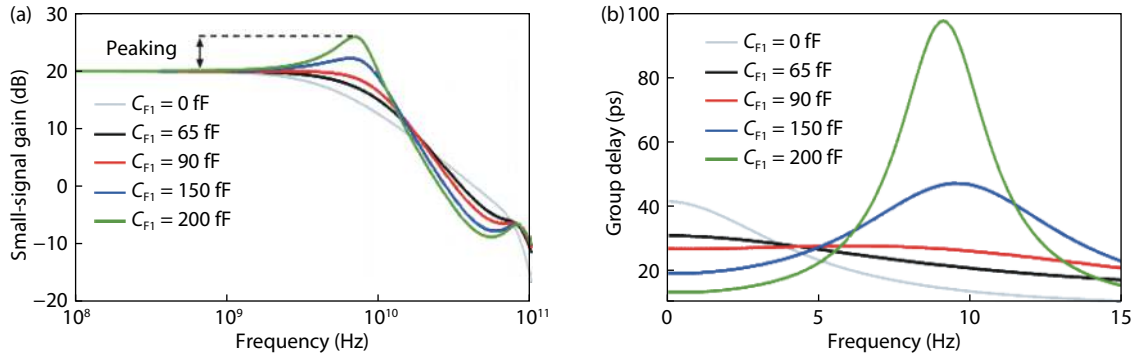


Fig. 11. (Color online) Slice I small-signal frequency response at different values of  $C_{F1}$ . (a) Magnitude response. (b) Group delay response.

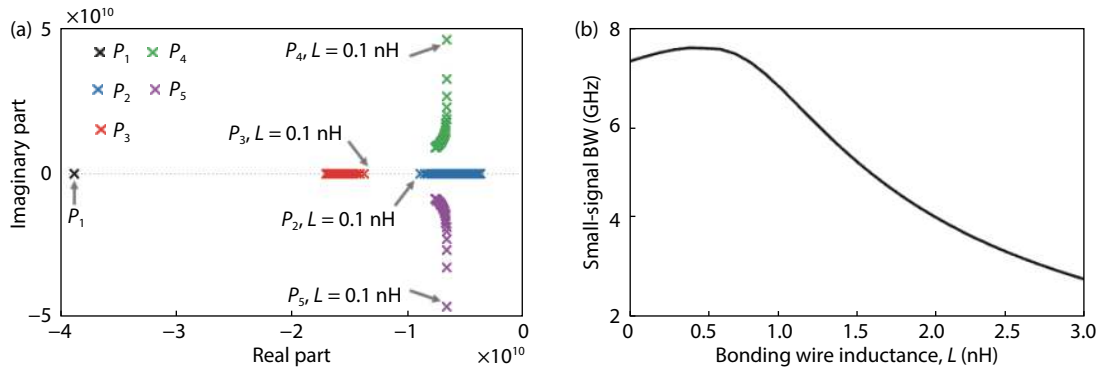


Fig. 12. (Color online) (a) Poles locus when  $C_{F1} = 65$  fF and  $L$  is swept from 0.1 to 3 nH. (b) small-signal BW dependence on  $L$ .

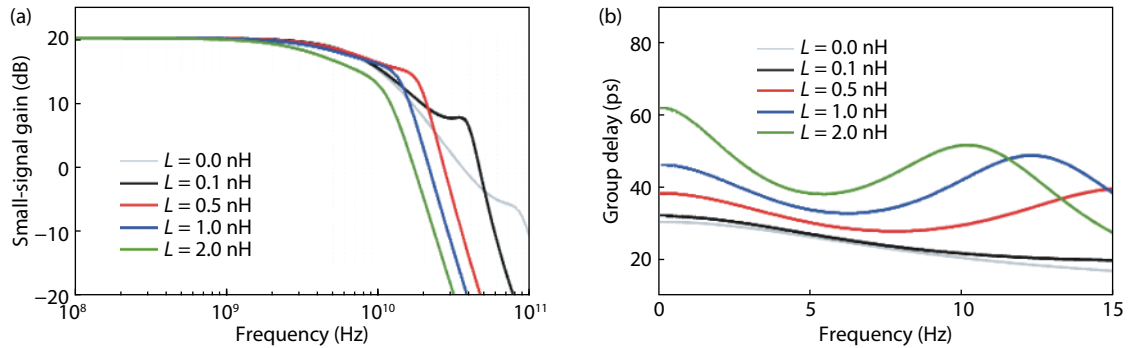


Fig. 13. (Color online) Slice I small-signal frequency response at different values of  $L$  for  $C_{F1} = 65$  fF. (a) Magnitude response. (b) Group delay response.

compensate for the decrease in  $P_2$ , and thereby the BW is dominated by  $|P_2|$ . Also, group delay variances across the frequency domain are observed when  $L > 0.5$  nH. Therefore, the bonding wiring inductance must be as small as possible to avoid the previous effects.

Fig. 14 shows the simulated 15 Gbps single-ended output eye diagrams at different  $L$  values. The input pattern is  $2^7-1$  pseudorandom bit sequence (PRBS) with a single-ended amplitude of  $300$  mV<sub>pp</sub>. A well-behaved time response, without ringing, overshoots, or undershoots, is observed for  $L < 1$  nH. The rise/fall times (20%–80%) at  $L = 0$  nH equal 22/19.8 ps. At higher  $L$  values, the driver BW dramatically decreases, leading to higher rise/fall times and severe inter-symbol interference (ISI) as shown in Fig. 14(d).

The second slice is designed using the same previous pro-

cedure. With  $I_{P2}$ ,  $R_{P2}$ ,  $R_{S2}$ ,  $W_3$ ,  $W_4$ , and  $C_{F2}$  of 12 mA, 68.75  $\Omega$ , 233  $\Omega$ , 55  $\mu\text{m}$ , 120  $\mu\text{m}$ , and 30 fF, respectively, the small-signal bandwidth is about 8 GHz and the rise/fall times equal 16.5/15 ps.

#### 4. Post-layout simulations

Large signal  $S$ -parameters characterization of the driver is performed at an input signal level of  $0.6$  V<sub>ppd</sub> ( $0.3$  V<sub>pp</sub> single-ended), and the results are presented in Fig. 15(a). The forward-path gain ( $S_{21}$ ) curves demonstrate that the large signal bandwidth of slice I and slice II are 10 and 11.15 GHz, respectively. The input return loss is better than 10 dB up to 20 GHz for both slices. The output return loss is better than 10 dB up to 13.2 GHz. It is worth mentioning that both slices are required to produce similar group delay responses in the band

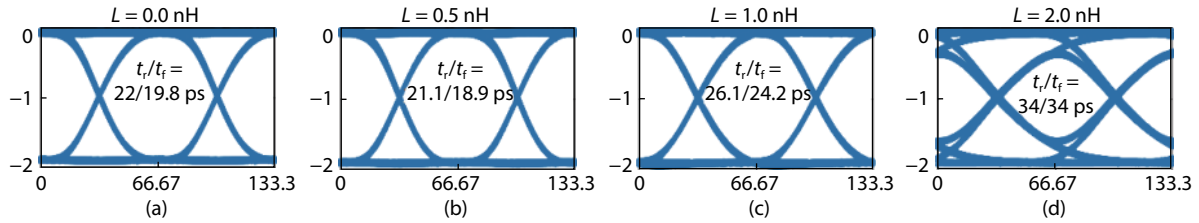


Fig. 14. (Color online) Simulated 15 Gbps single-ended output eye diagram, when only slice I is enabled, at (a)  $L = 0$  nH, (b)  $L = 0.5$  nH, (c)  $L = 1.0$  nH, (d)  $L = 2.0$  nH. Horizontal: time in ps, vertical: amplitude in V.

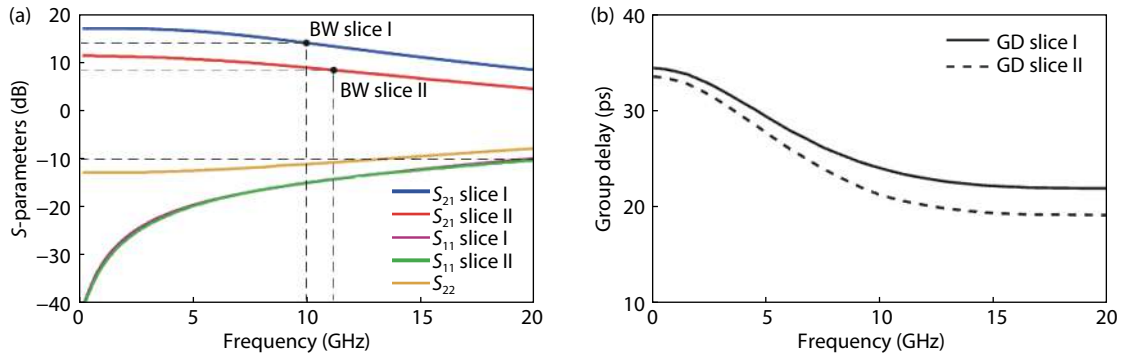


Fig. 15. (Color online)  $S$ -parameters simulation results. (a) Gain and return loss. (b) Group delay.  $S$ -parameters characterization is performed using a 100- $\Omega$  input port (fully differential), and a 25- $\Omega$  output port that is connected to one output terminal of the driver. Whereas, the other output terminal is connected to a 25- $\Omega$  dummy resistor.

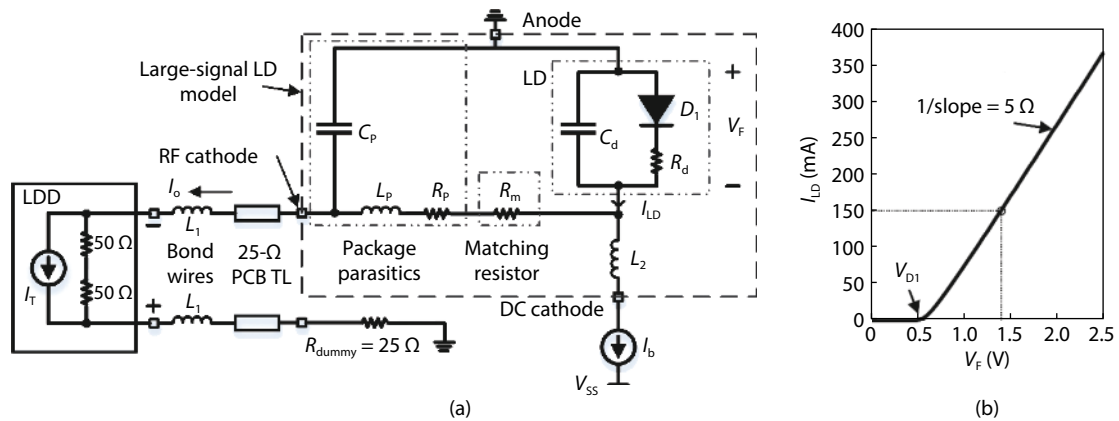


Fig. 16. (a) Large signal model of a DFB LD and its interface with the LDD chip. The LD parasitics  $R_d$  and  $C_d$  are accounted for 5  $\Omega$  and 4 pF, respectively. The package parasitics are assumed as  $R_p = 1$ - $\Omega$ ,  $L_p = 0.15$  nH, and  $C_p = 0.5$  pF.  $R_m$  and  $L_1$  equal 20- $\Omega$  and 0.4 nH, respectively. (b)  $I$ - $V$  characteristic curve of the LD showing that  $R_d = 5$   $\Omega$ ,  $V_{D1} = 0.51$  V, and  $V_F = 1.4$  V at  $I_{LD} = 150$  mA.

of interest to avoid distortions in the output PAM4 signal. Fig. 15(b) shows the simulated group delay of both slices. The low-frequency group delay is about 34.5 and 33.7 ps for the MSB (slice I) and LSB (slice II) paths, respectively, and the peak difference is only 2.8 ps at 20 GHz.

The time-domain analysis was also performed to demonstrate the large-signal capability of the proposed driver. In this analysis, a large signal model of the laser diode, shown in Fig. 16(a), is utilized. The model consists of a forward-biased PN junction diode ( $D_1$ ) with its own parasitics ( $R_d$  and  $C_d$ ), and the package parasitic elements,  $R_p$ ,  $C_p$ , and  $L_p$ [27, 28]. As most DFB lasers have a series resistance ( $R_d$ ) of approximately 5- $\Omega$ , a series matching resistor ( $R_m$ ) of 20- $\Omega$  is included in the laser package to provide a total input impedance of 25- $\Omega$ [24, 29].

The laser diode threshold current ( $I_{th}$ ) and the forward voltage ( $V_F$ ) are assumed to be 10 mA and 1.4 V at 150 mA forward current, respectively. The  $I$ - $V$  characteristic curve of  $D_1$ , given in Fig. 16(b), shows that  $R_s = 5$   $\Omega$ ,  $D_1$  forward voltage ( $V_{D1}$ ) is about 0.51 V at 1 mA forward current, and  $V_F = 1.4$  V at 150 mA forward current, which matches the assumed laser diode characteristics. The laser diodes are often biased above  $I_{th}$  to improve their speed[24], and thereby  $D_1$  is DC biased with  $I_b = 25$  mA. The RF cathode terminal of the LD model is DC-coupled to the inverting output terminal of the LDD chip through a bonding wire inductance ( $L_1$ ) and a 25- $\Omega$  microstrip PCB TL, while the non-inverting terminal is loaded with a 25- $\Omega$  dummy resistor. The length of the TL is 5 mm, and it is designed using Rogers PCB which has  $\epsilon_r = 3.48$ .



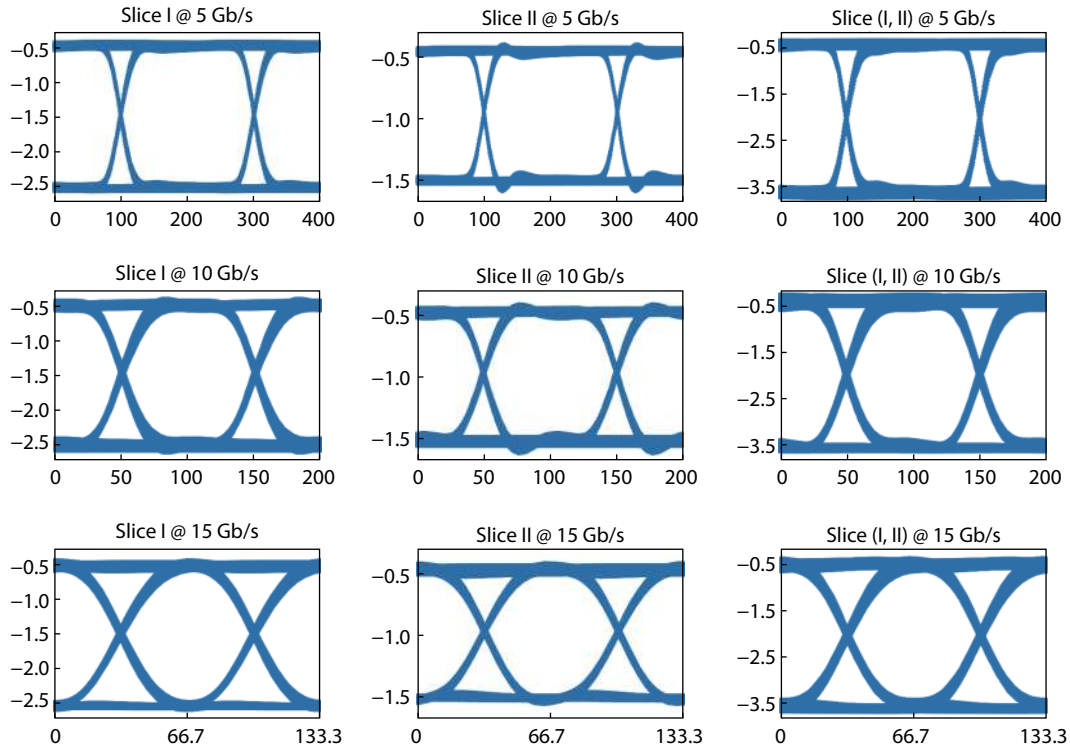


Fig. 17. (Color online) Simulated single-ended output eye diagrams for slice I, slice II, and both slices at different data rates. (Horizontal: time in ps, vertical: amplitude in V).

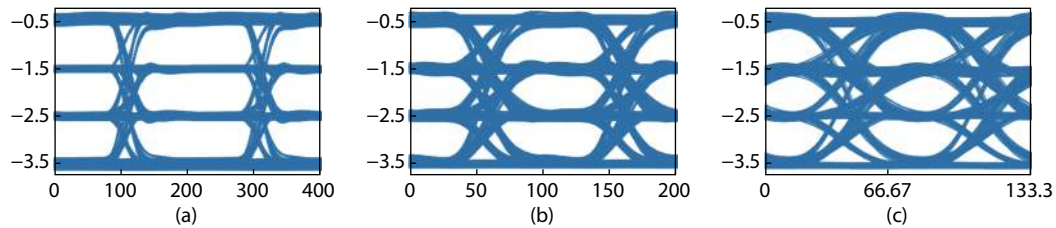


Fig. 18. (Color online) Simulated output PAM4 eye diagrams at (a) 10 Gbps (5 Gbaud/s), (b) 20 Gbps (10 Gbaud/s), (c) 30 Gbps (15 Gbaud/s). Horizontal: time in ps, vertical: amplitude in V.

The input pattern is a PRBS-7 signal with a single-ended amplitude of 300 mV<sub>pp</sub>. The simulated single-ended output eye diagrams at the RF cathode terminal of the LD model are illustrated in Fig. 17. The eye diagrams are obtained at different data rates when either slice is enabled or both slices are simultaneously enabled and driven by identical input patterns. Clear output eye diagrams are obtained at speeds up to 15 Gbps. The amplitude of the output eye diagram and the corresponding output current amplitude are (2 V and 80 mA) for slice I, (1 V and 40 mA) for slice II, and (3 V and 120 mA) for both slices, respectively. The rise/fall times at 15 Gbps for slice I and II are 24.2/23.3 ps and 19.3/18.5 ps, respectively.

If a simple resistive load was used, the high-level of the output eye diagrams, which occurs at zero output current, would be zero. However, when interfacing the proposed LDD, which has a 50-Ω single-ended output back termination, with the forward-biased LD model given in Fig. 16, the high-level values are shifted down to approximately -0.5 V, as shown in Fig. 17. Also, the low-level values are shifted down by the same amount. The proposed driver offers a suffi-

cient output voltage compliance range that allows DC-coupling to 25-Ω lasers with output current up to 120 mA. With  $V_{ss} = -5.2$  V, simulation results reveal that the minimum voltage needed at the output of the driver for proper operation, achieving fast complete current switching, is about -3.65 V. Therefore, the allowable headroom for the laser and its matching resistor equals 3.65 V when the laser anode terminal is grounded. If the laser anode terminal is powered from a positive supply voltage ( $V_{DD}$ ), the output headroom will increase to  $V_{DD} + 3.65$  V, at the cost of increasing the power dissipation.

Fig. 18 shows the output eye diagrams when the driver is used as a PAM4 transmitter at different data rates. A PRBS-7 pattern is applied to slice I while slice II is supplied with a one-bit delayed replica of the same pattern. Clear PAM4 eye diagrams are obtained at speeds up to 30 Gbps (15 Gbaud/s). The output voltage levels are -0.5, -1.5, -2.5, and -3.5 V, and consequently the peak-to-peak output voltage and current are 3 V and 120 mA, respectively.

The design reliability is verified by checking the circuit performance at different process corners, supply voltage ( $\pm 10\%$ ),

Table 1. Proposed driver performance at 15 Gbps when operated at different PVT corners.

Parameter	Slice I	Slice II
Eye height (V)	1.49–1.85	0.75–0.91
Eye width (UI)	0.82–0.9	0.84–0.91
Rise time (ps)	21.4–31	16.8–29.7
Fall time (ps)	19.7–30.5	16–29.1
Total jitter (UI pk-pk)	0.12–0.225	0.1–0.21

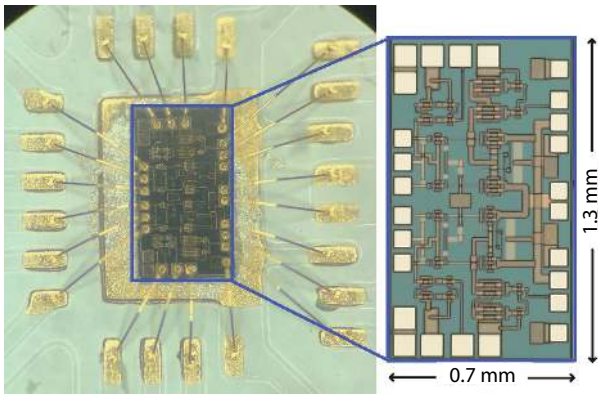


Fig. 19. (Color online) Photograph of the laser driver chip after wire bonding on a custom-designed PCB.

and temperatures (from  $-40$  to  $125$  °C), (PVT analysis). The output eye diagram features, for slice I and slice II, at 15 Gbps are summarized in Table 1. The results demonstrate that the eye diagram features are almost acceptable.

## 5. Experimental results

The proposed driver is fabricated in a  $0.15\text{-}\mu\text{m}$  GaAs E-mode pHEMT process. The chip occupies a total area of  $0.7 \times 1.3$  mm<sup>2</sup>. The die photograph and its corresponding bonding wire to a custom-designed Rogers PCB ( $\epsilon_r = 3.48$ ) are shown in Fig. 19. Two pads are assigned for each output terminal of the driver to reduce the bonding wire inductance. Gold bonding wires with a  $25.4$   $\mu\text{m}$  diameter were used, and the output bonding wires' lengths are less than  $0.8$  mm. Using the rule of thumb of  $1$  nH/mm, the estimated output bonding wire inductance will be less than  $0.4$  nH. With this low bonding wire inductance, the circuit performance will not be substantially affected, as discussed in Section 3.2.

Low-dropout (LDO) regulators are used to generate the required supply voltage and biasing to the chip. The ground bounce noise caused by supply bonding wires is suppressed by using localized decoupling networks, consisting of ferrite beads and ceramic capacitors. These components are mounted near the chip on the bottom side of the evaluation board. Both of the input connectors and the output load are placed as near as possible to the chip to reduce the traces' lengths. The input signals are AC coupled to the chip using  $0.1$   $\mu\text{F}$  coupling capacitors. Each output terminal of the driver is DC coupled to a  $25\text{-}\Omega$  resistive load that is formed of two parallel-connected high-frequency  $50\text{-}\Omega$  resistors. The input traces are designed as  $100\text{-}\Omega$  differential transmission lines, while the output traces are considered as short interconnects due to the difficulty of designing  $25\text{-}\Omega$  PCB transmission lines. The electrical length of the input and output traces are  $18.7$  and  $3.5$  mm, respectively.

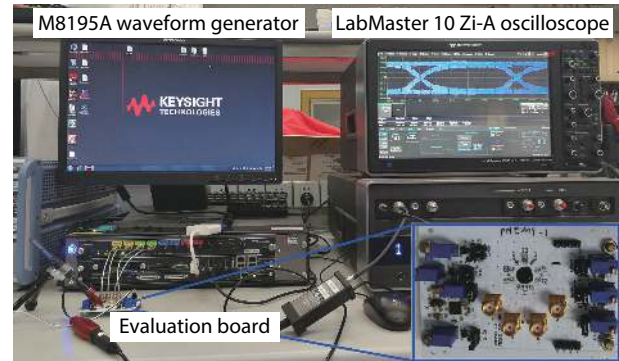


Fig. 20. (Color online) Experimental setup for eye diagram measurements.

Fig. 20 shows the measurement setup of the proposed driver. The input pattern is a PRBS-31 with a single-ended amplitude of  $300$  mV<sub>pp</sub> (at the chip inputs), generated from a Keysight M8195A arbitrary waveform generator. The LabMaster 10 Zi-A high-speed oscilloscope, along with its active probe, is used to measure the eye diagram of the output signal.

Fig. 21 shows the measured single-ended output eye diagrams at different data rates when either slice is enabled or both slices are simultaneously enabled and driven by identical input patterns. Clear open eyes are obtained up to  $15$  Gbps. The rise/fall times (20%–80%) at  $15$  Gbps are below  $25$  and  $20$  ps for slice I and slice II, respectively. The eye amplitude equals approximately  $2$  V for slice I and  $1$  V for slice II at different data rates. Hence, it could be deduced that the output modulation current is  $80$  and  $40$  mA, respectively. When both slices are enabled and driven with the same input pattern, the output current reaches  $120$  mA with an output eye amplitude of about  $3$  V.

At  $15$  Gbps, the eye width and height are  $0.531$  UI and  $1.4$  V for slice I, and  $0.518$  UI and  $0.68$  V for slice II. The random jitter ( $R_{j,RMS}$ ) and the deterministic jitter ( $D_j$ ) is about ( $0.014$  and  $0.376$  UI) for slice I and ( $0.015$  and  $0.388$  UI) for slice II. Consequently, the measured total jitter at a bit error rate of  $10^{-12}$  ( $T_j @ BER = 10^{-12}$ ) equals  $0.577$  and  $0.598$  UI for slice I and slice II, respectively. When both slices are simultaneously enabled,  $R_{j,RMS}$ ,  $D_j$ , and  $T_j$  are  $0.012$ ,  $0.354$ , and  $0.526$  UI, respectively. Meanwhile, the eye width and height are  $0.533$  UI and  $2$  V. Most of the jitter observed in the measurement results arises from the pattern generator, cables, connectors, PCB TMs, and oscilloscope. The fully differential input eye diagram, measured at the output terminals of the coupling capacitors, shows high jitter levels ( $R_{j,RMS} = 0.03$  UI,  $D_j = 0.297$  UI, and  $T_j = 0.717$  UI @  $BER = 10^{-12}$ ) as depicted in Fig. 22. Consequently, this input jitter severely degrades the output jitter performance of the driver at  $15$  Gbps.

Fig. 23 shows the output eye diagrams of the proposed driver when it is tested as a PAM4 transmitter at different data rates. In this test, the two slices are activated and a PRBS-31 pattern is applied to slice I (MSB path) while slice II (LSB path) is supplied with a one-bit delayed replica of the same pattern. The results demonstrate that the PAM4 eye diagrams still keep open and clear up to  $30$  Gbps ( $15$  Gbaud/s) with a peak-to-peak amplitude of about  $3$  V (single-ended).

Table 2 summarizes the performance of the proposed driver, along with that of prior works. In our design, the modulation current is as high as  $120$  mA, with a power consump-

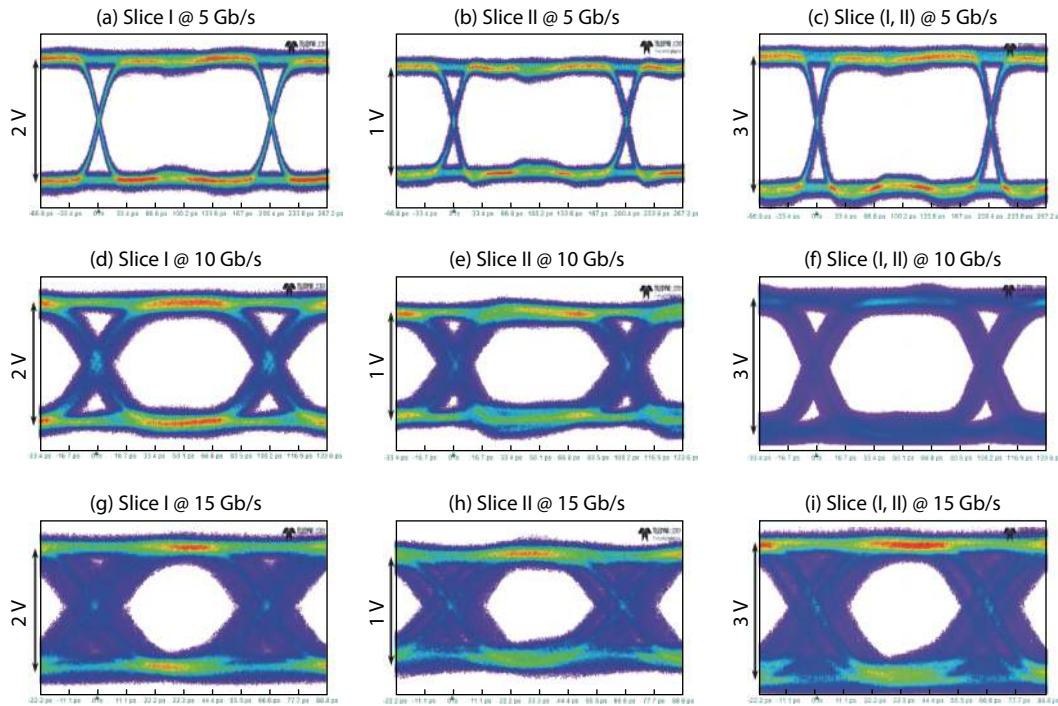


Fig. 21. (Color online) Measured output eye diagrams for slice I, slice II, and both slices at 5, 10, and 15 Gbps. Horizontal scale: 33.4 ps/div for (a, b, and c), 16.7 ps/div for (d, e, and f), and 11.1 ps/div for (g, h, and i).

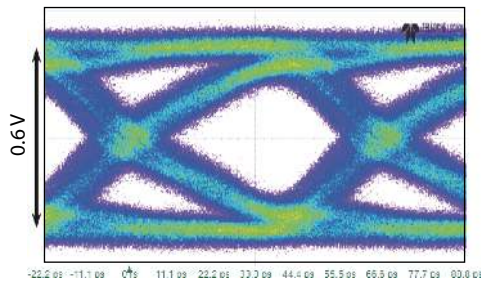


Fig. 22. Fully measured differential input eye diagram at 15 Gbps. Horizontal scale: 11.1 ps/div.

tion of 1.228 W from a single  $-5.2$  V supply. The proposed driver has a better  $FOM_1$  than prior works that operate at nearby speeds. It also shows a high output power to power dissipation ratio that is defined using  $FOM_2$ . Ref. [4] has a slightly higher FOMs than the reported driver as it employs AC coupling to interface the output load, which helps to reduce the supply voltage, and hence the power consumption is also reduced. However, the AC coupling technique requires discrete off-chip coupling components, which causes signal distortion at high speeds and significantly degrades the driver gain at low frequencies<sup>[19]</sup>. Ref. [11] also shows a higher  $FOM_1$  than the proposed driver in NRZ mode. The reason is that Ref. [11] adopts the ABT technique which reduces the power dissipation on the expense of higher area. Also, the driver circuit in Ref. [11] is powered from three different supply voltages (1.2, 1.5, and 3.3 V), compared to a single supply in the reported driver. The reported modulation currents of the PAM4 driver in Ref. [21] and the NRZ driver in Ref. [30] are as low as 6.4 and 6.6 mA, respectively, making them only suitable for low current VCSEL diodes. As the modulation current decreases, the output voltage swing decreases, and consequently a lower supply voltage could be used. Therefore,

the power consumption is significantly reduced as both of the total current and supply voltage are reduced, leading to a higher  $FOM_1$ . Moreover, smaller output transistors can be used, leading to higher speed operation. Therefore, it is unfair to directly compare  $FOM_1$  of driver circuits with widely separated modulation currents. Nevertheless, the proposed NRZ/PAM4 driver has the highest modulation current with a better output power to power dissipation ratio ( $FOM_2$ ), and it is still showing a comparable  $FOM_1$  with these low current drivers. These results demonstrate the potential of the implemented driver to drive high current DFB lasers.

## 6. Conclusion

In this paper, the performance of a  $0.15\text{-}\mu\text{m}$  GaAs pHEMT laser driver IC has been demonstrated. The driver supports both NRZ and PAM4 modulation schemes. A detailed design procedure was presented to optimize the driver circuit to achieve complete current switching at acceptable speed and power dissipation with a well-behaved transient response. The IC provides clear output eye diagrams at speeds up to 15 Gbps with NRZ and 30 Gbps (15 Gbaud/s) with PAM4 when driving  $25\text{-}\Omega$  loads. The reported driver demonstrates a high current driving capability along with better output power to power dissipation ratio, which makes it a good choice in driving high current DFB lasers.

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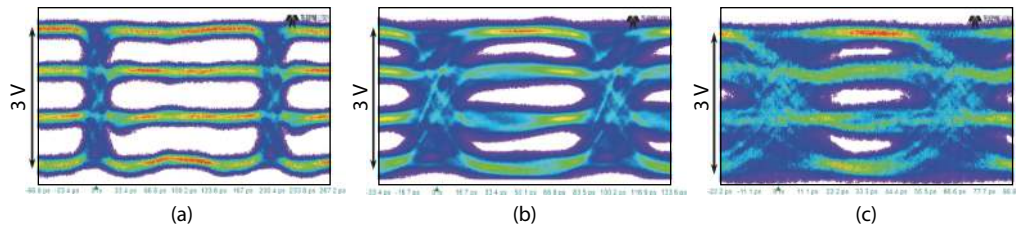


Fig. 23. (Color online) Measured PAM4 output eye diagram at (a) 10 Gbps (5 Gbaud/s), (b) 20 Gbps (10 Gbaud/s), (c) 30 Gbps (15 Gbaud/s). Horizontal scale: 33.4, 16.7, and 11.1 ps/div for (a), (b), and (c), respectively.

Table 2. Performance summary and comparison to prior work.

Parameter	This work		Ref. [9]	Ref. [4]	Ref. [7]	Ref. [2]	Ref. [10]	Ref. [21]	Ref. [11]		Ref. [30]
Modulation format	NRZ	PAM4	NRZ	NRZ	NRZ	NRZ	NRZ	PAM4	NRZ	PAM4	NRZ
Data rate (Gbps)	15	30	10	10	24	10.7	4.25	56	32	30	42
Termination	Passive	Passive	Active	Passive	passive	Active	Active	Passive	Active	Active	Passive
Output coupling	DC	DC	DC	AC	DC	AC	DC	DC	DC	DC	DC
Input swing ( $V_{pp}$ ) (single-ended)	0.3	0.3	0.4	0.4	0.5	N/A	0.2	0.15	0.15	0.15	N/A
Modulation current (mA)	120	120	100	100	56 <sup>b</sup>	80	80	6.4 <sup>b</sup>	44 <sup>d</sup>	32 <sup>d</sup>	6.6 <sup>e</sup>
Supply voltage (V)	-5.2	-5.2	-5.2	1.8/2	-4.5	3.3	3.3	2.3/3	1.2/1.5/3.3	1.2/1.5/3.3	N/A
Power (W)	1.228	1.228	1.3	0.675	1.8	0.67	0.343 <sup>c</sup>	0.115	0.55	0.55	0.0815
Output return loss (dB)	<10 dB up to 13.2 GHz <sup>a</sup>	<10 dB up to 13.2 GHz <sup>a</sup>	<10 dB up to 12 GHz	N/A	N/A	<10 dB up to 10 GHz	N/A	<8 dB up to 30 GHz	N/A	N/A	N/A
FOM <sub>1</sub> (A-Gbps/W)	1.47	2.93	0.77	1.48	0.75	1.28	0.74	3.1	2.56	1.75	3.4
FOM <sub>2</sub>	14.7%	11.4%	9.6%	18.5%	4.4%	11.9%	13.1%	0.7%	1.76%	0.73%	2.7%
Die area (mm <sup>2</sup> )	0.91	0.91	N/A	1.62	1	2.25	2.66	0.59	1.2	1.2	0.5
Technology	0.15 $\mu$ m GaAs E-mode pHEMT	0.15 $\mu$ m GaAs E-mode pHEMT	0.25 $\mu$ m GaAs pHEMT	0.18 $\mu$ m CMOS	0.2 $\mu$ m GaAs pHEMT	SiGe SOI Bipolar	SiGe BiCMOS	SiGe BiCMOS	65 nm CMOS	65 nm CMOS	14 nm Bulk CMOS

FOM<sub>1</sub> is defined as the product of the modulation current and data rate divided by the power dissipation, without DC bias current of load devices. The higher, the better.

FOM<sub>2</sub> is the output power divided by the total power dissipation, without DC bias current of load devices. The higher the better.

<sup>a</sup> Based on post-layout simulation results.

<sup>b</sup> The modulation current is deduced from the measured eye diagram at 50- $\Omega$  output load.

<sup>c</sup> Power and FOMs are given at 60 mA modulation current.

<sup>d</sup> The modulation current is deduced from the measured eye diagram at 10- $\Omega$  equivalent output load.

<sup>e</sup> Modulation current at 100- $\Omega$  load.

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