ARTICLES

Journal of Semiconductors
(2021) 42, 062803
doi: 10.1088/1674-4926/42/6/062803
JOS

A 3.3 kV 4H-SiC split gate MOSFET with a central implant region for superior trade-off between static and switching performance

Jongwoon Yoon and Kwangsoo Kim†

Department of Electronic Engineering, Sogang University, Seoul 04107, Korea

Abstract: A split gate MOSFET (SG-MOSFET) is widely known for reducing the reverse transfer capacitance (C_{RSS}). In a 3.3 kV class, the SG-MOSFET does not provide reliable operation due to the high gate oxide electric field. In addition to the poor static performance, the SG-MOSFET has issues such as the punch through and drain-induced barrier lowering (DIBL) caused by the high gate oxide electric field. As such, a 3.3 kV 4H-SiC split gate MOSFET with a grounded central implant region (SG-CIMOSFET) is proposed to resolve these issues and for achieving a superior trade-off between the static and switching performance. The SG-CIMOSFET has a significantly low on-resistance (R_{ON}) and maximum gate oxide field (E_{OX}) due to the central implant region. A grounded central implant region significantly reduces the C_{RSS} and gate drain charge (Q_{GD}) by partially screening the gate-to-drain capacitive coupling. Compared to a planar MOSFET, the SG MOSFET, central implant MOSFET (CIMOSFET), the SG-CIMOSFET improve the $R_{ON}\times Q_{GD}$ by 83.7%, 72.4% and 44.5%, respectively. The results show that the device features not only the smallest switching energy loss but also the fastest switching time.

Key words: 4H-SiC; split gate; on-resistance; reverse transfer capacitance; switching energy loss; switching time

Citation: J Yoon and K Kim, A 3.3 kV 4H-SiC split gate MOSFET with a central implant region for superior trade-off between static and switching performance[J]. *J. Semicond.*, 2021, 42(6), 062803. http://doi.org/10.1088/1674-4926/42/6/062803

1. Introduction

Silicon carbide (SiC) is considered to be a promising candidate for power applications, thanks to its superior material properties[1]. In particular, the SiC MOSFET has been proven to have lower switching time and loss compared to the Si insulated-gate bipolar transistor (IGBT)[2–4]. Recently, many studies on the SiC trench MOSFET have been conducted to achieve small cell pitches and high channel mobility. Rohm proposed a double-trench MOSFET that applies a grounded p^+ region in the source region to disperse the electric field and achieve low on-resistance (R_{ON})[5, 6]. However, a high electric field at the trench corner may lead to a reliability problem, which in turn makes it difficult to meet the required 3 MV/cm oxide reliability limit[7]. In the 3.3 kV class, this problem becomes more pronounced and the channel resistance does not have a significant effect on the overall resistance due to the thick drift region. Compared to the trench MOSFETs, the simpler fabrication process and lower reverse transfer capacitance (C_{RSS}) of the planar MOSFETs are more suitable for high voltage (3.3 kV or larger) and fast switching applications.

There are many approaches to reduce the C_{RSS} (or Q_{GD}) in planar MOSFETs. The most widely known structure is the split gate MOSFET (SG-MOSFET), which splits the gate polysilicon to reduce the gate oxide capacitance (C_{OX}). The SG-MOSFET not only has inferior static characteristics compared to that of the planar MOSFET, but also has a problem that the electric field is concentrated in the gate corner. As a result, the concentrated electric field concentrated at the gate corner can lead to punch through problems[8]. To resolve these issues, various structures using the split gate concept have been studied. Agarwal *et al.*[9] successfully manufactured a 2.3 kV class SG-MOSFET, but failed to meet the 3 MV/cm limit. Han *et al.*[10] proposed a buffered-gate MOSFET (BG-MOSFET) to lower the oxide field. However, the BG-MOSFET features a long cell pitch and high R_{ON}. Vudumula *et al.*[11] obtained dramatic reduction in the C_{RSS} by introducing a shorted-dummy gate between the split gates. Although the shielding effect of the dummy gate led to an increased breakdown voltage (BV), the depletion region caused by the dummy gate led to a higher R_{ON} compared to that of a typical SG-MOSFET. Cree reported a central implant MOSFET (CIMOSFET) in which a p-type implant region was introduced in the middle of the JFET region of a planar MOSFET[12, 13]. The CIMOSFET can significantly reduce the gate oxide field and C_{RSS} by introducing a grounded central implant region. Furthermore, by increasing the drift concentration they were able to achieve a lower R_{ON} compared to that of a planar MOSFET. However, the grounded central implant region of the CIMOSFET may increase the parasitic input capacitance (C_{ISS}) and negatively affect the switching time. Therefore, it seems very difficult to improve both static and switching performance in the SG-MOSFET. Moreover, research on the SG-MOSFET structure has only been studied up to the 2.3 kV class, and it is not clear whether the split gate concept can be applied to the 3.3 kV class.

A novel 3.3 kV split gate MOSFET with a central implant region (SG-CIMOSFET) is proposed and analyzed in comparison with the planar MOSFET, SG-MOSFET and CIMOSFET. Because of the high drain bias voltage in the 3.3 kV class, the SG-MOSFET does not guarantee the 3 MV/cm oxide limit. In addition, the SG-MOSFET suffers from issues such as punch through and drain-induced barrier lowering (DIBL), which make it more difficult to design. However, the SG-CIMOSFET

Correspondence to: K Kim, kimks@sogang.ac.kr
Received 4 NOVEMBER 2020; Revised 12 JANUARY 2021.
©2021 Chinese Institute of Electronics

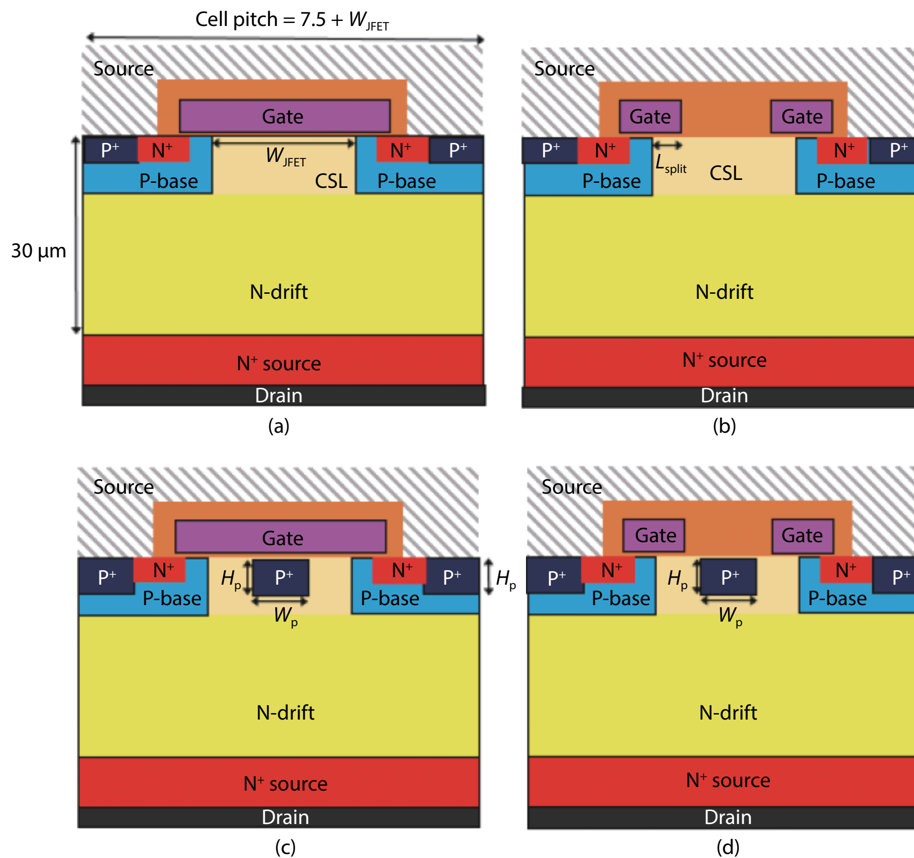

Fig. 1. (Color online) Schematic cross-sectional views of the MOSFETs. (a) Planar MOSFET. (b) SG-MOSFET. (c) CIMOSFET. (d) SG-CIMOSFET.

blocks the oxide electric field by introducing a central implant region in the JFET region and resolves all these issues of the SG-MOSFET. Like the CIMOSFET, the SG-CIMOSFET can significantly reduce the R_{ON} because of the high drift doping concentration. By applying the split gate structure and grounded central implant region, the C_{OX} and bulk depletion capacitance (C_{dep}) of the SG-CIMOSFET are reduced simultaneously. In addition, the grounded central implant region partially screens the gate-to-drain capacitive coupling as seen in the CIMOSFET, resulting in the lowest C_{RSS} in spite of the high drift concentration. Since the gate is not directly in contact with the central implant region, the C_{ISS} can be reduced significantly compared to that of the CIMOSFET. As a result, the SG-CIMOSFET has the best high frequency figure of merit (HF-FOM) in terms of $R_{ON}\times Q_{GD}$, $R_{ON}\times C_{RSS}$, $R_{ON}\times Q_G$ and achieving a superior switching time as well as switching loss. Thus, the SG-CIMOSFET boasts a superior trade-off between static and switching performance.

2. Device structure and optimization

This study was conducted by the Sentaurus TCAD tool[14]. The electron/hole continuity equations and the Poisson equations were solved using doping-dependent Shockley–Read–Hall (SRH) recombination, Auger recombination, inversion and accumulation layer mobility models, and Okuto-Crowell models[15, 16]. The mobility model contains incomplete ionization, high-field velocity saturation, and band narrowing models.

2.1. Device structure and features

Fig. 1 shows the schematic cross-sectional views of the planar MOSFET, SG-MOSFET, CIMOSFET, and SG-CIMOSFET. In all device structures, the thickness of the 4H-SiC drift layer is 30 μm and the gate oxide thickness is 50 nm. In order to suppress the current flow disturbance resulting from the central implant region in the CIMOSFET and SG-CIMOSFET, a current spreading layer (CSL) with a doping concentration of 2×10^{16} cm^{-3} is introduced in all structures. The channel length and doping concentration are 0.5 μm and 2×10^{17} cm^{-3}, respectively. A fixed charge concentration of 1×10^{12} cm^{-2} is included at the SiC/SiO_2 interface for all devices. In the CIMOSFET and SG-CIMOSFET, the p$^+$ base and the central implant region is set to same depth to prevent additional mask consumption. The doping concentration of the central implant region is set to 5×10^{18} cm^{-3}.

2.2. Optimization of each structure

In this optimization process, the drift concentration of all structures starts at 2.2×10^{15} cm^{-3} to set BV of 3.3 kV in the planar MOSFET. Fig. 2(a) shows the maximum oxide electric field (E_{OX}) and R_{ON} changes of the planar MOSFET according to the JFET width (W_{JFET}). E_{OX} is obtained at V_{DS} = 3000 V and V_{GS} = 0 V. As the W_{JFET} decreases, the JFET resistance component increases significantly resulting in a high R_{ON}. However, a large W_{JFET} induces a high E_{OX} as it enhances the shielding ability of the p-base. Therefore, W_{JFET} = 2.5 μm (the cell pitch is 10 μm in all structures), which satisfies the 3 MV/cm oxide reliability limit, was adopted in the rest of the study. The relationship between the L_{split} and device characteristics is shown in Fig. 2(b). In Fig. 2(b), when L_{split} is less than 0.4 μm, E_{OX} is obtained when breakdown occurs because BV is less than 3000 V. As the L_{split} decreases so does the Q_{GD}. This is due to

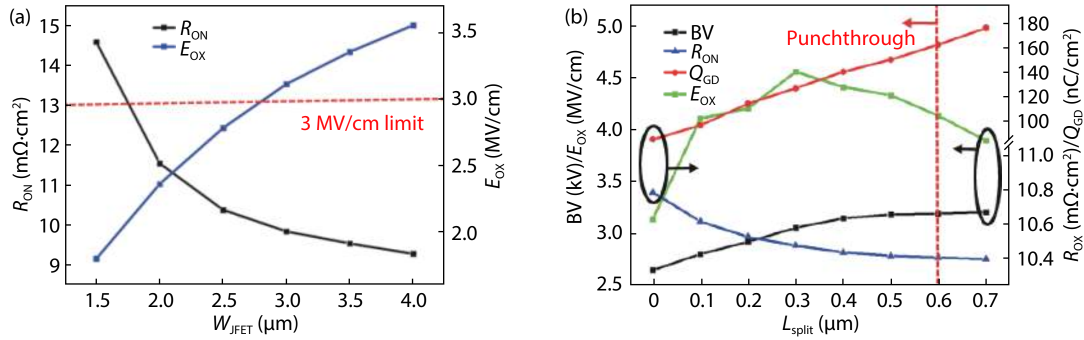

Fig. 2. (Color online) (a) E_{OX} and R_{ON} changes of the planar MOSFET according to the W_{JFET}, and (b) influence of the L_{split} on BV, R_{ON}, Q_{GD} and E_{OX} in SG-MOSFET. BV is extracted at V_{GS} = 0 V and I_{DS} = 1 μA/cm^2.

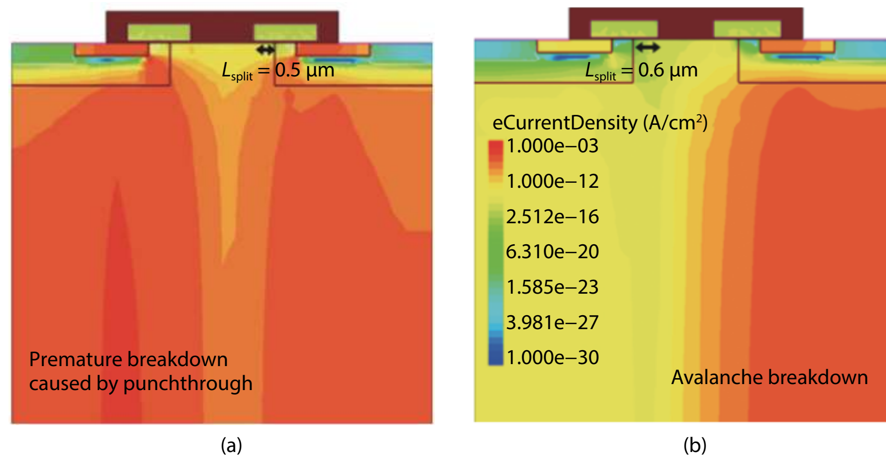

Fig. 3. (Color online) Electron current density distribution when breakdown occurs in the SG-MOSFET (a) when L_{split} = 0.5 μm, and (b) when L_{split} = 0.6 μm.

the decrease in the area between the gate and the drain. Simultaneously, the accumulation resistance increases and the field plate effect of the MOS structure decreases, leading to degradation in the R_{ON} and BV[17, 18]. Therefore, changes in the L_{split} results in a trade-off between the static and dynamic characteristics. The SG-MOSFET shows a high oxide field at all L_{split} values due to its high drain bias voltage. Even if the gate does not protrude (when breakdown occurs at L_{split} = 0 μm), it shows 3.138 MV/cm of E_{OX}, which does not satisfy the 3 MV/cm limit. Furthermore, the electric field concentrated at the edge of the gate increases the depletion of the p-base region, which can result in punch through if it extends to the N$^+$ source region. Fig. 3 shows the electron current density distribution when breakdown occurs in the SG-MOSFET. If L_{split} is less than 0.6 μm, premature breakdown due to punch through occurs. On the other hand, when L_{split} is 0.6 μm or more, the electric field is far away from the p-base and N-drift junction, and premature breakdown can be suppressed. But long L_{split} cannot achieve a low Q_{GD} compared to the planar MOSFET (210.37 nC/cm^2), and the purpose of the split gate is lost. To solve this punch through problem, a long channel can be considered[11]. However, if the channel length is increased, the V_{TH}, R_{ON}, cell pitch, and Q_{GD} all increase. As a result, the SG-MOSFET is not the best option in the 3.3 kV class for these given problems. The central implant region is a good solution to these problems.

Considering static and switching characteristics, the L_{split} = 0.3 μm was chosen for SG-CIMOSFET and SG-MOSFET in the rest of the study. Fig. 4(a) shows the R_{ON} and BV relation in the SG-CIMOSFET according to changes in the central implant width (W_P) and height (H_P). As W_P and H_P increase, the depletion region of the JFET region expands and the R_{ON} increases. However, the central implant area under the oxide disperses the electric field along with the p-base, greatly reducing the E_{OX} and increasing the BV. When H_P is small, the electric field dispersion effect is weak in the central implant region, and impact ionization still occurs in the p-base region (Fig. 4(b)). On the other hand, when H_P becomes large (0.6 μm or more), an excessive electric field is concentrated in the central implant region and impact ionization occurs only in the central implant region (Fig. 4(c)). When the W_P is 0.8 μm and H_P is 0.5 μm, impact ionization occurs simultaneously in the p-base and the central implant region. In this way, the highest BV (3940 V) and BV^2/R_{ON} of 1281.88 MW/cm^2 were obtained as shown in Fig. 4(d). Introduction of the central implant region in the SG-CIMOSFET greatly reduces the maximum oxide field to less than 1.4 MV/cm in all the cases in Fig. 5(a). As a result, punch through is suppressed in SG-CIMOSFET. Therefore, the SG-CIMOSFET can apply a short channel length while suppressing punch through problems when compared to the SG-MOSFET. Fig. 5(b) shows the Q_{GD} variation with respect to W_P and H_P. As the W_P and H_P increase, Q_{GD} becomes smaller because of the depletion expansion. Notably, increasing W_P has a greater impact on the decrease of

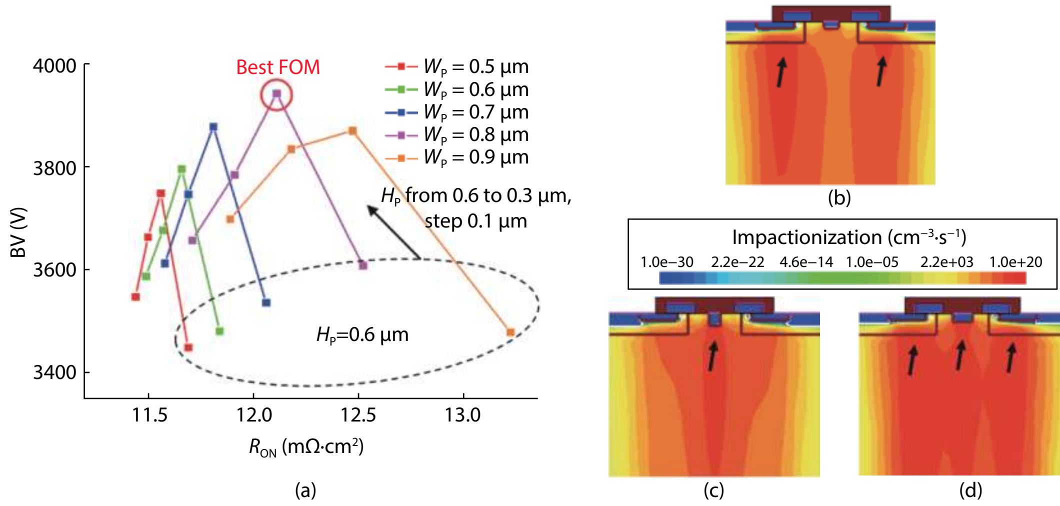

Fig. 4. (Color online) (a) R_{ON} and BV relation in the SG-CIMOSFET according to change in W_P and H_P. (b)–(d) Impact ionization position when breakdown occurs in the SG-CIMOSFET according to change in W_P and H_P (the arrow indicates the breakdown point).

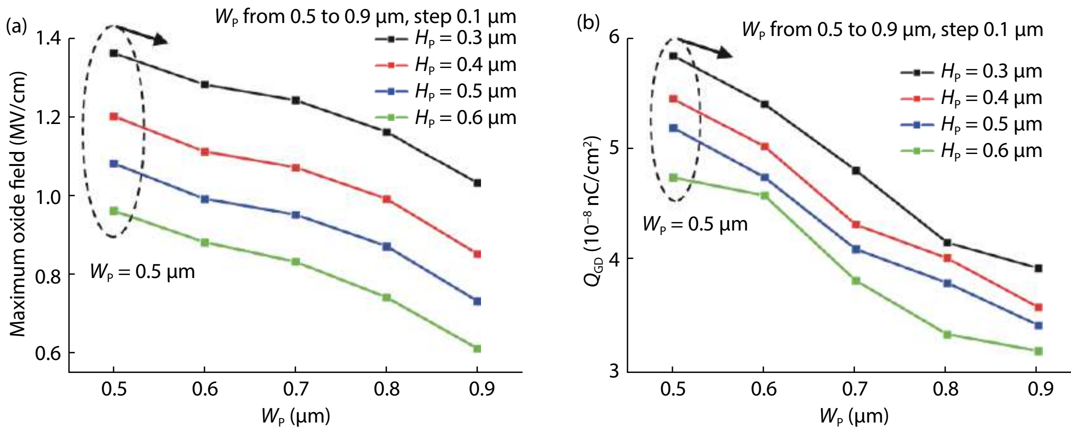

Fig. 5. (a) E_{OX} changes and (b) Q_{GD} changes in the SG-CIMOSFET according to change in W_P and H_P. E_{OX} is obtained at V_{DS} = 3000 V and V_{GS} = 0 V.

Q_{GD} than increasing H_P. This is because the grounded central implant region partially screens the capacitive coupling between the gate and the drain as W_P increases. Detailed analysis of the capacitance and gate charge characteristics will be covered in the next section. Consequently, the lowest $R_{ON}\times Q_{GD}$ of 418.17 mΩ·nC and BV^2/R_{ON} of 1199.79 MW/cm² were obtained for W_P = 0.8 μm and H_P = 0.6 μm. However, this study chose to move forward with W_P = 0.8 μm and H_P = 0.5 μm, which resulted in the best BV^2/R_{ON} and had an adequately low $R_{ON}\times Q_{GD}$ of 460.18 mΩ·nC. CIMOSFET also adopted these parameters as it resulted in the best BV^2/R_{ON}. The CIMOSFET was almost the same BV (3949 V) as the SG-CIMOSFET. However, it has a lower R_{ON} (11.19 mΩ·cm²) than the SG-CIMOSFET (12.11 mΩ·cm²) due to its accumulation layer resistance. After parameter optimization, the BV of the SG-CIMOSFET and CIMOSFET was set to 3.3 kV by adjusting the drift doping concentration (3×10^{15} cm^{-3}) in order to compare the R_{ON} of four devices in the 3.3 kV class.

3. Results and discussions

3.1. Static characteristics

Fig. 6 shows the *I–V* characteristics of four devices. R_{ON} is obtained for V_{GS} = 20 V. BV is extracted at V_{GS} = 0 V and I_{DS} = 1 μA/cm². The R_{ON} of planar MOSFET, SG-MOSFET, CIMOSFET, and SG-CIMOSFET are 10.39, 10.49, 8.59, and 8.67 mΩ·cm², respectively. Due to the increased drift doping concentration, CIMOSFET and SG-CIMOSFET were able to significantly improve their R_{ON}. Also, the SG-CIMOSFET has nearly the same R_{ON} as the CIMOSFET. This is because the current disturbance due to the accumulation resistance is minimized due to the improvement of the drift resistance, which occupies most of the total resistance. The off-state electric field distributions are shown in Fig. 7. Due to the split gate structure of the SG-MOSFET, the electric field is concentrated on the gate edge (E_{OX} = 4.56 MV/cm) and thus the 3 MV/cm reliability limit cannot be met. However, due to the introduction of the central implant region, the electric field is dispersed in the SG-CIMOSFET, reducing the E_{OX} by 2.5 times compared to the planar MOSFET and 4.3 times compared to the SG-MOSFET. CIMOSFET shows the lowest E_{OX} (0.97 MV/cm) but is not significantly different from that of the SG-CIMOSFET (1.06 MV/cm). Fig. 8 shows the band diagram in the channel of the four devices at V_{DS} = 0 V (solid line) and V_{DS} = 3000 V (dotted line). When V_{DS} = 0 V, the band diagram of the four devices is nearly the same because of the same p-base and CSL doping concentration. However, the SG-MOSFET and planar MOSFET show the severe barrier lowering at V_{DS} = 3000 V because of the potential around the channel resulting from the high electric field. The CIMOSFET and SG-CIMOSFET show excellent DIBL supp-

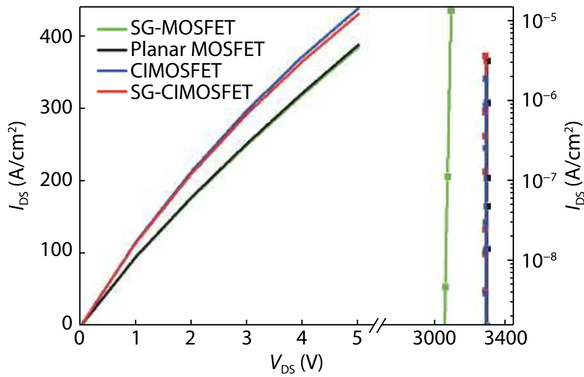

Fig. 6. The I–V characteristics of the four devices. R_{ON} and saturation current is obtained for V_{GS} = 20 V. BV is extracted at V_{GS} = 0 V and I_{DS} = 1 μA/cm².

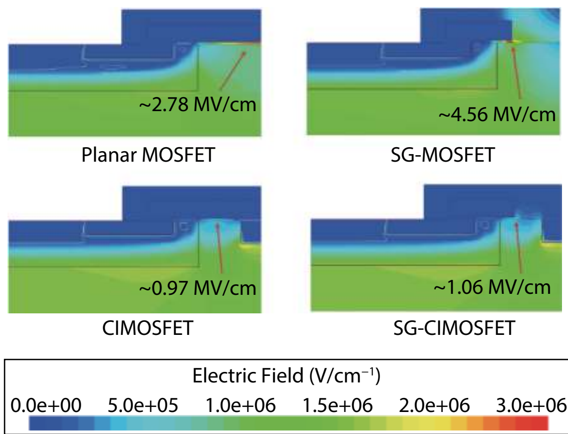

Fig. 7. (Color online) Off-state electric field distributions of the four devices when V_{GS} = 0 V and V_{DS} = 3000 V.

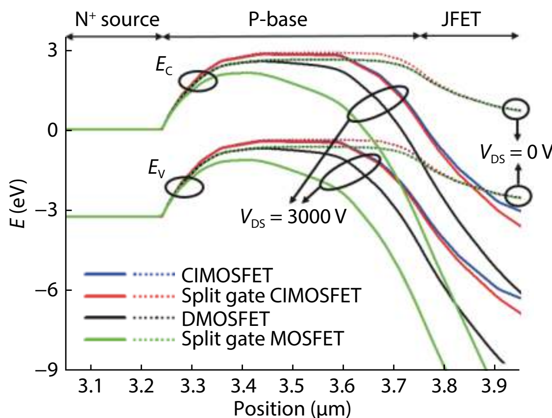

Fig. 8. (Color online) The band diagram in the channel of the four devices at V_{DS} = 0 V, V_{DS} = 3000 V in off-state.

ression due to the electric field shielding of the central implant region.

3.2. Capacitance and gate charge characteristics

For the analysis of the capacitance characteristics, the SG-CIMOSFET with floating central implant region is added to understand the capacitance characteristics. Fig. 9 shows the capacitance characteristics as a function of V_{DS} for the five devices. The CIMOSFET has the largest C_{ISS} due to the overlap of the grounded central implant region and the gate. This in turn increases the switching time. In contrast, the SG-CIMOSFET shows a great reduction in C_{ISS} compared to the CIMOSFET, due to the separation of the central implant region and gate. In general, the C_{RSS} is expressed by the following equation[8]:

$$C_{RSS} = \frac{C_{ox}C_{dep}}{C_{ox} + C_{dep}}, \tag{1}$$

where C_{OX} is the gate oxide capacitance and C_{dep} is the bulk depletion capacitance. The SG-MOSFET reduces the C_{RSS} by reducing the C_{OX}. But at low V_{DS}, due to its shallow depletion region, the split gate structure induces a large C_{dep} compared to that of the planar MOSFET, as shown in Fig. 10(a)[8]. Therefore, the C_{RSS} of the SG-MOSFET temporarily becomes larger than the C_{RSS} of the planar MOSFET in the vicinity of V_{DS} = 10 V, which is shown in the inset of Fig. 9(a). The CIMOSFET reduces the C_{RSS} in two ways. First, C_{dep} decreases with the expansion of the depletion region of the bulk region. Second, the grounded central implant region under the gate screens the gate-to-drain capacitive coupling[19]. CIMOSFET has low C_{RSS} despite having shallow depletion regions in high V_{DS} (Fig. 10(b)) due to high drift doping concentration compared to SG-MOSFET and planar MOSFET. Therefore, screening the gate-to-drain capacitive coupling is the main reason for C_{RSS} reduction. At a low V_{DS}, the floating SG-CIMOSFET and SG-CIMOSFET have lower C_{RSS} than SG-MOSFET due to the wider depletion region by the central implant region as shown in Fig. 10(a). On the other hand, at a high V_{DS}, the floating SG-CIMOSFET exhibits slightly higher C_{RSS} than SG-MOSFET because of the large depletion region due to high drift doping concentration. But in SG-CIMOSFET, the grounded central implant region partially screens the gate-to-drain capacitive coupling like a CIMOSFET, resulting in the lowest C_{RSS}. Therefore, as the W_P increases, the amount of screening gate-to-drain capacitive coupling increases, resulting in a sharp decrease in Q_{GD} as shown in Fig. 5(b). The drain source capacitance (C_{DS}) characteristics of the five devices is shown in Fig. 9(b). The grounded central implant region of the CIMOSFET and SG-CIMOSFET cause an increase in C_{DS}. C_{DS} of the floating SG-CIMOSFET is larger than that of SG-MOSFET and planar MOSFET. It is due to the shallow depletion region caused by the high drift concentration. As a result, the grounded central implant region converts part of the C_{RSS} to C_{DS} and C_{GS} as shown in the capacitance model of the SG-CIMSOFET and the CIMOSFET (Fig. 10(a))[20]. Increases in C_{DS} lead to an increase in output capacitance (C_{OSS} = C_{DS} + C_{GD}), which affects the reverse recovery characteristics of MOSFET due to the discharging current. However, the increase in C_{DS} is not insignificant, and the effect of reducing C_{RSS} is even greater. This further reduces the switching energy loss compared to SG-MOSFET. Detailed analysis of switching characteristics is shown in the next section.

The gate charge characteristics of the four devices are shown in Fig. 11. The mixed-mode TCAD simulation circuit is shown in the inset of Fig. 11. The Q_{GD} is obtained by overlaying the V_{DS} waveform with the gate charge characteristic (measured at 90% of the V_{DS} to 10% of the V_{DS})[21]. The total gate charge (Q_G) is defined as the gate charge from V_{GS} = 0 V to V_{GS} = 20 V. The Q_G, Q_{GD}, and Q_{TH} values of the four devices are shown in Table 1. The SG-CIMOSFET has the lowest Q_{GD} (42.49 nC/cm²) and Q_G (424.85 nC/cm²). The CIMOSFET has

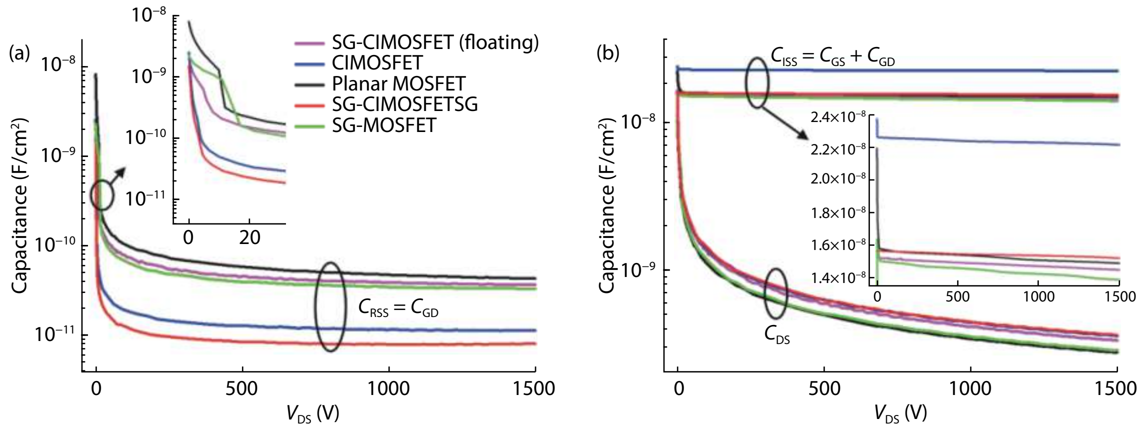

Fig. 9. (Color online) (a) Reverse transfer capacitance characteristics (C_{RSS}) of the five devices. (b) Input capacitance (C_{ISS}) and drain source capacitance (C_{DS}) characteristics of the five devices (when V_{GS} = 0 V, AC signal of 1 MHz).

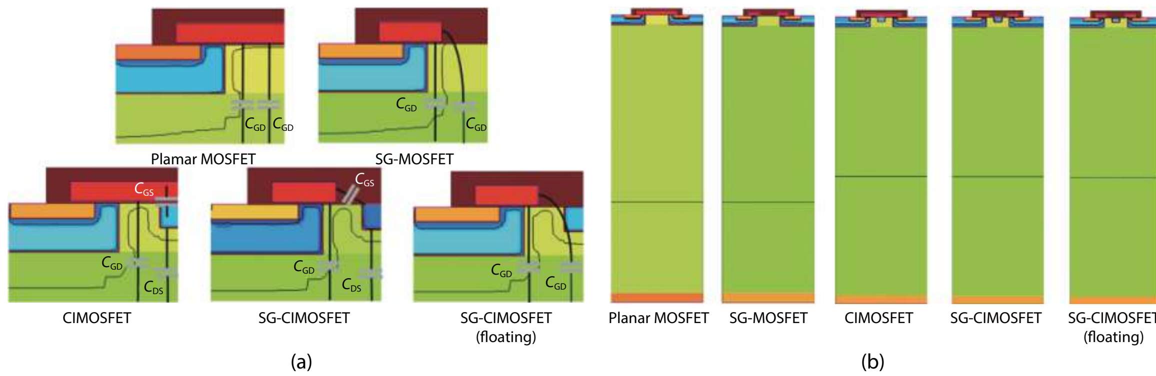

Fig. 10. (Color online) (a) Depletion lines and reverse transfer capacitance models of the five devices when V_{DS} = 0 V, V_{GS} = 0 V. (b) Depletion lines of the five devices when V_{DS} = 800 V, V_{GS} = 0 V. The solid black line represents the depletion layer.

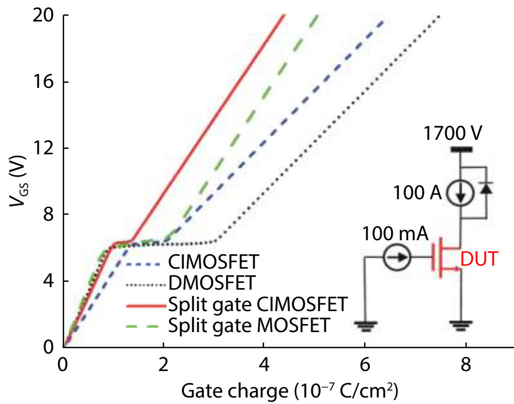

Fig. 11. Gate charge characteristics and test circuit of the four devices.

Table 1. Device characteristics comparison.

Parameter	Planar MOSFET	SG-MOSFET	CI-MOSFET	SG-CIMOSFET	Unit
N-drift doping concentration	2.2 × 10^{15}	2.2 × 10^{15}	3 × 10^{15}	3 × 10^{15}	cm^{-3}
R_{ON} [a]	10.39	10.49	8.59	8.67	mΩ·cm²
E_{OX} [b]	2.78	4.56	0.97	1.06	MV/cm
Q_G [c]	754.06	503.62	651.56	424.85	nC/cm²
Q_{GD}	216.92	126.98	77.21	42.49	nC/cm²
Q_{TH}	72.32	60.95	112.48	80.12	nC/cm²
Q_{GD}/Q_{TH}	2.99	2.08	0.69	0.53	
C_{RSS} [d]	42.27	32.19	11.16	7.72	pF/cm²
C_{ISS} [d]	14.99	13.93	22.31	15.21	nF/cm²
C_{OSS} [d]	316.21	315.78	365.96	365.96	nF/cm²
R_{ON}×Q_{GD}	2254	1332	663	368	mΩ·nC
R_{ON}×Q_G	7834	5282	5597	3683	mΩ·nC
R_{ON}×C_{RSS}	439	338	96	67	mΩ·pF

[a] R_{ON} at V_{GS} = 20 V, [b] E_{OX} at V_{DS} = 3000 V, [c] Q_G is the total gate charge, which is the gate charge from V_{GS} = 0 to 20 V. [d] C_{ISS}, C_{OSS}, and C_{RSS} are measured at V_{DS} = 1500 V.

the second highest Q_{GD} (77.21 nC/cm²) but has a higher Q_G (651.56 nC/cm²) than the SG-MOSFET (503.62 nC/cm²) due to its high C_{ISS}. Therefore, the SG-CIMOSFET features best characteristics in terms of Q_G, Q_{GD}, and C_{RSS}. In addition, it has the smallest Q_{GD}/Q_{TH} value, which helps to suppress the parasitic turn-on effect[21, 22]. The comprehensive performance of the four devices are shown in Table 1. The SG-CIMSOFET boasts the lowest HF-FOM in terms of R_{ON}×Q_{GD}, R_{ON}×C_{RSS}, and R_{ON}×Q_G.

3.3. Switching characteristics

The switching performance analysis of each device are conducted through a double pulse test (DPT) by the mixed-mode TCAD simulation. The active areas of all devices under test (DUT) are set to 1 cm². Fig. 12 shows the switching waveforms of the four devices. The test circuit for DPT is shown in Fig. 13(a). The body diode of the DUT was used as a freewheeling diode. The gate resistance and stray inductance are set

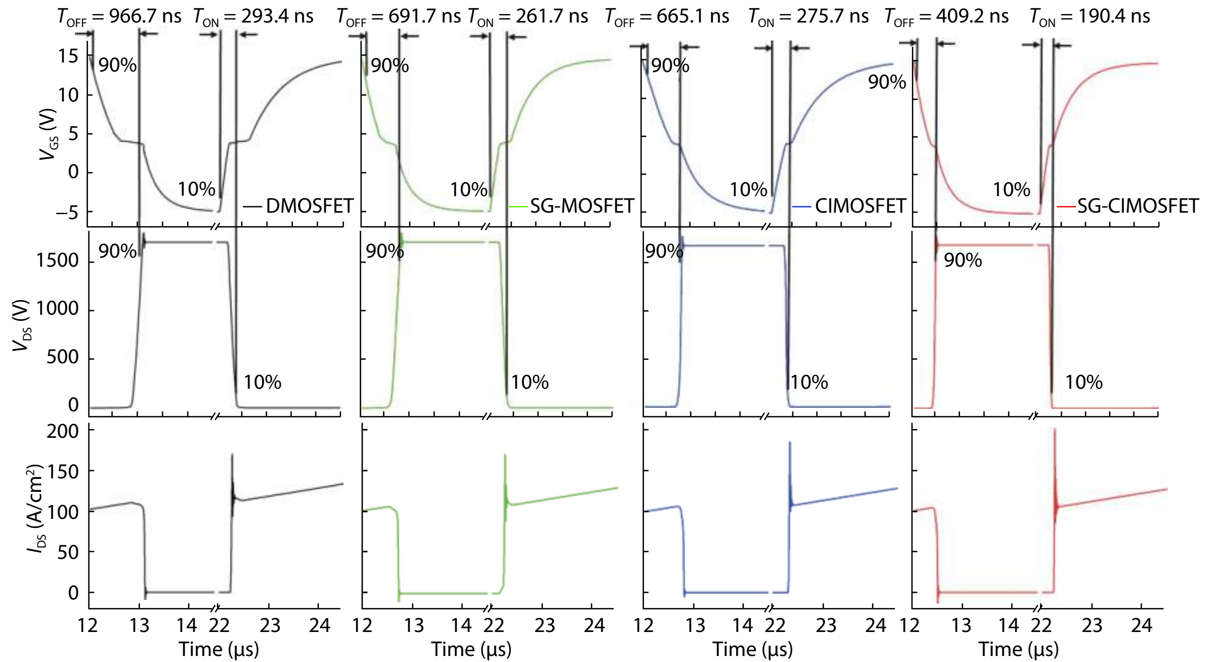

Fig. 12. Switching waveforms of the four devices. The active areas of all DUT are set to 1 cm².

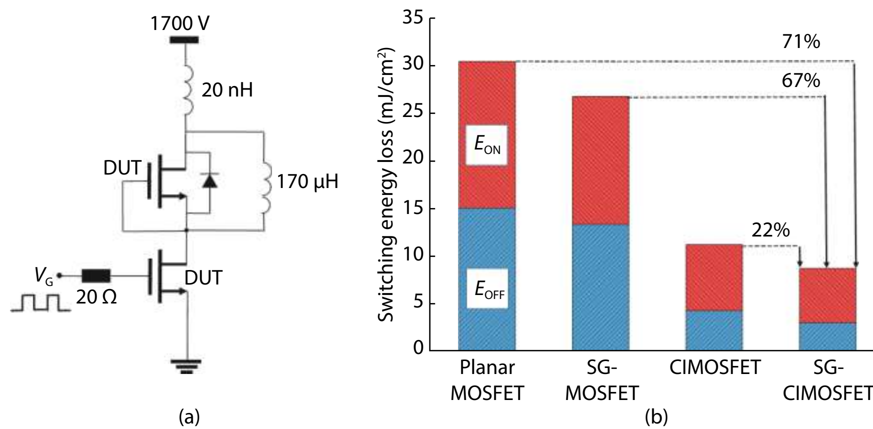

Fig. 13. (Color online) (a) Double pulse test circuit. (b) Switching energy loss diagrams of the four devices.

to 20 Ω and 20 nH, respectively. The load inductor is set to 170 μH and the first V_{GS} pulse lasted for 10 μs to yield a load current of 100 A/cm^2. The gate voltage is switched between 15 and –5 V. In this paper, the turn-off time (T_{OFF}) consists of two parts, the turn-off delay time ($T_{D\text{-}OFF}$: from 90% of V_{GS} to 10% of V_{DS}) and the turn-off fall time (T_F: from 10% of V_{DS} to 90% of V_{DS}). The turn-on time (T_{ON}) consists of two parts, the turn-on delay time ($T_{D\text{-}ON}$: from 10% of V_{GS} to 90% of V_{DS}) and the turn-on rise time (T_R: from 90% of V_{DS} to 10% of V_{DS})[23]. Due to its low C_{RSS}, the SG-CIMOSFET shows the largest dV/dt, resulting in the fastest switching time in terms of T_{OFF} and T_{ON}. The CIMOSFET also shows faster T_F and T_R compared to the planar MOSFET and SG-MOSFET due to its low C_{RSS}. However, the CIMOSFET shows fairly slow $T_{D\text{-}OFF}$ and $T_{D\text{-}ON}$ due to its high C_{ISS}. As a result, the CIMOSFET exhibits T_{OFF} and T_{ON} similar to that of the SG-MOSFET despite its low C_{RSS}. Fig. 13(b) shows the switching energy loss diagrams of the four devices. Because the body diode of the DUT was used as a freewheeling diode, E_{ON} contains the reverse recovery energy of the DUT. It shows the E_{ON} of the SG-CIMSOFET is much smaller than planar MOSFET and SG-MOSFET. This means that although grounded central implant region increases the reverse recovery energy, reduction of switching energy loss because of the reduced C_{RSS} is more dominant in SG-CIMOSFET. The total switching energy loss (E_{TOTAL}) of the SG-CIMOSFET decreased by 71%, 67%, and 22%, respectively, compared to the planar MOSFET, SG-MOSFET, and CIMOSFET. The comprehensive switching performance of the four devices is shown in Table 2. SG-CIMOSFET boasts the best switching performance in terms of switching energy loss and switching time. As a result, SG-CIMOSFET can achieve a superior trade-off between static and switching performance.

4. Proposed fabrication process

Fig. 14 shows the proposed fabrication procedure of SG-CIMSOFET. After N-type epitaxial growth, the p-base and N$^+$ source region can be formed by ion implantation as shown in Fig. 14(b). In Fig. 4, it shows that the static characteristics of SG-CIMOSFET according to W_P and H_P are very sensitive. To minimize the sensitivity of parameters, tilt implantation

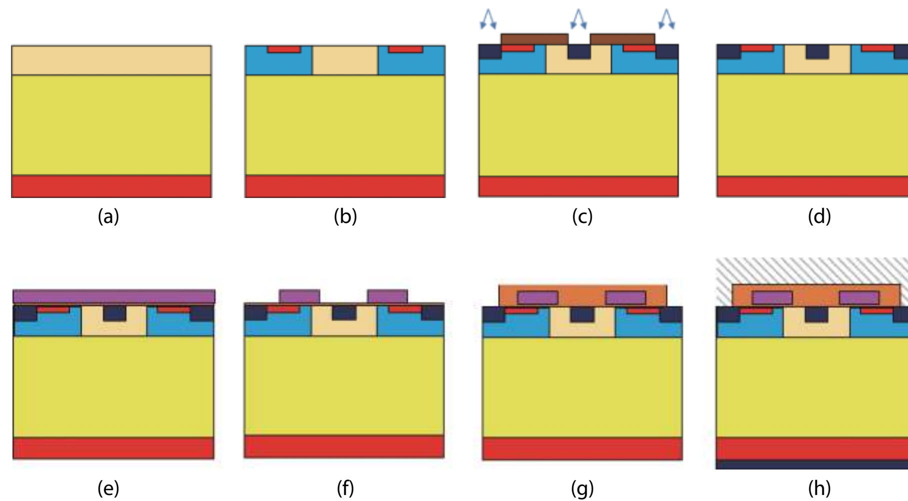

Fig. 14. (Color online) Proposed fabrication procedure of SG-CIMSOFET. (a) N-type epitaxial growth. (b) Form the base and N+ source region. (c) Form the P+ base and central implant region by tilt ion implantation. (d) Thermal oxidation. (e) Polysilicon deposition. (f) Polysilicon etching. (g) ILD oxide deposition and contact hole etching. (h) Metallization to form the source and drain.

Table 2. Switching characteristics comparison.

Parameter	Planar	SG-	CI-	SG-CI	Unit
$T_{D\text{-}OFF}$	795.4	540.6	603.6	363.1	ns
T_F	171.3	151.1	61.5	46.1	ns
T_{OFF}	966.7	691.7	665.1	409.2	ns
$T_{D\text{-}ON}$	159.2	146.1	227.5	154.1	ns
T_R	134.2	115.6	48.2	36.4	ns
T_{ON}	293.4	261.7	275.7	190.5	ns
E_{OFF}	15.1	13.4	4.4	3.1	mJ/cm²
E_{ON}	15.3	13.4	6.9	5.7	mJ/cm²
E_{TOTAL} [a]	30.4	26.8	11.3	8.8	mJ/cm²

[a] E_{TOTAL} is the sum of E_{ON} and E_{OFF}.

can be used to form the central implant region. The W_P and H_P can be determined by the implantation parameters[24]. Since the P+ base region and the central implant region are simultaneously formed by ion implantation, it is possible to prevent additional mask consumption as shown in Fig. 14(c). The gate oxide with a thickness of 50 nm is formed by thermal oxidation. Then, polysilicon deposition and etching was carried out to form split gate structure. After ILD oxide deposition, the contact hole etching process followed to shorten the source and central implant region in Fig. 14(g)[25]. Lastly, the metallization process followed to form the source and drain contact.

5. Conclusion

In this paper, a novel 3.3 kV class 4H-SiC SG-CIMOSFET is proposed. In the 3.3 kV class, the SG-MOSFET does not guarantee reliable operation due to its high oxide electric field. Moreover, the SG-MOSFET is very vulnerable to the punch through and has been shown to suffer from severe DIBL effect, which makes it more difficult to design devices. The SG-CIMOSFET resolves these problems by applying a central implant region and lowers the E_{OX} by 4.3 times compared to SG-MOSFET. Furthermore, due to its increased drift doping concentration, the SG-CIMOSFET is able to significantly improve R_{ON}. In addition, the SG-CIMOSFET significantly lowers the C_{RSS} by partially screening the gate-to-drain capacitive coupling. Compared to the planar MOSFET, the SG MOSFET and the CIMOSFET, the SG-CIMOSFET improves the $R_{ON}\times Q_{GD}$ by 83.7%, 72.4% and 44.5%, respectively. As a result, the SG-CIMOSFET shows the best performance in terms of switching energy loss and switching time. In addition to its simple fabrication process, the SG-CIMOSFET boasts superior trade-off between static and switching performance, making it a promising candidate for high voltage and high frequency applications.

Acknowledgements

This research was supported by the MSIT (Ministry of Science and ICT), Korea, under the ITRC (Information Technology Research Center) support program (IITP-2020-2018-0-01421) supervised by the IITP (Institute for Information & communications Technology Promotion), and then Samsung Electronics.

References

[1] Baliga B J. Power MOSFETs Fundamentals of power semiconductor devices. Boston, MA: Springer US, 2008, 276
[2] Ji S Q, Zhang Z Y, Wang F. Overview of high voltage sic power semiconductor devices: Development and application. CES Trans Electr Mach Syst, 2017, 1, 254
[3] Cooper J A, Agarwal A. SiC power-switching devices-the second electronics revolution. Proc IEEE, 2002, 90, 956
[4] Wang G Y, Wang F, Magai G R, et al. Performance comparison of 1200V 100A SiC MOSFET and 1200V 100A silicon IGBT. 2013 IEEE Energy Convers Congr Expo, 2013, 3230
[5] Nakamura T, Nakano Y, Aketa M, et al. High performance SiC trench devices with ultra-low R_{on}. 2011 International Electron Devices Meeting, 2011, 26.5.1
[6] Sampath M, Morisette D T, Cooper J A. Comparison of single- and double-trench UMOSFETs in 4H-SiC. Mater Sci Forum, 2018, 924, 752
[7] Krishnaswami S, Das M, Hull B, et al. Gate oxide reliability of 4H-SiC MOS devices. 2005 IEEE International Reliability Physics Symposium, 2005, 592
[8] Xu S M, Ren C H, Liang Y C, et al. Theoretical analysis and experimental characterization of the dummy-gated VDMOSFET. IEEE Trans Electron Devices, 2001, 48, 2168

[9] Agarwal A, Han K, Baliga B J. 2.3 kV 4H-SiC accumulation-channel split-gate planar power MOSFETs with reduced gate charge. IEEE J Electron Devices Soc, 2020, 8, 499
[10] Han K, Baliga B J, Sung W. A novel 1.2 kV 4H-SiC buffered-gate (BG) MOSFET: Analysis and experimental results. IEEE Electron Device Lett, 2018, 39, 248
[11] Vudumula P, Kotamraju S. Design and optimization of 1.2-kV SiC planar inversion MOSFET using split dummy gate concept for high-frequency applications. IEEE Trans Electron Devices, 2019, 66, 5266
[12] Zhang Q C J, Duc J, Hull B, et al. CIMOSFET: A new MOSFET on SiC with a superior $R_{on}{\cdot}Q_{gd}$ figure of merit. Mater Sci Forum, 2015, 821–823, 765
[13] Zhang Q J, Wang G Y, Doan H, et al. Latest results on 1200 V 4H-SiC CIMOSFETs with R_{sp}, on of 3.9 mΩ·cm^2 at 150 °C. 2015 IEEE 27th International Symposium on Power Semiconductor Devices & IC's (ISPSD), 2015, 89
[14] TCAD Sentaurus Device Manual, Synopsys. 2016, Inc., Mountain View, CA, USA
[15] Darwish M N, Lentz J L, Pinto M R, et al. An improved electron and hole mobility model for general purpose device simulation. IEEE Trans Electron Devices, 1997, 44, 1529
[16] Mujtaba S A. Advanced mobility models for design and simulation of deep submicrometer MOSFETs. PhD Dissertation, Stanford University, 1995
[17] Han K, Baliga B J, Sung W. Split-gate 1.2-kV 4H-SiC MOSFET: Analysis and experimental validation. IEEE Electron Device Lett, 2017, 38, 1437
[18] Wei J, Zhang M, Jiang H P, et al. Low ON-resistance SiC trench/planar MOSFET with reduced OFF-state oxide field and low gate charges. IEEE Electron Device Lett, 2016, 37, 1458
[19] Wei J, Zhang M, Jiang H P, et al. Dynamic degradation in SiC trench MOSFET with a floating p-shield revealed with numerical simulations. IEEE Trans Electron Devices, 2017, 64, 2592
[20] Ren M, Chen Z, Niu B, et al. A low miller capacitance VDMOS with shield gate and oxide trench. 2016 IEEE International Nanoelectronics Conference (INEC), 2016, 1
[21] Basler T, Heer D, Peters D, et al. Practical aspects and body diode robustness of a 1200 V SiC trench MOSFET. International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, 2018, 1
[22] Maerz A, Bertelshofer T, Bakran M, et al. A novel gate drive concept to eliminate parasitic turn-on of SiC MOSFET in low inductance power modules. International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, 2017, 1
[23] Tian K, Hallén A, Qi J W, et al. An improved 4H-SiC trench-gate MOSFET with low ON-resistance and switching loss. IEEE Trans Electron Devices, 2019, 66, 2307
[24] Morikawa T, Ishigaki T, Shima A. Device design consideration for robust SiC VDMOSFET with self-aligned channels formed by tilted implantation. IEEE Trans Electron Devices, 2019, 66, 3447
[25] Zhou X T, Yue R F, Zhang J, et al. 4H-SiC trench MOSFET with floating/grounded junction barrier-controlled gate structure. IEEE Trans Electron Devices, 2017, 64, 4568

Jongwoon Yoon got his BS degree from Sogang University in 2020. Now he is in Master's course at Sogang University under the supervision of Prof. Kim. His research focuses on 4H-SiC MOSFET.

Kwangsoo Kim received his BS degree in 1981, MS degree in 1983, and PhD at Sogang University in 1992. Since then, he joined Electronics and Telecommunications Research Institute (ETRI), Institute for Information Technology Advancement (IITA) and Daegu Gyeongbuk Institute of Science and Technology (DGIST). In 2008, he joined Sogang University as a full professor. His research focuses on 4H-SiC semiconductor devices and process.